On Carving Basic Boolean Functions on Graphene Nanoribbons Conduction Maps

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***Abstract*—As CMOS feature size approaches atomic dimensions, unjustifiable static power, reliability, and economic implications are exacerbating, prompting for research and development on new materials, devices, and/or computation paradigms. Within this context, Graphene Nanoribbons (GNRs), owing to graphene's excellent electronic properties, may serve as basic blocks for carbon-based nanoelectronics. En route to GNR-based logic circuits, the ability to externally control GNRs' conduction to map a basic Boolean logic function onto its electrical characteristics, with a high $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio, and uncompromised carriers mobility, is the main desideratum. To this end, we augment a trapezoidal GNR with top gates as controlling inputs, and investigate its conductance G by means of the NEGF-Landauer formalism. Further, we demonstrate that the butterfly GNR can exhibit conduction maps (high G for logic $''1''$, and low G for logic $''0''$) capturing the functionality of 2 and 3-input Boolean gates, by properly adjusting its topology and dimensions. Our simulations prove butterfly GNR structure capability to capture basic Boolean logic transfer functions, while potentially providing $30\times$ and $3000\times$ smaller propagation delay and gate active area, respectively, when compared to $15\,\mathrm{nm}$ CMOS equivalent counterparts, establishing GNR's potential as basic building block for future graphene-based logic gates.**

***Index Terms*—Graphene, GNR, Graphene-based Boolean Gates, Carbon-Nanoelectronics.**

I. Introduction

As CMOS scaling is approaching atomic feature size, the faster switching speed comes at the expense of increased power density and leakage, decreased reliability and yield, increased production costs, and as a result diminishing returns, which calls for the development of new materials, structures, and computation paradigms [1], [2]. One of the post-Si forerunners is graphene, which has enjoyed a research surge in the past decade, paving the way for a wide range of graphene-based applications, e.g., electronics, spintronics, photonics and optoelectronics, sensors, energy storage and conversion, flexible electronics, and biomedical applications [3].

Graphene wealth of unique, remarkable properties, among which ballistic charge transport, room temperature carrier mobility $10\times$ higher than Si, and ultimate thinness, as well as the possibility of low-cost mass production, provide a strong drive to investigate its usage as a potent contender to Si technology and promising avenue for carbon-based nanoelectronics [4], [5], [6]. Generally speaking, the main impediments to graphene-based Boolean logic can be divided into design and manufacturing related [7], [8], [9], [10], [11]. From the manufacturing point of view, finding a cost-effective, scalable and reliable manufacturing process, which enables mass-production with minimum defects density and highly reproducible features, is the main desideratum. From the design perspective, several aspects have to be considered: (i) ability to control conductivity and yield distinguishable "on" and "off" states, while (a) not compromising any of the graphene intrinsic highly advantageous properties (e.g., high carrier mobility), and (b) providing an $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio in the order of 10^6 to 10^7 (i.e., the typical ratio for low power $<20\,\mathrm{nm}$ Si logic process), (ii) encoding the desired Boolean logic transfer function into the graphene electrical characteristics (e.g., conduction maps), (iii) finding proper external electric means (e.g., top gates, back gates) to control the graphene behavior and induce the desired logic functionality, and (iv) ensuring the conditions for cascading digital circuits (i.e., clean and compatible/matching electric levels, e.g., voltage, current, for the gates inputs and outputs).

In this paper, we address (ii) and (iii) related issues and demonstrate that by augmenting the trapezoidal Quantum Point Contact (QPC) topology in [12] with top gates, we can modulate its conductance by means of external voltages, such that it mirrors the behavior of basic Booelan functions. In particular, we consider a set of 2-input Boolean functions $\{\mathrm{AND}, \mathrm{NAND}, \mathrm{OR}, \mathrm{NOR}, \mathrm{XOR}, \mathrm{XNOR}\}$ and perform a Design Space Exploration (DSE) with regard to topology and dimensions of the proposed butterfly GNR, such that for each Boolean function, a conductance map (conductance G vs. top gate input controlling voltages) which reflects its Boolean functionality (high G for logic $''1''$, low G for logic $''0''$) is identified. For modelling the electronic transport properties of butterfly GNRs, we employ the NEGF-Landauer formalism [12], [13]. Simulation results prove butterfly GNR-based structure capability to mimic Boolean logic functions (as well as its potential scalability to more complex Boolean logic, e.g., with 3 inputs), with promising performance figures (e.g., $0.65\,\mathrm{eV}$ energy bandgap for 2-input XNOR function, $30\times$ and $3000\times$ smaller delay and gate active area, respectively, when compared to an XNOR gate in $15\,\mathrm{nm}$ CMOS technology), suggesting that butterfly GNRs are fundamental basic building blocks for the implementation of future graphene-based logic gates.

The remaining of this paper is structured as follows: Section II presents an overview of the utilized simulation framework. Section III entails the simulation results and comments on the potential of GNR-based Boolean logic design. Finally, some concluding remarks are given in Section IV.

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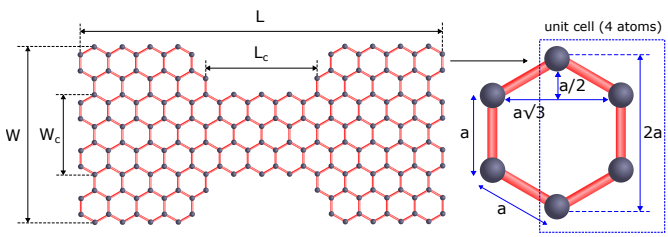

Fig. 1: Butterfly GNR dimensions.

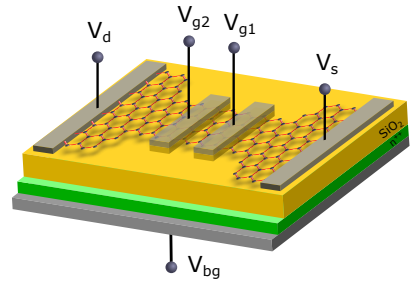

Fig. 2: Butterfly GNR-based basic building block structure.

II. Simulation Framework

In this paper, we investigate the potential of using GNRs as basic building blocks for future graphene-based logic gates, and deal with the following problem statement: Given a GNR with a specified initial shape and a desired Boolean logic transfer function, carve the GNR geometry and modulate its conductance (via external electric means, e.g., gate voltages), such that it reflects the desired logic functionality with good conduction properties. To this end, we present subsequently the underlying GNR-based structure, the simulation model of its electronic transport properties, followed by the design space exploration methodology that we employ for mirroring Boolean functions onto graphene conductance.

As GNR research vehicle, we build upon the trapezoidal QPC with zig-zag atomic edge alignment, described in [12]. We shape its geometry, with dimensions graphically defined in Figure 1, and further denote it as butterfly GNR. As illustrated in Figure 2, we employ the butterfly GNR as a conduction channel, through which the current flow is induced by applying a bias voltage (i.e., $V_{\rm d}-V_{\rm s}$) between the two end-point contacts of the graphene sheet, and is modulated by input voltages (i.e., $V_{\rm g1}$ and $V_{\rm g2}$), which are applied via two top gates. On the back of the graphene we apply a back-bias potential $V_{\rm back}$, which in manufactured devices is typically a small fraction of the back gate potential, i.e., $V_{\rm bg}$, (because of the significant potential drop on the dielectric layer - usually SiO_2 - residing underneath the graphene ribbon).

Based on this structure, we vary the nanoribbon geometry and the gate contacts topology, until a conduction map reflecting the desired Boolean functionality, is obtained. Specifically, we consider the set of 2-input Boolean functions $\{\text{AND}, \text{NAND}, \text{OR}, \text{NOR}, \text{XOR}, \text{XNOR}\}$, and apply voltage levels via the two top gates, as illustrated in Figure 2. We convene to use $0\,\text{V}$ and $1\,\text{V}$ as the voltage levels afferent to logic $''0''$ and logic $''1''$. We note that this choice is solely for explanatory purpose and is not restrictive in any way; one can also choose other voltage levels (e.g., $10\times$ or $100\times$ smaller), and for a certain Pareto butterfly GNR geometry, obtain a conduction map that complies with the desired Boolean logic. We set the left contact (drain) and the right contact (source) voltage to $0.2\,\text{V}$ and $0\,\text{V}$, respectively. For each Boolean logic function, we perform a design space exploration by varying the following: (i) the butterfly GNR dimensions defined in terms of the distance between adjacent carbon atoms, a ($1.42\,\text{Å}$), as depicted in Figure 1 (i.e., the nanoribbon total width, W, and length, L, from $41\,\text{a}$ to $47\,\text{a}$ and from $25\sqrt{3}$ a to $27\sqrt{3}$ a, respectively; and the constriction width, $W_{\rm c}$ and length, $L_{\rm c}$, from $2\,\text{a}$ to $35\,\text{a}$ and from $3\sqrt{3}$ a to $12\sqrt{3}$ a, respectively), (ii) the top gate contacts topology (i.e., the distance between the two top gate contacts, $P_{\rm Vg}$, symmetrically, with respect to the middle of the nanorribon from $\sqrt{3}$ a to $13\sqrt{3}$ a, and the contact width, $W_{\rm Vg}$ from $3\sqrt{3}$ a to $7\sqrt{3}$ a), and (iii) $V_{\rm back}$ from $-1\,\text{V}$ to $1\,\text{V}$ (in increments of $0.2\,\text{V}$).

For each design point, we derive the conductance map with respect to the 2-input top gate voltages. For modelling the electronic ballistic transport in GNRs, we employ the Non-Equilibrium Green Function (NEGF) quantum transport model, the semi-empirical Tight Binding (TB) computations to obtain the system Hamiltonian, and the Landauer formalism to derive the GNR current and conductance [12], [13]. In particular the current flow, when the GNR is exposed to the bias voltage $V = V_d - V_s$, writes as:

$$I(V) = \frac{\rm q}{\rm h} \int_{-\infty}^{\infty} T(E) \cdot (f(E-\mu_1) - f(E-\mu_2))\, {\rm d}E, \quad (1)$$

where $T(E)$ is the transmission function which describes the electrons (endowed with energy E) rate of transfer from the left to the right electrode; $f(E)$ denotes the Fermi-Dirac distribution function; $\mu_{1,2} = E_F \pm {\rm q}V/2$ represent the two electrodes Fermi Energy; q is the electrical charge; and h is the Plank constant. Based on (1), the conductance G is then estimated as: $G = I/V$.

The convergence criteria that we employed for the Pareto conduction maps are threefold: (i) for each (V_{g1}, V_{g2}) pair of inputs ($(0,0)$, $(0,1)$, $(1,0)$ and $(1,1)$), the conductance magnitude should mirror the desired Boolean output logical value, (ii) the standard deviation of all conductance values corresponding to logic $''0''$ (logic $''1''$) should be smaller than a certain imposed percentage, e.g., 10%, and (iii) given that no optimization with respect to the $I_{\rm ON}/I_{\rm OFF}$ ratio is targeted, the worst ratio between the logic $''1''$ and logic $''0''$ conductance should be ≥ 10.

In the next Section, we present the DSE simulation results which correspond to a set of logic functions, and discuss the implications for graphene-based Boolean logic design.

III. GNR Conduction Carving

This Section entails the conduction plots for 2 and 3-inputs butterfly GNR structures, mapping the set

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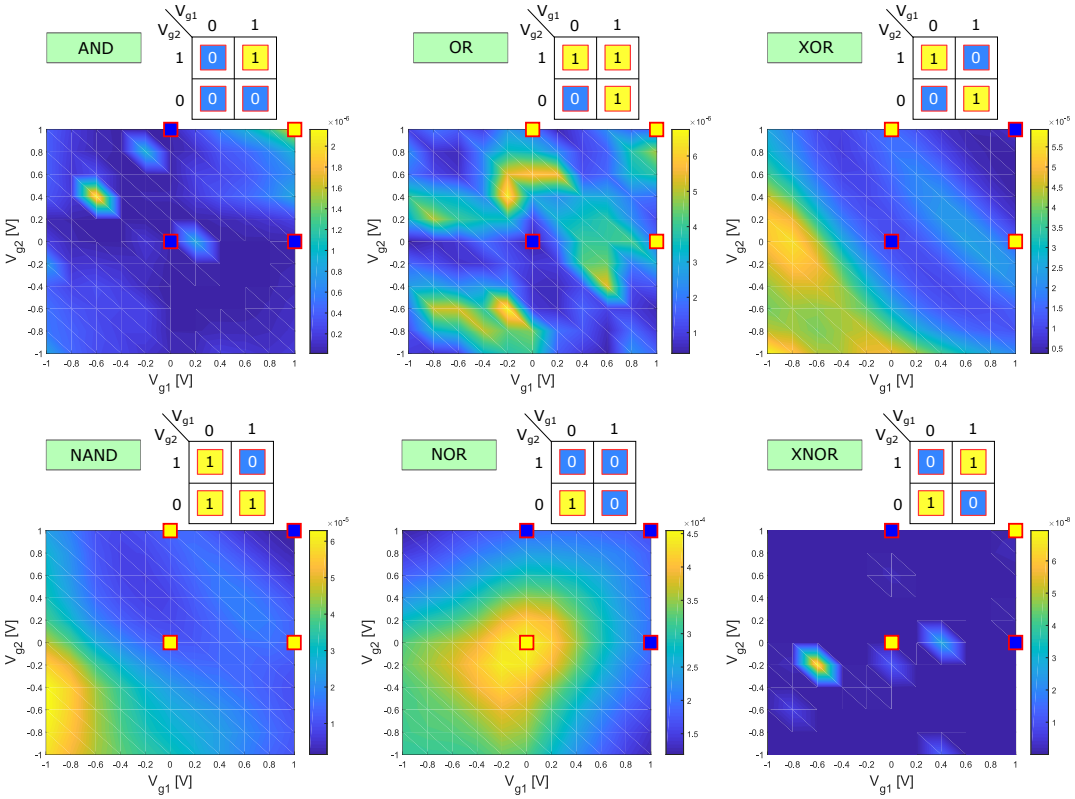

Fig. 3: Conduction maps for basic 2-input Boolean logic functions.

$\{$AND, NAND, OR, NOR, XOR, XNOR$\}$, followed by a description of the transport and performance figures, and some comments on the potential applicability of our results for Boolean logic gate implementations.

Table I summarizes the optimal butterfly GNR dimensions and back bias voltages, that resulted from the DSE, afferent to each considered Boolean logic function. All 6 butterfly GNR shapes have the same total width and similar length, but different constriction width and length. The constriction width has a big impact on the conductance (when compared to the length influence), and thus, as seen in the table, its value can significantly vary between GNRs corresponding to different Boolean functions. One can observer that, the distance between the top gate contacts is smaller for $\{$NAND, NOR, XOR$\}$, and larger for $\{$AND, OR, XNOR$\}$, while the contact width remains the same for all 6 Boolean logic functions. As for the V_{back} value, $0\,\text{V}$ or a low value ($\leq 0.4\,\text{V}$) is found to enable the most appropriate top gate control on the conductance.

The conduction maps (conductance G vs. input voltages V_{g1}, and V_{g2}) exhibited by the 6 butterfly GNR structures described in Table I, are presented in Figure 3. Emphasized as red outlined squares in each density plot, are the GNR conductance values for $(V_{\text{g1}}, V_{\text{g2}})$ equal to the 4 possible input combinations: $(0,0)$, $(0,1)$, $(1,0)$, and $(1,1)$. As color convention we used yellow for logic $''1''$ conductance and blue for logic $''0''$ conductance. For each density plot, the corresponding Karnaugh map mirrored in the conductance magnitude is also displayed. Moreover, logic $''1''$ ($''0''$) conductance values

TABLE I: Butterfly GNR Topologies.

	AND	NAND	OR	NOR	XOR	XNOR
W [a]	41	41	41	41	41	41
L [a]	$25\sqrt{3}$	$27\sqrt{3}$	$27\sqrt{3}$	$25\sqrt{3}$	$25\sqrt{3}$	$27\sqrt{3}$
W_{c} [a]	8	8	14	20	8	2
L_{c} [a]	$5\sqrt{3}$	$5\sqrt{3}$	$11\sqrt{3}$	$9\sqrt{3}$	$5\sqrt{3}$	$7\sqrt{3}$
$P_{V_{\text{g}}}$ [a]	$9\sqrt{3}$	$\sqrt{3}$	$5\sqrt{3}$	$\sqrt{3}$	$\sqrt{3}$	$9\sqrt{3}$
$W_{V_{\text{g}}}$ [a]	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$	$3\sqrt{3}$
V_{back} $[V]$	0	0.4	0	0.4	0.4	0

dispersion is under 10% for all mapped functions (e.g., 6% for XNOR), which enables robust operation.

A. Discussion

As concerns the I_{ON}/I_{OFF} ratio, it is rather modest (e.g., 38 for the AND function, 49 for the XNOR function), however this can be enhanced by doping [14], or by using per se sawtooth shaped gate contacts instead of rectangular shaped ones [15], or any other band gap engineering methods reported in the literature. We note that improving I_{ON}/I_{OFF} ratio is part of the actual gate design and is beyond the scope of this paper. The GNR shape determines the carrier confinement properties, and as a consequence, in our case, it can open an energy bandgap of e.g., up to $0.65\,\text{eV}$ for the butterfly GNR which mirrors the XNOR function. A bandgap of this magnitude was deemed sufficient to effectively switch off a manufactured device [16].

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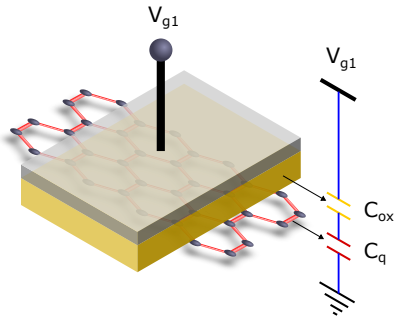

Fig. 4: Top gate capacitance.

An alternative solution could be to rely on a butterfly GNR topology which makes use of one top gate and one back gate in order to apply the two Boolean inputs. In this case, the V_{back} voltage modulates the Fermi level for the energy at the Dirac point and thus the back-gated GNR can enable a much higher $I_{\text{ON}}/I_{\text{OFF}}$ ratio ($10^4\times$ bigger ratio) when compared to the previous case with 2 top gate inputs. However, as the graphene sheet and the back gate contact are generally separated by a thick dielectric layer (e.g., $\approx$300 nm SiO_2), back-gated GNR topologies were proven to suffer from very large parasitic capacitances [17], [12], rendering them, at least in the current development state, rather impractical when compared to top-gated GNR structures.

As the butterfly GNR-based structure, graphically depicted in Figure 2, can be regarded as the main building block of a GNR-based Boolean gate, we can gain some insight - even though speculatively - into the potential discrepancy between Graphene and CMOS gates performance figures. To this end, we evaluated for the butterfly GNR mapping the XNOR function, and an XNOR gate implemented in a commercial 15 nm CMOS technology, the worst case input-to-output propagation delay, and the area footprint. The CMOS XNOR gate figures were measured in Cadence RTL Compiler [18]. For deriving the GNR propagation delay, we assumed that a 12 nm Al_2O_3 layer is utilized as insulator underneath the top gate contacts [19], and computed the delay τ_p as a function of the current I through the GNR, the input gate voltage V_{g1} (V_{g2}), and the top gate capacitance, C_{g} (depicted in Figure 4 as a function of the quantum capacitance, C_{q}, and the oxide capacitance, C_{ox}), as: $\tau_p = (C_{\text{g}} \cdot V_{\text{g1}})/I$. In order to compute the quantum capacitance, C_{q}, we followed the approach in [13], [20], and expressed it as a function of the density of states $DOS(E)$, the thermal broadening function $F_{\text{T}}(E)$, and the energy E, as :

$$C_{\text{q}} = \text{q}^2 \cdot \int_{-\infty}^{+\infty} DOS(E) \cdot F_{\text{T}}(E - (\mu_1 - \mu_2))\, \text{d}E. \quad (2)$$

Our calculations indicate 30$\times$ and 3000$\times$ smaller delay and gate active area, respectively, for the butterfly GNR structure when compared to the CMOS XNOR gate. These results suggest that, potentially speaking, GNR-based logic gates can substantially outperform advanced CMOS counterparts and constitute the foundation for future post-Si nanoelectronics.

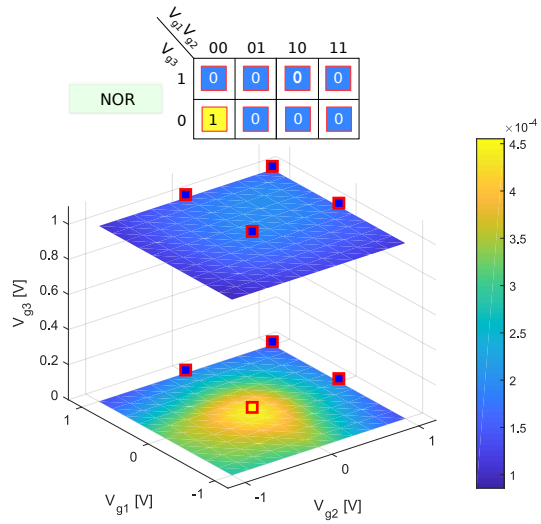

Fig. 5: 3-input NOR conduction map.

To explore the butterfly GNR structure scalability with respect to the number of inputs, we added a third top gate to build a new structure able to mirror the 3-input NOR gate functionality. The 3-input butterfly GNR structure is similar to the 2-inputs counterpart geometry-wise ($W = 41$ a, $L = 27\sqrt{3}$ a, $W_{\text{c}} = 20$ a, and $L_{\text{c}} = 13\sqrt{3}$ a, and $V_{\text{back}} = 1$ V), which demonstrates the GNR structure flexibility to easily accommodate multiple top gate inputs. The obtained conductance map is depicted in Figure 5 in a double layered manner, i.e., the top layer corresponds to $V_{\text{g3}} = 1$ V, and all possible combinations of the other two inputs $(V_{\text{g1}}, V_{\text{g2}})$, while the bottom layer corresponds to $V_{\text{g3}} = 0$ V. The 8 points on the two conductance density plot layers reflect the NOR output logic value ($''0''$ or $''1''$). The conductance values are in good agreement with the NOR functionality, which proves the ability of the butterfly GNR (or GNR in general for that matter) to reflect more complex Boolean logic functions.

IV. Conclusions

In this paper, we investigated the potential of butterfly GNRs as fundamental building blocks for the carbon-based implementation of Boolean logic gates and circuits. To this purpose, we built upon a graphene QPC, by extending it with additional top gates, as means to control and modulate its conductance according to a desired Boolean functionality. We performed a design space exploration on butterfly GNRs topology and dimensions, and obtained conduction maps which mirror 2-input Boolean functionality. Furthermore, our simulation results suggested butterfly GNR scalability vis-à-vis accommodating additional inputs and reflecting more complex Boolean logic. Even though the butterfly GNR is equivalent to a logic gate only from the behaviour point of view, our investigation provided preliminary insight into potential performance figures of future graphene-based logic gates. Our study, strongly suggests that GNRs can flexibly reflect generic Boolean logic transfer functions, and open a promising avenue towards carbon-based nanoelectronics.

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