On Effective Graphene based Computing

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***Abstract*—With CMOS feature size heading towards atomic dimensions, unjustifiable static power, reliability, and economic implications are exacerbating, prompting for research on new materials, devices, and/or computation paradigms. Within this context, Graphene Nanoribbons (GNRs), owing to graphene's excellent electronic properties, may serve as basic blocks for carbon-based nanoelectronics. In this paper, we present the two main avenues, i.e., graphene FET- and GNR- based, undertaken towards graphene based computing. The first approach is conservative and focuses on the realization of graphene FET transistor based switches as MOSFET replacements to maintain the state of the art logic Boolean algebra paradigm design methodology. The second one follows a different line of thinking and seeks GNR-based structures able to provide more complex behaviours by making better use of graphene's conduction properties. We first discuss Graphene Nanoribbon (GNR) based field Effect Transistors (GNRFETs) and Tunnelling GNR based Transistors (GNRTFETs) and their utilization as underlying elements for Boolean gate implementations. Subsequently, we present GNR-based structures that can directly compute Boolean functions, e.g., NAND, XOR, by means of one GNR only and a way to complementary arrange them in energy effective gates. To get inside into the potential of the two avenues we consider an inverter as discussion vehicle and evaluate the designs in terms of area and energy consumption. The GNR-based structure outperforms its counterparts by $15\times$ up to $104\times$ and $230\times$ smaller delay and 6 to 7 and 4 orders of magnitude smaller power than the GNRFET- and GNRTFET- based designs, respectively. Moreover, when compared with CMOS 7 nm Boolean gates GNR-based desgns exhibit up to $6\times$ smaller delay, and up to 2 orders of magnitude smaller active area, and total power consumption. Our analysis confirms that the alternative GNR-based design paradigm, which transcends the traditional switch based approach and takes better advantage of graphene intrinsicnproperties, is better suited for future carbon based nanoelectronics.**

***Index Terms*—Graphene Nanoribbons, Conduction Maps, Boolean Gates, Graphene-based Boolean Gates, Carbon-Nanoelectronics, Energy Efficiency.**

I. Introduction

In the past three decades, CMOS scaling has resulted in new technology generations every two to three years with doubled logic device density, lowered cost per operation, and increased chip performance. However, as CMOS feature size is approaching the atomic level, the faster switching speed comes at the expense of increased power density and leakage, decreased reliability and yield, increased production costs, and diminishing returns. In this landscape, and in line with the continuous impetus of device performance improvement, the development of new materials, structures, and computation paradigms are called for [1] [2]. One of the post-Si forerunners is graphene, which has enjoyed a surge of research during the past decade, paving the way for a wide range of graphene-based applications, among which electronics, spintronics, photonics and optoelectronics, sensors, energy storage and conversion, flexible electronics, and biomedical applications [3].

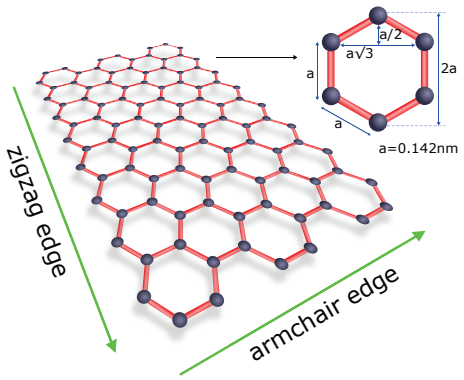

Fig. 1: Graphene Atomic Structure.

Graphene is a 2-dimensional carbon atom monolayer lattice, as illustrated in Figure 1 for 2 types of edge terminations along the transport direction: zigzag and armchair. Virtue to the edge structures, graphene can present different electronic properties (i.e., the armchair terminated graphene can exhibit both metallic and semiconducting properties depending on the nanoribbon width, while the zigzag edge-patterned graphene is always metallic), offering appealing opportunities for the development of graphene-based electronic devices. Graphene has a wealth of unique, outstanding characteristics, which provide a strong drive to investigate its usage as a potent contender to Si-based technology and as a promising means towards carbon based nanoelectronics [4], [5], [6]. Notably, graphene exhibits: (i) atomic thinness and 2D structure (which allows for the direct excitation of charge carriers, and provides unique advantages that could be compatible with scalable fabrication processes), (ii) ballistic transport, with micron long mean free path and charge Fermi velocity $\nu_F \sim 10^6$ ms^{-1}, $10\times$ higher than in Si [7], (iv) ultrahigh intrinsic carrier mobility μ both at room temperature (over 2.5×10^5 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ [8]) and at low temperature (6×10^6 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ at $4\,\mathrm{K}$ [9]), outperforming existing materials with high mobility as InP ($1.5\times10^3\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$), InAs ($1.32\times10^3\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$), or strained Si ($1.4\times10^3\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$) [10], (v) outstanding thermal properties (very high thermal conductivity $k \sim 3000$ to 5000 $\mathrm{Wm}^{-1}\mathrm{K}^{-1}$ [11]), and ability to sustain very high current densities (10^6 greater than copper [12]), and (vi) it is the strongest material ever measured, with a Young modulus

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of 1 TPa and intrinsic tensile strength of 130 GPa, being able to withstand elastic deformations of $\sim 26\%$ without fracture [13]. Apart of those very attractive properties graphene is also transparent and by its very nature biocompatible, which makes it extremely fit for medical applications, e.g., implantable prosthetics.

Generally speaking, the principal impediments to graphene-based logic are twofold: design related, and manufacturing related [7], [14], [15], [16], [17]. From the manufacturing perspective, finding a cost-effective, scalable, and reliable manufacturing process, which enables mass-production with minimum defects density and with highly reproducible features, is the main desideratum. From the design point of view, the main caveat is graphene's absence of a bandgap, which impedes charge carriers depletion, results in high "off" state static power, and limits the achievable "on"-"off" current ratios ($I_{\text{ON}}/I_{\text{OFF}} < 10$ while $I_{\text{ON}}/I_{\text{OFF}} > 10^7$ is typical for current CMOS technology nodes). For digital Boolean logic applications, there are certain aspects that graphene-based structures need to comply with, foremost: (i) ability to control conductivity and yield distinguishable "on" and "off" states, while (a) not compromising any of the graphene intrinsic highly advantageous properties (e.g., high μ), and (b) providing acceptable $I_{\text{ON}}/I_{\text{OFF}}$ ratio (in the range 10^4 to 10^7), (ii) finding the proper external electrical means (e.g., top gates, back gates) to control graphene behaviour and induce the desired logic functionality, (iii) ability to encode some desired logic transfer function onto the graphene electrical characteristics, and (iv) ensuring the conditions for digital circuits cascading (i.e., clean and compatible/matching electric levels, e.g., voltage, current, for the circuit inputs and outputs).

In this paper, we present the main approaches undertaken to comply with the aforementioned computing tenets and the approaches that pervade them for beyond CMOS computation. We first focus on device level efforts towards the realization of graphene based switches and by implication of graphene based logic circuits. The idea behind this approach is to maintain the state of the art logic design methodology, which constructs on the Boolean algebra paradigm, and just replace the MOS switches (transistors) with graphene based counterparts. To this end we describe Graphene Nanoribbon (GNR) based field Effect Transistors (FETs) and their underlying operation principle [18] and tunnelling GNR based FETs [19]. To put things into prospective we also summarize the potential performance of Boolean gates based on such graphene switches as reported in [20] and [21].

Subsequently, we follow a different line of thinking inspired by our previous investigation in [22], which provides strong evidence that GNRs can exhibit functionalities beyond the traditional switch. Thus, to take advantage of the full graphene potential, one can depart from the traditional switch based computation and envision novel GNR-based structures and computing avenues. In this regard, we present structures that can directly compute Boolean functions, e.g., NAND, XOR, by means of one GNR only and a way to arrange such structures instead of transistors in energy effective gates. Considering an inverter gate, the GNR-based structure outperforms the transistor-based ones as follows: its propagation delay is from $15\times$ up to $104\times$ and $230\times$ smaller and its total energy consumption is 6 to 7 and 4 orders of magnitude smaller than the one of GNRFET- and GNRTFET- based designs, respectively.

Finally, we briefly present some other graphene based structures which exploit some advantageous properties, such as weak intrinsic spin-orbit coupling and absence of hyperfine interactions, negative differential resistance, and ambipolar transport, in the context of spintronics, multiple valued logic, and in-field controllable dynamic and static logic.

This study suggests that: (i) bandgap opening is not an issue and can be energy effective dealt with by topological measures, in synergy with chemical and electrostatic, (ii) the alternative GNR-based design paradigm which transcends the traditional switch based approach takes better advantage of intrinsic graphene properties and outperform GFET based gate deigns in terms of area, delay, and energy consumption, and (iii) GNR-based Boolean gates can potentially outperform state of the art CMOS 7 nm counterparts by up to $6\times$ smaller delay, and up to 2 orders of magnitude smaller active area, and total power consumption.

The remaining of the paper is structured as follows: Section II presents an overview of graphene-based transistors. Specifically, FETs are discussed in Section II-A, and Tunnelling FETs, with both planar and out-of-plane tunnelling, are addressed in Section II-B. In Section III, we provide a brief encounter with GNR-based structures, which do not rely on the traditional switching mechanism as operation principle. Section IV concludes the paper with an outlook and opportunities for graphene-based computing.

II. Graphene Transistor-based Computing

According to ITRS, one of the requisites to continue devices scaling along the "More Moore" strategy, is the implementation of transistors that make use of high mobility channel materials [23]. In view of this, graphene comes as a natural channel material choice as its extremely high carrier mobility is surpassing by far currently utilized materials (e.g., Ge for pMOS transistors and III-V compound semiconductors - SiGe, InGaAs - for nMOS transistors). However, while a non-zero energy bandgap is not necessary for high speed analog circuits, for proper operation of digital logic it is a key property. Up to date, several approaches have been undertaken to induce a bandgap in graphene, noteworthy: (i) lateral confinement of a large sheet of graphene charge carriers in the form of narrow strips of graphene called Graphene Nanoribbons (GNRs), or in the form of Graphene Quantum Dots (GQDs), (ii) breaking the planar symmetry of the graphene crystal structure via chemical and/or structural modifications (e.g., substrate use, substitutional doping, chemical functionalization, straining), and (iii) applying a transverse electrical field to bilayer graphene [3]. For graphene-based transistors usage, a GNR quantum confinement and substrate induced bandgap opening approach is typically relied upon.

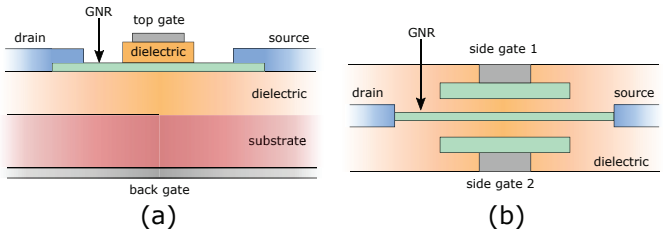


Fig. 2: GNRFET cross-section schematics: (a) GNRFET with top and/or back gate; and (b) FEBM GNRFET.

Subsequently, we present graphene devices (transistors) meant to enable the road towards traditional switch-based logic design approaches.

A. GNR-based FETs

In GNRFET structures, as illustrated in Figure 2 (a), graphene serves as conduction channel, through which a current flow is induced by applying a bias voltage between the two graphene nanoribbon end-point contacts (source and drain). The top gate voltage, as local perturbation potentials, modulate the source-to-drain current, while the back gate shifts the Fermi level chemical potential away from the Dirac point, into the electron or hole conduction regime. Most past efforts typically employ a Si conducting substrate as back-gate and a thick layer of SiO_2 ($\sim$ 300 nm) as top gate dielectric. Recently, high-k dielectric materials (e.g., HfO_2, Al_2O_3) that reduce leakage gate tunneling currents are being increasingly utilized [24]. As for the source and drain electrodes, depending on wether they are metallic or semiconducting, two varieties of GNRFETs exist: Schottky Barrier (SB) type and Metal-Oxide-Semiconductor (MOS) type. For SB-GNRFETs, the source and drain contacts are metallic, resulting in formation of Schottky barriers at the metal-graphene junctions. MOS-GNRFETs on the other hand, have the source and drain contacts made of heavily doped graphene. While for MOS-GNRFETs the current flow is determined either by electrons or holes, depending on the dopant type of source/drain reservoirs, SB-GNRFETs exhibit ambipolar current conduction, which is not appropriate for CMOS-style logic.

While ambipolar devices-based logic designs have been investigated [25] such an approach is not particularly of interest as to obtain NMOS or PMOS transfer characteristics, SB-GNRFETs require extra work function engineering, which can result in unbalanced n-type and p-type characteristics, leading to robustness and performance loss. On the other hand MOS-GNRFETs exhibit a higher I_{ON}/I_{OFF} ratio and larger transconductance and cut-off frequency, however they are susceptible to doping variation (as it is difficult to control the exact doping level of source/drain reservoirs with several thousands atoms), and need to consider minimizing the ohmic contacts to graphene [26]. In practice the GNRFET channel usually consists of a dense array of parallel rectangularly shaped and equally spaced GNRs in order to increase the its drive strength.

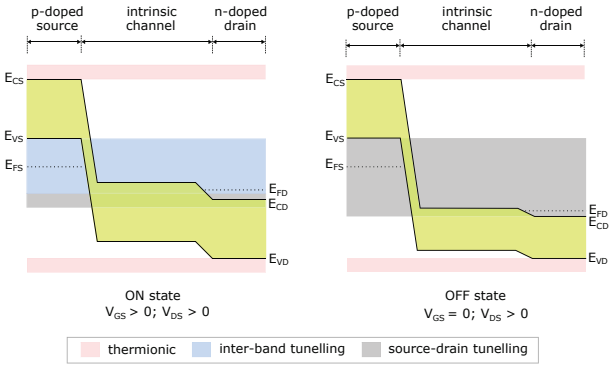


Fig. 3: GNRTFET Band Diagram.

Table I summarizes the power consumption and propagation delay figures reported in [20] for a set of Boolean gates constructed with SB-GNRFETs and MOS-GNRFETs ($V_{DD} = 0.5$ V), comparatively to Si-based CMOSFETs using HP 16 nm CMOS technology, with nominal $V_{DD} = 0.7$ V. These results indicate that relative to Si-based MOSFETs, SB-GNRFETs are better suited for high speed applications, while MOS-GNRFETs are more appropriate for low power applications.

To improve the GNRFET performance, several device architectures have been explored. One such structure is the GNR transistor with Field Effect Bandgap Modulation (FEBM) [27]. The rationale is to use the intrinsic bandgap for the "off" state, and a narrower bandgap enabled by the electrical field from two side gates - as illustrated in Figure 2 (b) - for the "on" state. Another structure that reduces the parasitic drain contact tunnelling current, and the "off" state current, uses an SB-GNRFET with an asymmetric top gate, which is situated closer to the source contact [28].

B. GNR-based Tunelling FETs

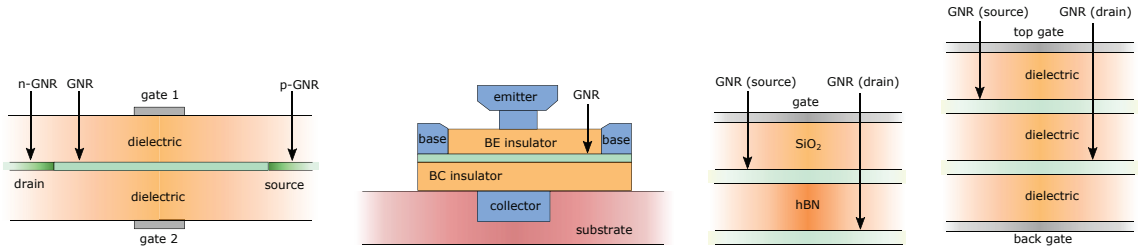
Other structures which have been recently investigated for their promising perspective in digital electronics, are GNR-based Tunnelling FETs (TFETs). Regular TFETs have either a single or double gate geometry (similarly to the GNRFET structure), and doped source and drain (via either chemical or electrostatic doping). Figure 3 illustrates a typical p-type GNRTFET energy band structure, noting that while for GNRFETs the transport is governed by both a thermionic emission current and a tunnelling current, for GNR-based TFETs the thermionic current component is negligible. The gate voltage shifts the energy bands, and has a big impact on the carriers tunnelling probabilities. Compared to GNRFETs, GNRTFETs benefit of superior gate control and higher I_{ON} current, and thus seems to be more attractive then GNRFETs for graphene-based computing. To get inside in GNRTFETs potential performance we present in Table II the evaluation results reported in [21] for a low-power inverter constructed with double-gated GNRTFETs with GNR channel widths of 10a, 13a, and 16a. One can observe in the Table that the GNRTFET avenue enables 8 to 9 orders of magnitude reduction of the static power when compared to the GNRFET counterpart.

TABLE I: GNRFET-based Gates Propagation Delay and Power Consumption vs. CMOS 16 nm [20]

	Delay $[ps]$			Dynamic Power $[W]$			Leakage Power $[W]$		
	SB-GNRFET	MOS-GNRFET	CMOS	SB-GNRFET	MOS-GNRFET	CMOS	SB-GNRFET	MOS-GNRFET	CMOS
INV	4	28	15	$1.87 \cdot 10^{-5}$	$1.58 \cdot 10^{-6}$	$7.81 \cdot 10^{-6}$	$1.48 \cdot 10^{-6}$	$6.32 \cdot 10^{-11}$	$1.16 \cdot 10^{-8}$
NAND2	4	29	17	$5.83 \cdot 10^{-5}$	$1.13 \cdot 10^{-6}$	$6.85 \cdot 10^{-6}$	$1.89 \cdot 10^{-6}$	$1.11 \cdot 10^{-10}$	$1.35 \cdot 10^{-8}$
NOR2	4	29	22	$2.63 \cdot 10^{-5}$	$1.00 \cdot 10^{-6}$	$3.79 \cdot 10^{-6}$	$1.89 \cdot 10^{-6}$	$1.09 \cdot 10^{-10}$	$1.40 \cdot 10^{-8}$
XOR2	5	46	32	$4.10 \cdot 10^{-5}$	$1.22 \cdot 10^{-6}$	$9.47 \cdot 10^{-6}$	$8.84 \cdot 10^{-6}$	$4.87 \cdot 10^{-10}$	$7.09 \cdot 10^{-8}$

TABLE II: GNRTFET-based Inverter Propagation Delay, Static Power Consumption, and Energy [21].

	Delay $[ps]$			Static Power $[W]$			Dynamic Energy $[J]$		
pTFET \ nTFET	10	13	16	10	13	16	10	13	16
10	$1.96 \cdot 10^{4}$	$1.11 \cdot 10^{4}$	$1.35 \cdot 10^{4}$	$1.49 \cdot 10^{-19}$	$7.39 \cdot 10^{-19}$	$4.93 \cdot 10^{-11}$	$2.14 \cdot 10^{-17}$	$2.52 \cdot 10^{-17}$	$2.96 \cdot 10^{-17}$
13	$1.11 \cdot 10^{4}$	$2.16 \cdot 10^{2}$	$1.41 \cdot 10^{2}$	$7.39 \cdot 10^{-19}$	$1.29 \cdot 10^{-18}$	$6.01 \cdot 10^{-11}$	$2.52 \cdot 10^{-17}$	$2.90 \cdot 10^{-17}$	$3.20 \cdot 10^{-17}$
16	$1.35 \cdot 10^{4}$	$1.41 \cdot 10^{2}$	$6.24 \cdot 10^{1}$	$4.93 \cdot 10^{-11}$	$6.01 \cdot 10^{-11}$	$1.20 \cdot 10^{-10}$	$2.96 \cdot 10^{-17}$	$3.20 \cdot 10^{-17}$	$3.65 \cdot 10^{-17}$



(a) (b) (c) (d)

Fig. 4: GNRTFET cross-section schematics: (a) RTT; (b) GBT; (c) VTGNRFET; and (d) SymFET.

Vertical graphene-based structures (e.g., vertical tunnelling transistors, vertical Hot Electron Transistors (HET)), have been also proposed, which besides implications at the electronic transport level, enable integrated architectures with stacks of multiple transistors connected in series. Graphene Base Transistors (GBTs), as illustrated in Figure 4 (b), have a vertical structure composed of emitter, base, and collector just like a HET, with the base electrode made of graphene also [29] [30]. In the ON state, the emitter-base diode injects hot electrons which tunnel from emitter to collector. Operation in the THz frequency range and high current ratios are estimated to be obtained with GBTs.

A logical follow-up investigation of the tunnelling transistors refers to the Resonant Tunneling Transistors (RTT) [31]. Illustrated in Figure 4 (a), is a typical RTT structure, which enables barrier height modulation, and allows for resonant tunneling of the carriers. As RTTs can have several switching states (as a result of the negative differential resistance), they can also be potentially utilized for multiple valued logic.

For the previous transistor structures, the carrier transport was in the same plane as the graphene sheet. Changing the devices geometry, such that the tunnelling occurs between GNR layers (carrier transport vertical to the GNR), can significantly increase the current. VTGRGETs, structurally illustrated in Figure 4 (c), are vertical tunnelling heterogeneous structures, which rely on effective voltage induced modulation of the GNR density of states and of the tunnel barrier height. Between the GNR made source and drain contacts a few layers (e.g., 3 to 7) of hexagonal boron nitride (hBN) [32], or molybdenum disulfide (MoS_2) [33] serve as tunnelling barrier. Tungsten disulfide (WS_2) can also be used as tunnelling barrier material, allowing one to switch between thermionic and tunnelling transport [34] and further increase the "on" current and by implication the I_{ON}/I_{OFF} current ratio.

Another vertical structure is the interlayer tunnelling transistor, SymFET [35], illustrated in Figure 4 (d). It has 2 layers of GNRs between which resonant tunnelling behaviour occurs, the resonant current peak being modulated by the applied gate bias and by the GNR chemical doping. The two GNR layers, are separated by a dielectric and flanked by a top and a bottom gate. An advantage of this structure is the current insensitivity to temperature.

While the previously introduced devices have different topologies, operation mechanisms, fabrication complexity, and performance they all target the realization of graphene based switches able to replace MOSFETs in the implementation of

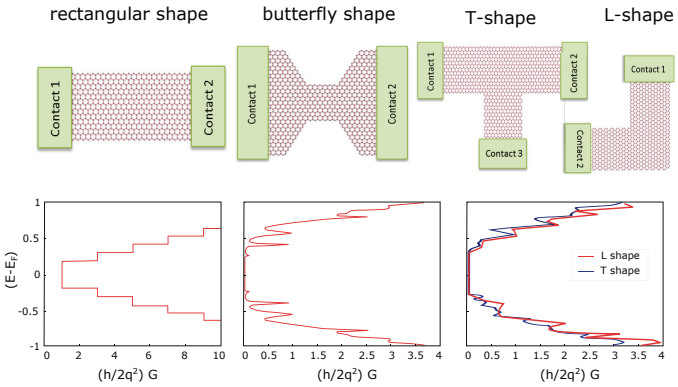


Fig. 5: Energy Bandgap vs GNR Geometry.

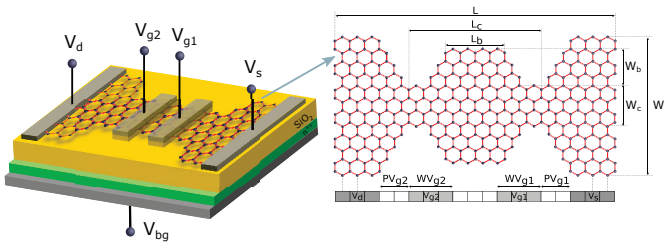


Fig. 6: Boolean Function Mirroring GNR-based Structure [22].

Boolean based graphene gates and circuits. In the next section we leave the traditional design avenue and investigate GNR potential to exhibit a more complex than switch behaviour and allow for the effective construction of basic blocks that my also go beyond traditional Boolean gates.

III. Graphene Nanoribbon-based Computing

In terms of novel devices and architectures, graphene's unique properties may enable operation modes which are fundamentally different than the traditional switching mechanism.

As mentioned in Section I, one of the main impediments of using graphene in logic design, is its lack of an energy bandgap. However, through GNR shape carving this problem can be overcome to some extent. In Figure 5, we exemplify 3 GNR shapes, which are subjected to a bias voltage via the 2 or 3 end-point contacts. The GNRs' associated conductance as a function of energy is depicted in the lower half of the figure. One can observe that for the standard rectangular shape the GNR is always conducting, while by carving the GNR geometry (e.g., into a butterfly shape, L-shape, or T-shape), a bandgap of approximately 0.5 eV can be induced, and the GNR conductance can be effectively switched off. GNR geometry shaping, together with the proper electrical external control means in order to modulate it conductance according to some desired logic function, provide the premises for a different perspective for logic design that is not based on transistors as basic building blocks. Specifically, the GNR can be patterned and biased in such a way that it can directly map a desired Boolean function onto its electrical characteristics [22]. Figure 6 presents such a GNR-based device architecture.

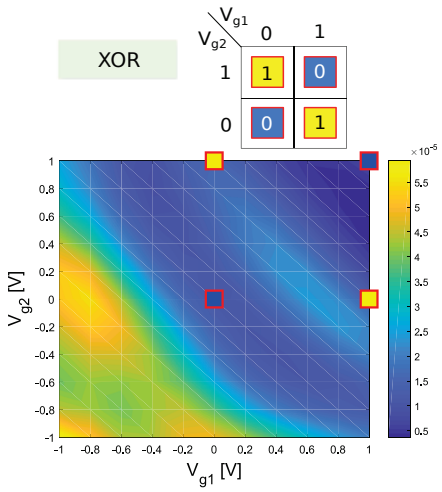


Fig. 7: 2-input XOR Gate Conductance Map.

The GNR-based basic building block is endowed with top gates, which modulate the current flow - through the GNR - induced by applying a bias voltage applied between the source and drain end point contacts. Underneath the graphene ribbon, there is a dielectric layer, the substrate, and a back gate. Different from GRNFETs, where the GNRs are rectangularly shaped, for this structure, a trapezoidal structure with zig-zag edges is utilized. To obtain a certain, e.g., Boolean gate, behaviour GNR's geometry is shaped and the top gate contacts topology (distance between gate contacts and position relative to source/drain contacts) varied, until a conduction map which reflects the desired Boolean functionality is obtained. The Boolean function inputs are applied by means of top gate input voltages. For example, Figure 7 depicts the GNR structure conductance map (i.e., conductance G vs. top gate input controlling voltages, V_{g1} and V_{g1}), obtained for a GNR whose geometry was optimized such that it reflects the Boolean XOR operator functionality, for logic high and low voltage levels associated with 1 V and 0 V, respectively. The blue squares encode the XOR output logic "0", while the yellow squares represent the XOR output logic "1", in line with the afferent Karnaugh map. A similar procedure can be followed to obtain a GNR structure whose conductance maps a multi-input Boolean function, i.e., 3-input Boolean XOR, which is illustrated in Figure 8. An advantageous point for the aforementioned GNR structures, is that the voltage levels chosen for "0" logic and "1" logic, are not restrictive and the device can still properly operate when they are reduced into the order of hundreds or even tens of mV. In principle, every GNR structure which mirrors a certain Boolean function onto its conductance map, has its own V_{DD} limitation, which is highly dependent on the GNR geometry and contacts topology. As an example, it was found that 0.02 V is the lowest V_{DD} voltage value for which can still be obtained butterfly GNR structures able to mirror AND functionality, and which have an $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ current ratio big enough to allow differentiation between logic low and logic high voltage levels [36].

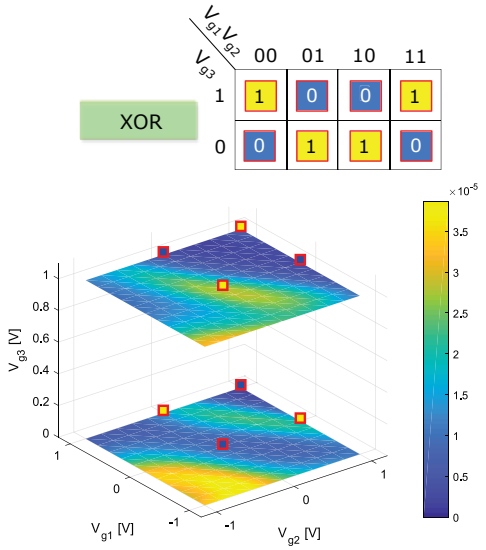


Fig. 8: 3-input XOR Gate Conductance Map.

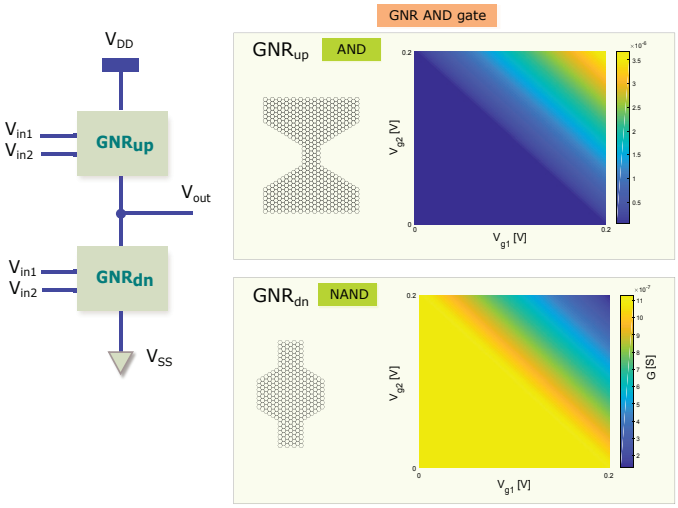


Fig. 9: GNR Boolean Gate [37].

In [37], the authors propose graphene-based Boolean gates, by arranging two such GNR structures as follows: a pull-up GNR structure, which has its drain terminal connected to V_{DD}, and a pull-down GNR, which has its source terminal connected to V_{SS}. The two GNR structures perform complementary functions: for instance for a graphene-based AND gate, the pull-up GNR mirrors the AND logic functionality onto it conductance, and the pull-down GNR maps the NAND Boolean functionality onto its conductance, as illustrated in Figure 9. For obtaining the GNR structures, which compose each GNR-based Boolean gate, the authors performed a design space exploration with respect to GNR's geometry and contacts topology. Figure 9 exemplifies an AND gate GNR structure and its conductance maps obtained as a result of the design space exploration. In Table III we summarize the propagation delay, active area (under the gate), and total power consumption reported in [37] for GNR-based gates operating at $V_{DD} = 0.2$ V and for CMOS 7 nm

TABLE III: GNR-based Gate Propagation Delay, Area, and Power Consumption vs. CMOS 7 nm [37]

	Delay $[ps]$		Active Area $[nm^2]$		Total Power $[W]$	
	GNR	CMOS	GNR	CMOS	GNR	CMOS
AND	1.38	9.618	$4.272 \cdot 10^1$	$1.452 \cdot 10^3$	$4.628 \cdot 10^{-9}$	$5.886 \cdot 10^{-7}$
NAND	2.15	7.556	$4.146 \cdot 10^1$	$9.680 \cdot 10^2$	$2.370 \cdot 10^{-9}$	$5.415 \cdot 10^{-7}$
XOR	7.48	9.168	$4.038 \cdot 10^1$	$2.420 \cdot 10^3$	$1.734 \cdot 10^{-9}$	$5.923 \cdot 10^{-7}$
BUFF	0.42	2.040	$3.283 \cdot 10^1$	$9.680 \cdot 10^2$	$0.937 \cdot 10^{-9}$	$4.704 \cdot 10^{-7}$
INV	0.27	1.110	$5.431 \cdot 10^1$	$4.840 \cdot 10^2$	$0.947 \cdot 10^{-9}$	$4.621 \cdot 10^{-7}$

($V_{DD} = 0.7$ V) counterparts. The Table indicates that the GNR-based approach substantially outperforms CMOS by up to $6\times$ smaller delay, and up to 2 orders of magnitude smaller active area, and total power consumption.

While a through comparison among graphene FET- and GNR- based logic gate implementations is not straight forward and also out the scope of this paper it is of interest to get a feeling about their potential and relative ranking. Let us consider as discussion vehicle the inverter, as cost and performance data have been reported for all its implementations, i.e., MOS-GNRFET, GNRTFET, and GNR-based, in Table I, Table II, and Table III, respectively. One can observe that the GNR-based inverter substantially outperforms its peers in terms of propagation delay, which is $15\times$, $104\times$, and $230\times$ smaller than the one of SB-GNRFET, MOS-GNRFET, and GNRTFET counterparts, respectively. Moreover, its power consumption is 4 and 3 orders of magnitude smaller than the one of SB-GNRFET and MOS-GNRFET, respectively. The GNRTFET inverter was specifically designed for extreme low power, thus at the expense of a very poor delay, its static power consumption is by 13 and 8 orders of magnitude smaller than the one of SB-GNRFET and MOS-GNRFET inverters, respectively. While no static power figures are available for the GNR-based inverter the 4 designs can be compared in terms of energy consumption, which is in the order of 10^{-17} J, 10^{-17} J, 10^{-17} J, and 10^{-21} J for the SB-GNRFET, MOS-GNRFET, GNRTFET, and GNR-based inverter, respectively. The area footprint is expected to be lower for the GNR-based gates as they comprise only two complementary GNR structures instead of several transistors.

These results clearly suggest that both the transistor-based and the GNR-based structures have the potential to outperform CMOS counterparts, with the GNR-based design style being the most promising one in terms of energy consumption.

By following the same avenue but a different line of reasoning in [38] the authors propose another GNR-based Boolean gate structure, arranged in a diapason like structure with 2 arms and 3 arms for 1-input and 2-input gates, respectively, as illustrated in Figure 10 for the particular case of a 2-input OR gate. The basic building block structure is this case is the L shaped GNR, which has a zig-zag side and an armchair side, which can give rise to an energy bandgap. The authors use -0.5 V for "0" logic, and 0.5 V for "1" logic. All 2-input

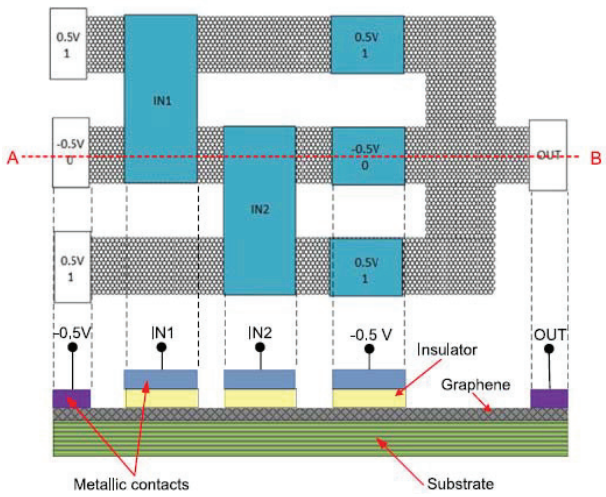


Fig. 10: Diapason GNR OR Gate [38].

gates (exemplified AND and OR) have an identical structure with 5 top gates and 4 electrodes, the only difference between the gates being the fixed applied bias voltages for 3 of the top gates, and for the left 3 electrodes, whose values can be either V_{DD} or V_{SS}. While being less effective in terms of delay and power the the gates introduced in [37] this GNR-based structure has some advantages which benefits fabrication, e.g., regularity and lack of a back gate, which can be proved useful for graphene-based biocompatible applications.

To conclude this section we would like to briefly highlight other computation approaches that can potentially benefit of graphene intrinsic properties. For instance, as graphene exhibits a negative differential resistance (peak-valley shaped I-V characteristic), one can envision graphene's potential for multi-valued non-binary logic [39]. For instance, in [40], the authors propose a one-digit radix-4 adder, composed of 2 GNRs, which exploits the quantized conductance and also uses the back gate as adder input. Graphene exhibits ambipolar transport, characterized by a superposition of electron and hole currents [41]. Thus, instead of suppressing this behavior as in the case of GNRFETs, one can also control it via an additional polarity top gate, with applications to in-field controllable dynamic logic, as well as static logic [42].

Besides electric charge, the fundamental electron property that was exploited for logic circuits, the electron spin and its associated magnetic moment can be used to control electrical conduction and create novel computing functionalities. Graphene's properties (e.g., negligible intrinsic spin-orbit coupling, absence of hyperfine interactions, long spin diffusion lengths) makes graphene an ideal candidate for spintronic devices expected to be faster, and to enable extremely low-power computing [43]. As an electron spin is inherently a quantum system that is in a superposition of states, it can serve as qubit for quantum information processing. To this end, graphene quantum dots have been proposed, as a host for spin qubits [44], as graphene holds the potential for long coherence time, as well as fast operating time.

IV. Conclusions

In this paper, we presented a comprehensive overview of state of the graphene-based computing. We have been interested in evaluating the potential impact graphene devices may have on circuit performance but also on circuit design style and underlying computation paradigm, thus we framed the discussion solely from a circuit design standpoint, without diving into any manufacturing and computer architecture related implications. We presented the mainstream switch-alike GNR-based transistors, namely GNRFETs and GNRTFETs, followed by other transistor structures that improve their performance via a better modulation and control of the electronic transport. Then we focused on beyond switch based approaches and discussed GNR-based devices able to directly compute a Boolean function and on Boolean gates built with 2 such GNR structures with complementary behaviour. Both transistors- and GNR-based gate structures have been evaluated and compared with CMOS counterparts, in terms of area, delay, power consumption, and energy, to asses the potential viability of carbon based computation platforms. Simulation results indicated that the GNR-based inverter substantially outperforms its graphene based counter-candidates in terms of delay and energy consumption. Moreover, when compared with CMOS 7 nm Boolean gates GNR-based implementations exhibit a 6× smaller propagation delay and a 2 orders of magnitude smaller total power consumption. Our analysis clearly indicated that graphene has great potential for the realization of beyond CMOS energy effective nanoscale circuits and that approaches that deviate from the traditional switch based design, in an attempt to take advantage of graphene's properties, are more successful and can catalyse the development of alternative computation avenues.

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