

Non-Equilibrium Green Function-based Verilog-A Graphene Nanoribbon Model

Y. Jiang, N. Cucu Laurenciu, S.D. Cotofana
Computer Engineering Laboratory,
Delft University of Technology, The Netherlands.
{Yande.Jiang, N.CucuLaurenciu, S.D.Cotofana}@tudelft.nl

Abstract—Graphene, due to its wealth of remarkable electronic properties, emerged as a potent post-Si forerunner for nanoelectronics. To enable the exploration and evaluation of potential graphene-based circuit designs, we propose a fast and accurate Verilog-A physics-based model of a 5-terminal trapezoidal Quantum Point Contact (QPC) Graphene Nano-Ribbon (GNR) structure with parametrizable geometry. The proposed model computes the GNR conductance based on the Non-Equilibrium Green's Function (NEGF)-Landauer formalism, via a Simulink model called from within the Verilog-A model. Furthermore, model accuracy and versatility are demonstrated by means of Simulink assisted Cadence Spectre simulation of a simple test case GNR-based circuit and a GNR-based 2-input XOR gate.

Index Terms—Graphene, GNR, Verilog-A, Spice Model, NEGF, Carbon-Nanoelectronics.

I. INTRODUCTION

As CMOS scaling approaches atomic dimensions, unjustifiable static power, decreased reliability and yield, and increased IC production costs are aggravating [1], prompting for research and development towards new materials, devices, structures, and computation paradigms. One of the potent contender to Si-based nanoelectronics is graphene [2], [3] due to its unique properties, e.g., flexibility, biocompatibility, ultimate thinness, high thermal conductivity, thermal stability, mechanical strength, optically transparent and so on [4]. Graphene, as one of the post-Si forerunners, has enjoyed the research surge during the past decade, paving the road for graphene-based applications, e.g., flexible electronics, biological engineering, optical electronics, ultrafiltration, composite materials, ultra-sensitive sensors, energy storage and conversion, and spintronics.

Graphene is a 2-dimension, carbon atom honeycomb monolayer lattice with a lot of remarkable electronic properties, such as high electron mobility ($10\times$ larger than Si), low effective electron masses, high current density, as well as ballistic carrier transport with long carrier mean-free paths [5]. These unique properties provide a strong drive to investigate graphene's potential as a replacement of Si, and open a promising avenue for carbon-based nanoelectronics. Since fabrication technology of graphene-based logic and circuits is still in an early stage, modeling and simulation has been playing an important role for providing a physical insight into futuristic graphene-based circuits, and a proper evaluation on its potential performance. Numerical simulations for Graphene Nano-Ribbon Field-Effect Transistors (GNRFETs), based on non-equilibrium Green's function (NEGF) formalism have

been published [6], which are accurate, but are too complex. Another simulator for GNRFETs tries to take the advantage of a look-up-table to speed up the simulation process, but with the design parameters increase and change, the simulator needs to rebuild the model, such that its complexity increases [7]. Analytical models that simulate Schottky-Barrier-Type graphene nanoribbon field-effect transistor (SB-GNRFETs) and graphene nanoribbon tunnel field effect transistors (GNR-TFETs) are published in [8], [9], respectively. The simulator presented in [10], [11] provide a SPICE-compatible model for GNRFETs simulation, also enabling circuit-level delay and power analysis under process variation.

In order to bring Graphene Nano-Ribbon specific phenomena from the physics to the circuit-level, to allow for graphene-based circuit design and optimizations, a fast and parameterized model that enables electrical simulation is required. However, since GNRs behavior and potential benefit in the circuit context are not fully comprehended, such a model should preserve the physical simulation accuracy degree. To this end, in this paper we focus on the graphene nanoribbon simulation and introduce a Verilog-A SPICE-compatible generic model based on NEGF formalism, which builds upon an accurate physics formalization, by computing GNR specific variables, e.g., conductance, via internally called Simulink code. In this way, the proposed GNR model symbiotically exploits accurate (in perfect agreement with physics results) Simulink results and optimized SPICE circuit solvers (e.g., Spectre, HSPICE). As discussion vehicle, we consider a 5-terminal trapezoidal Quantum Point Contact (QPC) GNR topology, whose conductance map can mirror basic Boolean functions [12], and develop a generic 8-parameter Verilog-A model able to capture the behavior of any QPC topology instance. To illustrate the proposed model applicability, we consider a simple test case circuit and the GNR-based 2-input XOR gate introduced in [13], and simulate the afferent I - V characteristic, via Cadence Spectre and Matlab Simulink. The simulation results indicate that our proposed physics-based Verilog-A GNR model is accurate and enables the proper evaluation of graphene-based circuits potential performance.

The remaining of this paper is structured as follows: Section II entails an overview of the physics-based Verilog-A GNR model. Section III presents the simulation results and comments on the practical applicability of our proposed Verilog-A GNR model. Finally, some concluding remarks are given in Section IV.

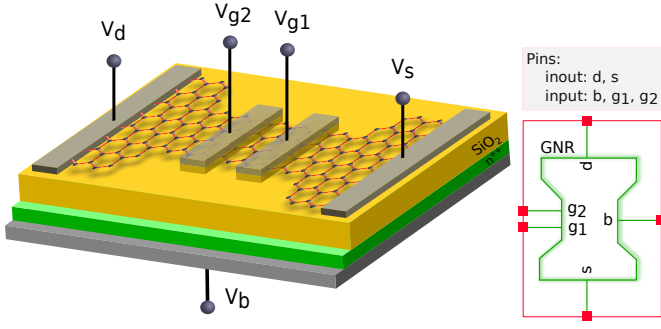


Fig. 1: Trapezoidal QPC Topology and Associated SPICE Symbol.

II. VERILOG-A GNR MODEL

In this section, we present the GNR model SPICE interface and its parameters, and describe the mathematical formalism underlying the GNR behavior. Further, in Section II-C, we outline the simulation flow for a transient nodal analysis.

A. GNR model specification

The proposed Verilog-A model captures the behavior of a generic trapezoidal QPC (with zig-zag atomic edge alignment) structure [14], as depicted in Fig. 1, in which we make use of the GNR as a conduction channel. In this structure, the current flow is induced by applying a bias voltage $V_d - V_s$ between the two end-point contacts above the graphene sheet and is further modulated by the input voltages V_{g1} , V_{g2} , which are applied via the two top gates contacts. On the back of GNR, we apply a back-bias potential V_{back} , which in manufactured devices, usually, is a small fraction of the back gate voltage, i.e., V_b , (because of the significant potential drop on the dielectric layer, e.g., SiO_2 , residing underneath the GNR sheet). Consequently, the Verilog-A model has 5 pins and 8 parameters (presented in Fig. 2) capturing: (i) the nanoribbon geometry, i.e., width W , length L , constriction width W_c , and constriction length L_c and (ii) the top gates topology, i.e., position PV_{g1} , PV_{g2} (the distance between the two top gate contacts and the source/drain contacts, respectively) and width WV_{g1} , WV_{g2} (the top gate contacts width). We note that all values are expressed in terms of a (0.142 nm), the distance between two graphene lattice adjacent carbon atoms. In this way, the model is generic and can accommodate a wide range of GNR shapes and topologies.

B. GNR model formalism

For modelling the GNR electronic transport, we employ the Non-Equilibrium Green Function quantum transport model, the semi-empirical Tight Binding (TB) computations to obtain the system Hamiltonian, and the Landauer-Buttiker formalism to derive the GNR current and conductance [15], [16].

In particular, we derive the conductance for the graphene-based structure with respect to the 2-input top gate voltages, as depicted in Fig. 1, where the GNR channel is described by a Hamiltonian matrix H , which incorporates all internal and

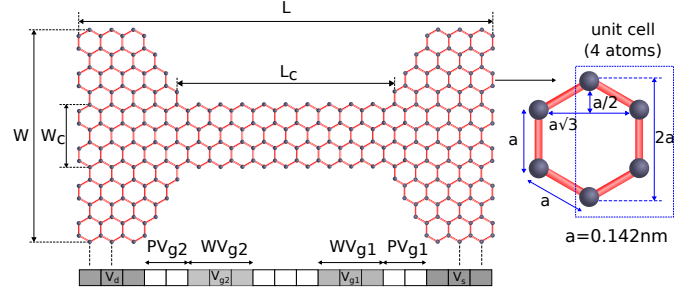


Fig. 2: GNR Geometry and Parameters: W , L , W_c , L_c , $PV_{g1, g2}$, $WV_{g1, g2}$.

external potentials (e.g., top gate voltages and back gate voltage). H is constructed using semi-empirical TB computations, as:

$$H = \sum_{i,j} t_{i,j} |i\rangle \langle j|, \quad (1)$$

$$\text{where } t_{i,j} = \begin{cases} 0, & \text{if atoms } i \text{ and } j \text{ are not adjacent} \\ \tau, & \text{otherwise,} \end{cases} \quad (2)$$

and in our simulation we set $\tau = -2.7$ eV. On the channel end sides, the drain and source contacts with different electrochemical potentials sustain the channel conduction. In addition, the contact channel interactions are modelled via the contact self-energy matrices Σ_1 and Σ_2 , respectively. After H and $\Sigma_{1,2}$ are derived, the transmission function $T(E)$, which models the probability of one electron being transmitted between the source and the drain contacts, is computed as a function of energy as:

$$T(E) = \text{Trace} \left[\Gamma_1 G_R \Gamma_2 G_R^\dagger \right] \quad (3)$$

where

$$G_R(E) = [EI - H - \Sigma_1 - \Sigma_2]^{-1}, \quad (4)$$

$$\Gamma_{1,2} = i[\Sigma_{1,2} - \Sigma_{1,2}^\dagger]. \quad (5)$$

The channel current is then derived based on Landauer formula, as:

$$I = \frac{q}{h} \int_{-\infty}^{+\infty} T(E) \cdot (f_0(E - \mu_1) - f_0(E - \mu_2)) dE, \quad (6)$$

where $f_0(E)$ denotes the Fermi-Dirac distribution function at temperature T , and $\mu_{1,2}$ represent the source and drain contacts Fermi energy. Finally, the conductance, when the GNR is exposed to the bias voltage $V = V_d - V_s$, writes as:

$$G = \frac{I}{V_d - V_s}. \quad (7)$$

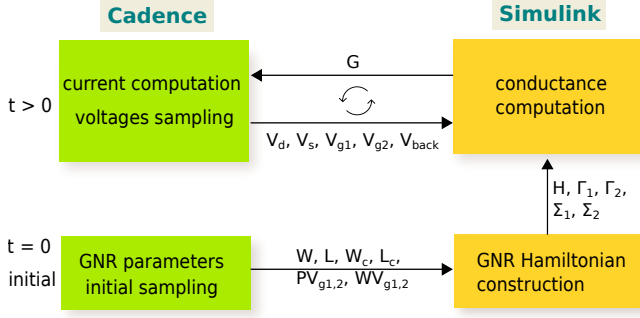


Fig. 3: Cadence-Simulink-Based Verilog-A GNR Simulation Framework.

C. Simulation flow

Let us assume a SPICE circuit description which also contains one or more GNR components, for which a transient nodal analysis is desired. At time steps automatically chosen by the SPICE solver (e.g., Cadence Spectre; Synopsys HSPICE), the Verilog-A GNR model samples the 5 voltages (afforent to the 5 pins depicted in Fig. 1).

The simulation flow we utilize in the proposed Verilog-A GNR model is presented in Fig. 3. In order to compute the conductance G , the Simulink code makes use of the GNR Hamiltonian, which is geometry dependent. Thus the Hamiltonian matrix H , and matrices $\Gamma_{1,2}$, $\Sigma_{1,2}$ are computed only once during the first-time step ($t = 0$, initial step) of the transient simulation, and saved for latter utilization in subsequent simulation steps.

Further, throughout the subsequent simulation iteration process, every time a voltage variation larger than a certain value is detected, the Verilog-A GNR model triggers the Simulink module that receives as input the GNR 5 voltages and 8 parameters (W , L , W_c , L_c , $PV_{g1,2}$, $WVG_{1,2}$). Subsequently, based on these voltages and parameters the Simulink module computes the actual and accurate GNR conductance G . Once the Simulink evaluated conductance value G is known to the Verilog-A model, the current through the GNR is updated via:

$$I(d, s) = V(d, s) \cdot G. \quad (8)$$

III. SIMULATION RESULTS

To exemplify and evaluate the Verilog-A GNR model practical applicability, we consider a test case circuit depicted in Fig. 4, composed of a capacitor of $C = 1$ fF, a resistor R , and a GNR with geometry specified by $W = 29$ a; $L = 19\sqrt{3}$ a; $W_c = 17$ a; and $L_c = 10\sqrt{3}$ a. In addition, the gate topology is given by $PV_{g1} = PV_{g2} = 2\sqrt{3}$ a, and $WVG_1 = WVG_2 = 3\sqrt{3}$ a. The GNR structure thus defined is subjected to the following voltages: $V_d = 0.2$ V; $V_b = 0$ V; $V_{g1} = 0.2$ V; and V_{g2} which is varied from 0 V to 0.2 V. The circuit is simulated with Cadence Spectre [17] and Matlab Simulink [18]. As example of simulated characteristics, we present in Fig. 5, the curves for the input voltage V_{g2} , and the resulted voltage V_s at the GNR's terminal, as well as the current through the GNR,

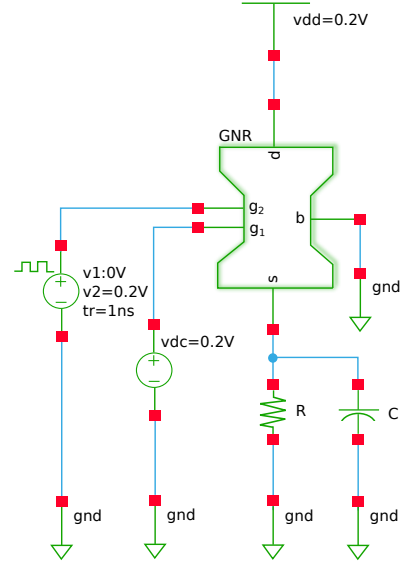


Fig. 4: One GNR-based Circuit Simulation Setup.

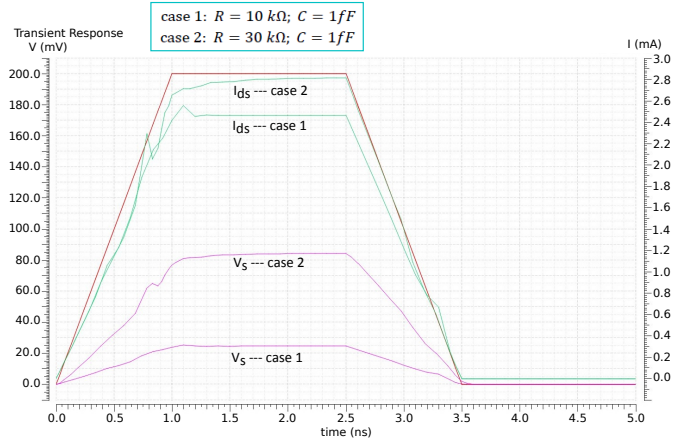


Fig. 5: One GNR-based Circuit Simulation Results.

I_{ds} , for 2 simulation scenarios: $R = 10$ k Ω (case 1), and $R = 30$ k Ω (case 2). The simulation results correctly capture the expected V_s and I_{ds} modifications induced by V_{g2} changes. Furthermore, we also observe the fact that the R value has a clear impact on the maximum I_{ds} value. We note that based on the obtained simulation results, one could easily measure the input-to-output propagation delay, and/or the power consumed by the circuit.

Further, we take as another test case circuit the GNR-based 2-input XOR gate introduced in [13], as depicted in Fig. 6. The XOR gate is constructed in a complementary way with a pull-up GNR (GNR_{up}) and a pull-down GNR (GNR_{dn}). The two GNRs perform complementary functions, i.e., they are designed in such a way that GNR_{up} maps the XOR functionality onto its conductance, while GNR_{dn} conductance reflects the XNOR functionality. The XOR gate GNR_{up} geometry and contacts topology are specified by $W = 41$ a; $L = 25\sqrt{3}$ a; $W_c = 8$ a; $L_c = 4\sqrt{3}$ a, $PV_{g1} = PV_{g2} = 1\sqrt{3}$ a, and

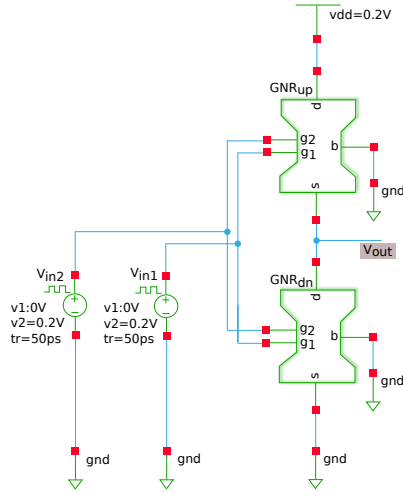


Fig. 6: GNR-based XOR Gate Simulation Setup.

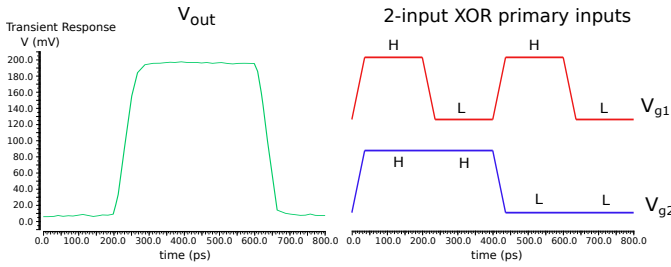


Fig. 7: GNR-based XOR Gate Simulation Results.

$WV_{g1} = WV_{g2} = 3\sqrt{3}$ a. The XOR gate GNR_{dn} dimensions and contacts topology are specified by $W = 29$ a; $L = 25\sqrt{3}$ a; $W_c = 5$ a; $L_c = 7\sqrt{3}$ a, $PV_{g1} = PV_{g2} = 6\sqrt{3}$ a, and $WV_{g1} = WV_{g2} = 3\sqrt{3}$ a. In order to simulate this test case circuit, we apply two gate inputs (V_{g1} , V_{g2}), and start with $V_{g1} = V_{g2} = 0$ V followed by $(V_{g1}, V_{g2}) = (0.2$ V, 0.2 V) \rightarrow (0 V, 0.2 V) \rightarrow (0.2 V, 0 V) \rightarrow (0 V, 0 V), as depicted in the right plot of Fig. 7, where the simulation duration is 800 ps.

The left plot in Fig. 7 captures the GNR-based XOR circuit output voltage response. We observe that the GNR-based XOR circuit exhibits the expected functionality and, based on this simulation, we derive the input to output propagation delay and power consumption of this GNR-based XOR gate as: (i) 7.48 ps delay, i.e., 18.4% smaller than that of CMOS XOR gate in 7 nm technology (9.168 ps); and (ii) 1.734 nW power consumption, i.e., 2 orders of magnitude smaller than that of 7 nm CMOS XOR gate (5.923×10^2 nW) [19].

As final remarks, we note that: (i) by computing the GNR conductance in Matlab Simulink, we benefit of accurate, physics-based results, which allows for a closer to reality assessment of the GNR-based circuits potential performance, when compared to, e.g., CMOS-based counterparts; (ii) a compact Verilog-A only model which directly embeds the NEGF-Landauer formalism would be prohibitively complex and most likely slower as it requires complex numbers matrices multiplication and inverse operations, and last but not

least (iii) our proposal can be easily extended to reflect the behaviour of other multi-gate GNR-based structures and/or to capture more GNRs into one Verilog-A model.

IV. CONCLUSIONS

In this paper we proposed an accurate physics-based Verilog-A GNR model, which enables the proper evaluation of graphene-based circuits potential performance. Our simulation results confirm its accuracy and capability to capture the behaviour of GNR based circuits, i.e., XOR gate, and to allow for performance comparison with CMOS counterparts. The development of compact Verilog-A only models, which trade accuracy for faster simulation, may constitute future work, once GNR behavior is properly understood and characterized from the circuit prospective.

REFERENCES

- [1] Liou, J. J. and Schwierz, F. and Wong, H., *Nanometer CMOS*. Pan Stanford Publishing, 2010.
- [2] Choi, W. and Lee, J. W., *Graphene Synthesis and Applications*. CRC Press, 2012.
- [3] Matsumoto, K., *Frontiers of graphene and carbon nanotubes - devices and applications*. Springer Japan, 2015.
- [4] Ferrari, A.C. and et al., "Science and technology roadmap for graphene related 2D crystals, and hybrid systems." in *Nanoscale*, vol. 7, no. 11, 2015, pp. 4587–5062.
- [5] Skakalova, V., and Kaiser, A. B., *Graphene: properties, preparation, characterisation and devices*. Elsevier, 2014.
- [6] Wu, Y. and Guo, D., "Modeling of graphene nanoribbon FET and analysis of its electrical properties." in *International Conference on Anti-counterfeiting, Security, and Identification (ASID)*, 2014, pp. 1–4.
- [7] Choudhury, M. and et al., "Graphene nanoribbon FETs: technology exploration for performance and reliability." in *IEEE Transactions on Nanotechnology*, vol. 10, no. 4, 2011, pp. 727–736.
- [8] Gholipour, M. and et al., "Analytical SPICE-compatible model of Schottky-barrier-type GNR-FETs with performance analysis." in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 2, 2016, pp. 650–663.
- [9] Fahad, M. and et al., "Analytical current transport modeling of graphene nanoribbon tunnel field-effect transistors for digital circuit design." in *IEEE Transactions on Nanotechnology*, vol. 15, no. 1, 2016, pp. 39–50.
- [10] Chen, Y. and et al., "A SPICE-compatible model of Graphene Nano-Ribbon Field-Effect Transistors enabling circuit-level delay and power analysis under process variation." in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2013, pp. 1–6.
- [11] Gholipour, M. and et al., "Highly accurate SPICE-compatible modeling for single- and double-gate GNR-FETs with studies on technology scaling." in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2014, pp. 1–6.
- [12] Jiang, Y. and Cucu Laurenciu, N. and Cotofana, S. D., "On carving basic Boolean functions on graphene nanoribbons conduction maps." in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018.
- [13] —, "Complementary arranged graphene nanoribbon-based Boolean gates." in *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2018.
- [14] Karafyllidis, I., "Current switching in graphene quantum point contacts." in *IEEE Transactions on Nanotechnology*, vol. 13, no. 4, 2014, pp. 820–824.
- [15] Datta, S., *Quantum transport: Atom to transistor*. Cambridge University Press, 2005.
- [16] Nikiforidis, I. and Karafyllidis, I. and Dimitrakis, P., "Simulation and parametric analysis of graphene p-n junctions with two rectangular top gates and a single back gate." in *Journal of Physics D: Applied Physics*, vol. 51, 2018, pp. 1–6.
- [17] Cadence. [Online]. Available: <https://www.cadence.com/>.
- [18] Simulink. [Online]. Available: <https://www.mathworks.com/>.
- [19] Predictive Technology Model. [Online]. Available: <http://ptm.asu.edu/>.