Complementary Arranged Graphene Nanoribbon-based Boolean Gates

Yande Jiang
Computer Engineering Laboratory
Delft University of Technology
Delft, The Netherlands
Yande.Jiang@tudelft.nl

Nicoleta Cucu Laurenciu
Computer Engineering Laboratory
Delft University of Technology
Delft, The Netherlands
N.CucuLaurenciu@tudelft.nl

Sorin Cotofana
Computer Engineering Laboratory
Delft University of Technology
Delft, The Netherlands
S.D.Cotofana@tudelft.nl

ABSTRACT

With CMOS feature size heading towards atomic dimensions, unjustifiable static power, reliability, and economic implications are exacerbating, prompting for research on new materials, devices, and/or computation paradigms. Within this context, Graphene Nanoribbons (GNRs), owing to graphene's excellent electronic properties, may serve as basic blocks for carbon-based nanoelectronics. In this paper we build upon the fact that GNR behaviour can be controlled according to some desired functionality via top/back gate contacts and propose to combine GNRs with complementary functionalities to construct Boolean gates. To this end, we introduce a generic GNR-based Boolean gate structure, composed of two GNRs, i.e., a pull-up GNR performing the gate Boolean function and a pull-down GNR performing the inverted Boolean function. Subsequently, by properly adjusting GNRs' dimensions and topology, we design 2-input AND, NAND, and XOR graphene-based Boolean gates, as well as 1-input gates, i.e., inverter and buffer. Our SPICE simulations indicate that the proposed gates exhibit a smaller propagation delay, from 23% for the XOR gate to 6× for the AND gate, and 2 orders of magnitude smaller power consumption, when compared with 7 nm CMOS based counterparts, while requiring a 1 to 2 orders of magnitude smaller active area footprint. These results clearly indicate that GNR-based gates have great potential as basic building blocks for future beyond CMOS energy effective nanoscale circuits.

CCS CONCEPTS

• **Hardware → Integrated circuits**; **Logic circuits**;

KEYWORDS

Graphene, GNR, Graphene-based Boolean Gates, Carbon-Nanoelectronics

ACM Reference Format:
Yande Jiang, Nicoleta Cucu Laurenciu, and Sorin Cotofana. 2018. Complementary Arranged Graphene Nanoribbon-based Boolean Gates. In *NANOARCH '18: IEEE/ACM International Symposium on Nanoscale Architectures, July 17–19, 2018, Athens, Greece.* ACM, New York, NY, USA, 6 pages. https://doi.org/10.1145/3232195.3232199

NANOARCH '18, July 17–19, 2018, Athens, Greece

ACM ISBN 978-1-4503-5815-6/18/07…$15.00
https://doi.org/10.1145/3232195.3232199

1 INTRODUCTION

As CMOS scaling approaches atomic feature size limit, resulting in high power density and leakage, low reliability and yield, and increased IC production costs, and thus increased diminishing returns, new materials, structures, and computation paradigms are called for [1], [2]. One of the post-Si fore-runners is graphene, whose research popularity has surged during the past decade, paving the way for graphene-based applications, e.g., spintronics, photonics and optoelectronics, sensors, energy storage and conversion, flexible electronics, and biomedical applications [3], [4], [5], [6].

Graphene is a 2D carbon atom honeycomb lattice with unique, remarkable properties, such as room temperature electron mobility (10× higher than Si), low effective electron masses, ultimate thinness, high thermal conductivity, as well as ballistic carrier transport with long carrier mean-free paths [7], [8], [9]. These properties provide a strong incentive to investigate graphene as a potent contender to Si and follow avenues for carbon-based nanoelectronics [10], [11], [12]. From the design point of view, there are several impediments to graphene-based Boolean logic to be considered: (i) controlling conductivity to obtain distinguishable "on" and "off" states, while not compromising graphene's intrinsic highly advantageous properties (e.g., high carrier mobility), (ii) encoding the desired Boolean logic transfer function into graphene's electrical characteristics (e.g., conduction maps), (iii) finding proper external electric means (e.g., top gates, back gates) to control the graphene behavior and induce the desired logic functionality, (iv) ensuring the conditions for cascading digital circuits, i.e., clean and compatible/matching gate inputs and outputs electric levels, (v) understanding the GNRs interaction when interconnected, and (vi) finding a way for constructing graphene based gates/circuits by properly combining GNRs.

Previous work in [13] demonstrated that by augmenting the trapezoidal Quantum Point Contact (QPC) topology in [14], with top gates, and by changing its GNR geometry, it is possible to enable GNR conductance modulation by means of external voltages, such that it mirrors the behaviour of Boolean logic functions. While this structure addresses (i)-(iii) related issues, and serves as basic ingredient to construct Boolean gates, several aspects are yet to be considered, foremost, how to shape and combine different GNRs in order to obtain Boolean gates with clean and compatible operation voltage levels for their primary inputs and outputs.

In this paper, we address GNR electrical interaction issues (iv)-(vi), in order to construct graphene-based Boolean gates. Specifically, we introduce a methodology to design GNR-based Boolean gates, and propose the set of 1 and 2-input gates {BUFF, INV}, and

{AND, NAND, XOR}, respectively. Each GNR-based gate is composed of two GNRs arranged in a complementary manner (i.e., a pull-up GNR which performs the gate desired Boolean function and a pull-down GNR which preforms the inverse Boolean function). The underlying GNR structures relies on a graphene zigzag ribbon as conduction channel between two end-point contacts (drain and source) while gate primary input voltages are applied via one/two top gate/s. Given that each gate requires GNRs with specific behaviour (e.g., conductance) corresponding to the Boolean function they mimic, we identify the topology and dimensions able to deliver each basic function, i.e., AND, NAND, XOR, XNOR, INV, and BUFF, behaviour by means of a design space exploration with respect to GNR shape, dimensions, and top gate contacts topology, subject to certain constraints (e.g., gate output voltage values compatible with input voltage values, high ratio between GNR's high and low conductance values).

We validate and evaluate the proposed GNR gates in Cadence by means of SPICE simulation that makes use of a Verilog-A model, which internally calls a Simulink model to derive the GNR conductance using the NEGF-Landauer formalism [15], [14], [16]. To get inside into our proposal potential we evaluate the GNR based gates in terms of propagation delay, active area footprint, and power consumption, and compare them with 7 nm FinFET CMOS [17] based counterparts. Our results indicate (i) smaller propagation delay, ranging from 23% for the XOR gate to 6× for the AND gate, (ii) 1 to 2 orders of magnitude smaller active area footprint, and (iii) 2 orders of magnitude smaller power consumption. We note that, as opposed to CMOS designs, the proposed GNR-based gates can enable effective power-delay trade-offs, at roughly the same area, as the graphene conductance main contributor is the nanoribbon geometry and overall topology, rather than the effective occupied area. Moreover, the Boolean function complexity does not necessarily bare a directly proportional relationship with the GNR based gate required area (e.g., the GNR-based INV area is similar to the GNR-based XOR area), which benefits the layout. The obtained results indicate that, due to their figures of merit, the proposed GNR-based complementary gates have great potential as basic building blocks for future beyond CMOS energy effective nanoscale circuits.

The remaining of this paper is structured as follows: Section 2 presents the proposed GNR-based Boolean gates, and the afferent design methodology. Section 3 describes the simulation framework, while Section 4 entails the obtained results. Finally, we conclude the paper with some remarks in Section 5.

2 COMPLEMENTARY GNR PAIR-BASED BOOLEAN GATES

In this section, we present the design methodology of the proposed GNR-based Boolean gates, and the rationale behind their construction.

We start by noting that the two key elements towards graphene-based circuits, are (i) opening the graphene energy bandgap to effectively switch off the current, and (ii) finding the means to control GNR conductance and enact an electrical response according to a desired Boolean functions. To this end, a trapezoidal graphene Quantum Point Contact (QPC), with zig-zag edges [14], is used as GNR research vehicle to build upon. The GNR can serve as a

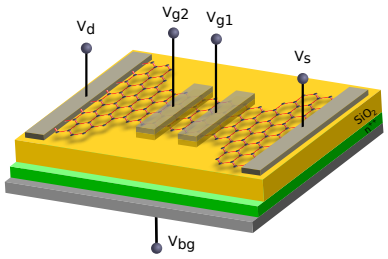

Figure 1: Boolean Gate Graphene-based Building Block.

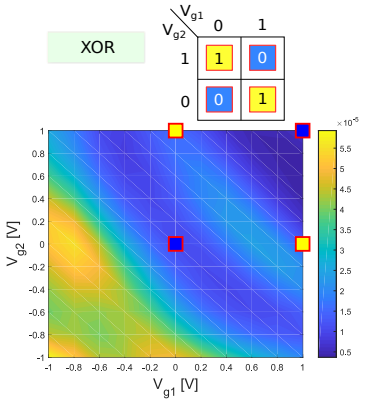

Figure 2: 2-input XOR Boolean Logic Conductance Map.

conduction channel between two end-point contacts, e.g., drain and source, which are biased by a voltage $V_d - V_s$. By changing the GNR geometry, the bandgap opening problem can be addressed to a certain extent. Adding on top of the GNR gates with various contact topologies and shaping the GNR geometry, the graphene conductance can be modulated (by means of external voltages applied via the top gates), such that it can mirror a desired Boolean function. The GNR structure augmented with top and back gate contacts, as previously described is graphically illustrated in Figure 1 and constitutes the main ingredient to construct GNR-based Boolean gates. Figure 2 depicts for instance, the conductance map obtained for a GNR whose geometry was optimized such that it reflects Boolean XOR operator functionality, for logic high and low voltage levels associated with 1 V and 0 V, respectively.

In the following, we build upon the structure in Figure 1 and propose GNR-based complementary Boolean gates. To this end, we construct every gate with two GNR basic building blocks, a pull-up GNR structure, denoted as GNR_{up}, which has its drain contact connected to the supply voltage V_{DD}, and a pull-down GNR structure, denoted subsequently as GNR_{dn}, which has its source terminal connected to the ground V_{SS}, as illustrated in Figure 3. The pull-up and the pull-down GNRs perform complementary functions, e.g., an AND gate is composed of a GNR_{up} which mirrors the AND logical functionality onto its conductance, and of a GNR_{dn} whose conductance maps the NAND logic functionality.

In order to obtain the appropriate GNRs for each gate, we perform a design space exploration, by varying the following parameters: (i)

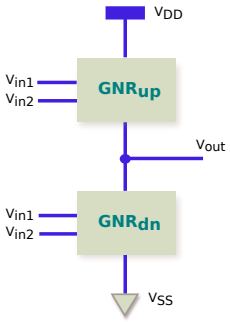

Figure 3: GNR Boolean Gate with Complementary GNRs.

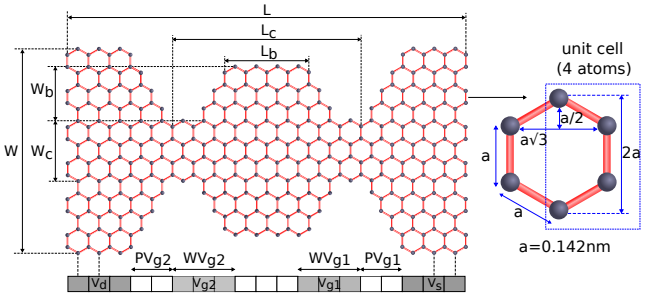

Figure 4: GNR Topology Parameters.

nanoribbon geometry (i.e., total length L and width W, constriction length L_c and width W_c, and bump width W_b and top length L_b), and (ii) top gate contacts topology (i.e., position with respect to the source and drain contacts P_{V_g}, and width W_{V_g}), as defined in Figure 4.

The gate output voltage in Figure 3 can be approximated as:

$$V_{out} = V_{DD} \cdot \frac{G_{up}}{G_{dn} + G_{up}}, \tag{1}$$

where G_{up} and G_{dn} are the conductances of the pull-up and pull-down GNR, respectively. Thus, during the design space exploration process we need to take into account several aspects, as follows:

- A high ratio between the pull-up and pull-down GNRs conductances is the key factor towards obtaining output voltages closer to the supply and ground rails, and low leakage power. Specifically, when the gate output voltage should pull-up to V_{DD}, the ratio G_{up}/G_{dn} should be at least > 10, in order to obtain $V_{out} \geq 91\% \cdot V_{DD}$. Conversely, when the gate voltage should pull-down to V_{SS}, the ratio G_{up}/G_{dn} should be smaller than $1/10$, in order to obtain $V_{out} \leq 9.1\% \cdot V_{DD}$.
- The conductance modulated via the gate input voltages shouldn't exhibit non-linear behaviour, in order to avoid spurious transients for the gate output voltage.
- Conductance values enabling a reasonable input to output propagation delay and power trade-off are preferable.
- Balanced output switching delay (i.e., "0" → "1" delay similar to "1" → "0" delay).

As a result of the design space exploration, we found 3 types of GNR shapes, i.e., butterfly, double butterfly, and camel, illustrated in Figure 5 as being the most relevant for constructing GNR Boolean gates. In Section 4 we demonstrate that by properly adjusting their dimensions they provide the functionalities required to build all the considered basic logic gates.

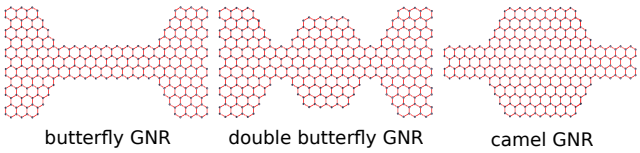

Figure 5: GNR Shapes for Boolean Gates.

We note that to build networks of gates and enable GNR circuit design, the GNR gates can be cascaded directly, as their input and output voltages are compatible. However, similar to the CMOS case, some circuit topologies may result in signal integrity degradations, and buffers, as the one presented in Section 4, are required in order to restore the logic low and high voltage levels.

3 SIMULATION SETUP

In this section, we present the underlying formalism for computing GNR's electrical properties and describe the SPICE GNR-based Boolean gates simulation setup.

3.1 GNR Electronic Transport Computation Model

For the electronic ballistic transport computation, we used the Non-Equilibrium Green's Function (NEGF)-Landauer formalism. The GNR channel is described by a Hamiltonian matrix H, which incorporates all internal and external potentials (e.g., top gate and back gate voltages). H is constructed using semi-empirical (tight-binding) computations, as:

$$H = \sum_{i,j} t_{i,j} \left|i\right\rangle \left\langle j\right|, \tag{2}$$

$$\text{where } t_{i,j} = \begin{cases} 0, & \text{if atoms } i \text{ and } j \text{ are not adjacent} \\ \tau, & \text{otherwise,} \end{cases} \tag{3}$$

and $\tau = -2.7$ eV. On the channel end sides, the drain and source contacts with different electrochemical potentials sustain the channel conduction, and the contact channel interactions are modelled via the contact self-energy matrices Σ_1 and Σ_2, respectively. After H and $\Sigma_{1,2}$ are derived, the transmission function $T(E)$, which models the probability of one electron being transmitted between the source and the drain contacts, is computed as a function of energy as:

$$T(E) = \text{Trace}\left[\Gamma_1 \; G_R \; \Gamma_2 \; G_R^{\dagger}\right] \tag{4}$$

where

$$G_R(E) = [EI - H - \Sigma_1 - \Sigma_2]^{-1}$$

$$\Gamma_{1,2} = i[\Sigma_{1,2} - \Sigma_{1,2}^{\dagger}].$$

The channel current is then derived based on Landauer formula, as:

$$I = \frac{q}{h} \int_{-\infty}^{+\infty} T(E) \cdot (f_0(E - \mu_1) - f_0(E - \mu_2)) \; dE, \tag{5}$$

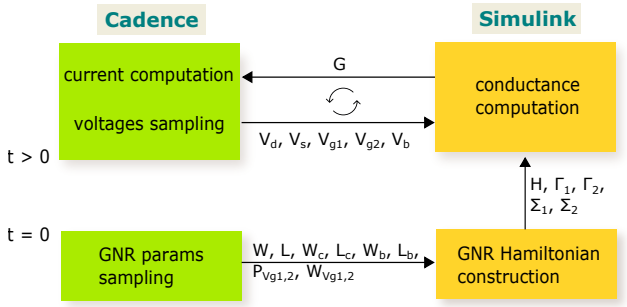

Figure 6: Cadence-Simulink GNR Simulation Flow.

where $f_0(E)$ denotes the Fermi-Dirac distribution function at temperature T, and $\mu_{1,2}$ represent the source and drain contacts Fermi energy. Finally, the conductance writes as:

$$G = \frac{I}{V_d - V_s}. \tag{6}$$

3.2 GNR Spice Simulation

To validate and evaluate the proposed GNR-based Boolean gates we make use of SPICE simulation in Cadence [18]. Each gate's GNR is modeled via a Verilog-A model with 5 pins (2 inout pins: source and drain, and 3 input pins: top gate 1, top gate 2, and back gate). To accommodate a wide range of GNR shapes and gate topologies, we developed a parametric Verilog-A model able to account for: nanoribbon total width W and length L, constriction width W_c and length L_c, bump width W_b and top length L_b, position of the top gate contacts relative to the source/drain contacts $P_{V_{g1,2}}$, and top gate contact widths $W_{V_{g1,2}}$, as previously defined in Figure 4. To benefit of accurate, physics level results, the Verilog-A model internally triggers a Simulink model which computes the GNR conductance according to the formalism presented in Section 3.3. The communication between Cadence and Simulink [19] is schematically illustrated in Figure 6. At the initial time step $t = 0$, based on the GNR geometry (specified by 10 parameters, as illustrated in Figure 6), Simulink computes the Hamiltonian H, the source and drain contacts self-energy, Σ_1 and Σ_2, and their energy broadening factors, Γ_1 and Γ_2. Then, for each and every of the remaining transient simulation time steps, Simulink receives as inputs from Cadence 5 voltages (V_d, V_s, V_{g1}, V_{g2}, and V_b), and based on the matrices computed during the initial time step it computes the corresponding GNR conductance G and passes this value back to Cadence. Once the conductance value is known to the Verilog-A model, the current through the GNR is updated using the relation: $I(d,s) = V(d,s) \cdot G$.

3.3 GNR Gates Spice Simulation

The proposed GNR gates are simulated in Cadence by using the generic setup presented in Figure 8. For each gate, there are two GNRs connected in series. The GNRs back gate voltage is connected to 0 V. As logic low voltage level, we use 0 V, while for logic high voltage level, we employ 0.2 V. The gate two primary input voltages, are periodic pulse signals, with 400 ps and 800 ps period, respectively, with 50 ps rise/fall time, and 50% duty cycle. For 1-input gates, i.e., inverter and buffer, V_{g2} is connected to 0 V.

Table 1: Dimensions of GNR Complementary Boolean Gates.

		(W, L)	(W_c, L_c)	(W_b, L_b)	(P_{V_g}, W_{V_g})
AND	GNR_{up}	$(41, 27\sqrt{3})$	$(8, 4\sqrt{3})$	$(0, 0)$	$(2\sqrt{3}, 6\sqrt{3})$
	GNR_{dn}	$(29, 25\sqrt{3})$	$(0, 0)$	$(9, 7\sqrt{3})$	$(6\sqrt{3}, 3\sqrt{3})$
NAND	GNR_{up}	$(29, 25\sqrt{3})$	$(0, 0)$	$(11, 7\sqrt{3})$	$(6\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 27\sqrt{3})$	$(8, 4\sqrt{3})$	$(0, 0)$	$(2\sqrt{3}, 6\sqrt{3})$
XOR	GNR_{up}	$(41, 25\sqrt{3})$	$(8, 4\sqrt{3})$	$(0, 0)$	$(1\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(29, 25\sqrt{3})$	$(5, 7\sqrt{3})$	$(0, 0)$	$(6\sqrt{3}, 3\sqrt{3})$
BUFF	GNR_{up}	$(29, 25\sqrt{3})$	$(5, 7\sqrt{3})$	$(2, 6\sqrt{3})$	$(3\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(29, 25\sqrt{3})$	$(0, 0)$	$(9, 7\sqrt{3})$	$(0, 6\sqrt{3})$
INV	GNR_{up}	$(41, 25\sqrt{3})$	$(14, 6\sqrt{3})$	$(2, 5\sqrt{3})$	$(6\sqrt{3}, 3\sqrt{3})$
	GNR_{dn}	$(41, 25\sqrt{3})$	$(14, 6\sqrt{3})$	$(3, 4\sqrt{3})$	$(6\sqrt{3}, 3\sqrt{3})$

All dimensions are expressed in terms of a =0.142 nm, the distance between adjacent carbon atoms.

4 SIMULATION RESULTS

Subsequently, we present the topology of each proposed GNR gate, validate its correct operation, and further evaluate it in terms of performance, area, and power, relative to 7 nm CMOS counterparts.

Figure 9 graphically illustrates the GNR shapes for the proposed set of 1-input and 2-input GNR-based basic gates. We note that, intuitively speaking, GNR_{up} and GNR_{dn} are interchangeable as part of two gates which perform inverse Boolean functions, i.e., we can use the same 2 GNRs for both AND gate and NAND gate per se. However, since the pull-up GNR is connected to V_{DD} and V_{out}, when connecting it as pull-down GNR to V_{out} and V_{SS} for the inverse gate, its conductance map might deviate from expected behaviour (might not properly mirror the same Boolean function). Thus, it becomes necessary to use different GNRs for the same Boolean function, for function complementary gates. The proposed GNR gates geometry and contacts topology, optimized for 0.2 V operating voltage, are summarized in Table 1. GNR gate designs operating on other supply voltage values, e.g., ranging from mV to V, are feasible and result in different power-delay-area tradeoffs, but require the identification of GNR topologies able to deliver the desired functionality under the new bias conditions. In principle, power supply value is constrained by delay and robustness requirements, but our choice for 0.2 V is mainly motivated by the fact that we wanted to probe graphene logic delay and power potential while maintaining GNR dimensions within a feasible range.

All gates GNRs have similar total length and width, but different constriction and bump dimensions. The constriction/bump

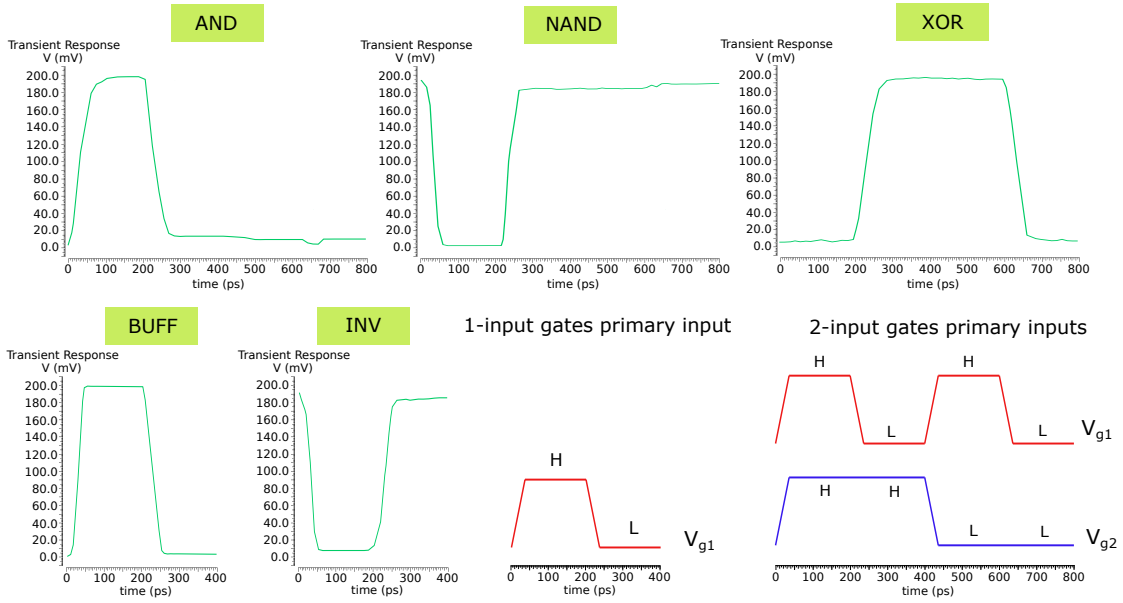

Figure 7: GNR Gate Output Voltage.

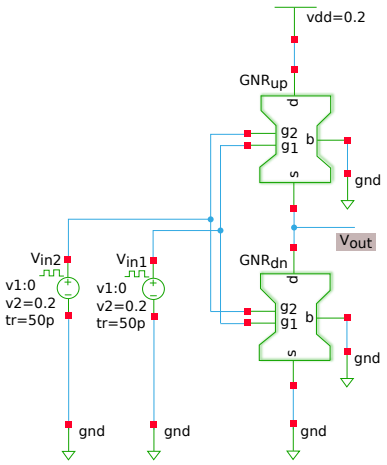

Figure 8: GNR Gate Spice Simulation Setup.

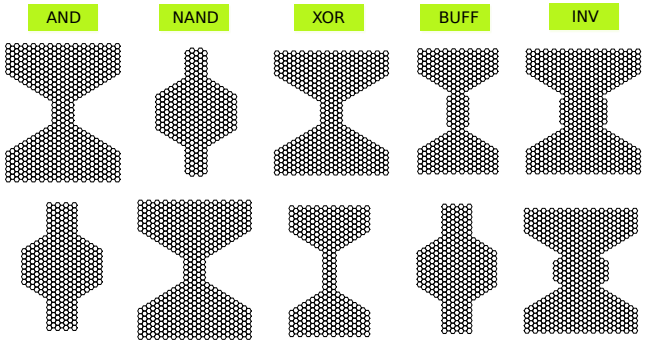

Figure 9: GNR_{up} (top row) and GNR_{dn} (bottom row) for Boolean Gates.

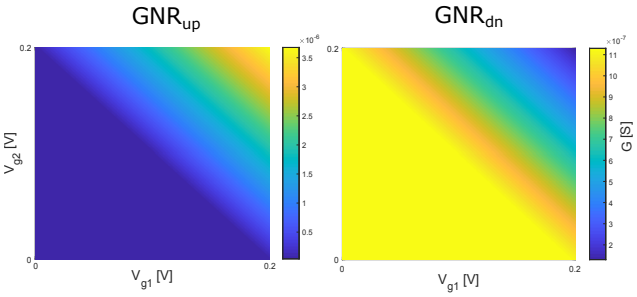

Figure 10: AND Gate GNR Conductance Maps.

width has a big impact on the conductance, which doesn't hold true for its length dimension influence. Thus, as one can infer from the Table 1, the constriction and bump width parameters can vary significantly between GNRs corresponding to different Boolean functions. One can also observe that the top gates contacts are placed closer to the source/drain contacts for the GNRs mapping {AND, OR, XOR, BUFF} Boolean logic, and further for {NAND, NOR, INV}, while the top gate contacts width remains the same for all GNRs with 2 exceptions (i.e., the GNRs mapping {AND, INV} Boolean functions).

To illustrate the complementary operation of proposed GNR-based Boolean gates, we consider the GNR-based AND gate, and present in Figure 10, the two conductance maps corresponding to its pull-up and pull-down GNRs. As it can be noticed, the 4 corner conductance points mirror logical AND functionality for GNR_{up}, and the inverted function (NAND) for GNR_{dn}. The two density

Table 2: Propagation Delay, Area, and Power Consumption

	$\tau_p[ps]$		Active Area $[nm^2]$		Total Power $[nW]$	
	GNR	CMOS	GNR	CMOS	GNR	CMOS
AND	1.38	9.618	$4.272 \cdot 10^1$	$1.452 \cdot 10^3$	4.628	$5.886 \cdot 10^2$
NAND	2.15	7.556	$4.146 \cdot 10^1$	$9.680 \cdot 10^2$	2.370	$5.415 \cdot 10^2$
XOR	7.48	9.168	$4.038 \cdot 10^1$	$2.420 \cdot 10^3$	1.734	$5.923 \cdot 10^2$
BUFF	0.42	2.040	$3.283 \cdot 10^1$	$9.680 \cdot 10^2$	0.937	$4.704 \cdot 10^2$
INV	0.27	1.110	$5.431 \cdot 10^1$	$4.840 \cdot 10^2$	0.947	$4.621 \cdot 10^2$

plots are also indicative of the proposed gate robustness to gate input voltages variations. For instance, $\approx$ 5% variation of the input voltages results in $\approx$ 4.9% and $\approx$ 4.4% variation of GNR_{up} and GNR_{dn} conductance, respectively.

Figure 7 depicts the {AND, NAND, XOR, BUFF, INV} GNR gates response when starting with $V_{g1} = V_{g2} = 0$ V followed by $(V_{g1}, V_{g2}) = (0.2, 0.2) \rightarrow (0, 0.2) \rightarrow (0.2, 0) \rightarrow (0, 0)$ for 2-input gate and $V_{g1} = 0.2 \rightarrow 0$ for 1-input gate, respectively. The simulation duration is 800 ps and 400 ps for 2-input and 1-input gates, respectively. We observe that all gates exhibit correct operation according to the afferent Boolean function. One can notice the presence of small spikes on the output voltage evolution. We attribute these spurious transients on one hand to the feedback currents of the input voltage sources, and on the other hand to non-linearities present in the dependence of the GNR conductance G on the voltages to which the GNR is subjected.

Table 2 summarizes the input to output propagation delay, the active area requirements, and the power consumption for all proposed GNR gates and for 7 nm FinFET CMOS [17] (V_{DD} =0.7 V) counterparts. Area-wise, for a fair comparison, instead of the total standard cell footprint (which is not available for GNR gates), we only consider the conduction channels area of the encompassed devices. As concerns the power, we measure in SPICE the total power for all the 4 clock cycles. The tabulated results reveal an input to output propagation delay reduction for the GNR gates, relative to the CMOS counterparts, ranging from 23% for the XOR gate, up to 6× for the AND gate, and 2 orders of magnitude smaller power consumption in all cases. Moreover, the GNR gates require a 1 to 2 orders of magnitude smaller active area footprint, when compared to 7 nm, the most advanced CMOS technology node [20], counterparts. We observe that, while for the {AND, NAND, XOR} CMOS gates, the propagation delay and power figures are similar, for the GNR gates this is not the case. For example, the GNR AND delay is 4.4× smaller than the GNR XOR gate delay. However, the GNR AND power consumption is 1.6× higher than that of the one of the GNR XOR. This is a direct consequence of our choice to design a faster GNR AND gate at the expense of increased power consumption. However, one may opt for other trade-offs when designing the GNR gates.

One can also observe in the Table 2 that while the active area of different CMOS gates can vary by up to 4×, in the case of the GNR gates, the variation is within 65%. Thus, we can conclude that while, generally speaking, complex Boolean logic translates into a larger CMOS circuit area realization, this is not the case for GNR, where one can obtain a complex Boolean functionality, with very little implications on the area. For instance, considering the XOR gate relative to the NAND gate, for the CMOS case the area increases by 1.5×, while for the GNR case the area is similar (decrease by 2.7%).

5 CONCLUSIONS

In this paper, we proposed GNR-based Boolean gates and investigated their potential as building blocks for post CMOS circuits. To this end, we introduced a generic GNR-based Boolean gate constructed with two complementary arranged GNRs (one performing the gate Boolean function while the other, the inverted Boolean function). Subsequently, we identified a set of appropriate GNR geometries and topologies, while considering the gate output switching behaviour, and presented 2-input {AND, NAND, XOR} and 1-input {BUFF, INV} gate designs. We validated and evaluated the proposed gates in Cadence, while modelling the GNR conductance by means of a Verilog-A model making use of the NEGF-Landauer formalism via an internally triggered Simulink model. Our results indicate that the proposed graphene gates outperform 7 nm CMOS counterparts as follows: (i) smaller propagation delay, ranging from 23% for the XOR gate to 6× for the AND gate, (ii) 1 to 2 orders of magnitude smaller active area footprint, and (iii) 2 orders of magnitude smaller power consumption, which clearly suggests that our proposal opens a promising avenue towards carbon based nanoelectronics.

REFERENCES

[1] Liou, J. J. and Schwierz, F. and Wong, H. *Nanometer CMOS.* Pan Standford Publishing, 2010.
[2] Rupp, K. and Siegfried, S. The economic limit to Moore's law. In *IEEE Transactions on Semiconductor Manufacturing*, volume 24, pages 1–4, 2011.
[3] Ferrari, A.C. and et al. Science and technology roadmap for graphene related 2D crystals, and hybrid systems. In *Nanoscale*, volume 7, pages 4587–5062, 2015.
[4] Stankovich, S. and et al. Graphene-based composite materials. In *Nature*, volume 442, pages 282–286, 2006.
[5] Ren, W. and Cheng, H. M. The global growth of graphene. In *Nature Nanotechnology*, volume 9, pages 726–730, 2014.
[6] Marmolejo, M. J. and Velasco-Medina, J. Review on graphene nanoribbon devices for logic applications. In *Microelectronics Journal*, volume 48, pages 18–38, 2016.
[7] Skakalova, V., and Kaiser, A. B. *Graphene: properties, preparation, characterisation and devices.* Elsevier, 2014.
[8] Nilsson, J. and et al. Electronic propertiesof graphene multilayers. In *Physical Review Letters*, volume 97, pages 266801 1–4, 2006.
[9] Castro Neto, A. .H. and et al. The electronic properties of graphene. In *Reviews of Modern Physics*, volume 81, pages 109–162, 2009.
[10] Choi, W. and Lee, J. W. *Graphene Syntehsis and Applications.* CRC Press, 2012.
[11] Allen, J. M. and Tung, V. C. and Kaner, R. B. Honeycomb carbon: a review of graphene. In *Chemical Reviews*, volume 110, pages 132–145, 2010.
[12] Matsumoto, K. *Frontiers of graphene and carbon nanotubes - devices and applications.* Springer Japan, 2015.
[13] Jiang, Y. and Cucu Laurenciu, N. and Cotofana, S. D. On carving basic Boolean functions on graphene nanoribbons conduction maps. In *IEEE International Symposium on Circuits and Systems (ISCAS), to appear.*, 2018.
[14] Karafyllidis, I. Current switching in graphene quantum point contacts. In *IEEE Transactions on Nanotechnology*, volume 13, pages 820–824, 2014.
[15] Datta, S. *Quantum transport: Atom to transistor.* Cambridge University Press, 2005.
[16] Nikiforidis, I. and Karafyllidis, I. and Dimitrakis, P. Simulation and parametric analysis of graphene p-n junctions with two rectangular top gates and a single back gate. In *Journal of Physics D: Applied Physics*, volume 51, pages 1–6, 2018.
[17] Predictive Technology Model. [Online]. Available: http://ptm.asu.edu/.
[18] Cadence. [Online]. Available: https://www.cadence.com/.
[19] Simulink. [Online]. Available: https://www.mathworks.com/.
[20] TSMC Future Research and Development Plans. [Online]. Available: http://www.tsmc.com/english/dedicatedFoundry/technology/future_rd.htm.