Power Analysis of Parallel CA-CFAR FPGA Design

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***Abstract*—We provide a power analysis of a parallel implementation of the Cell Average Constant False Alarm Rate (CA-CFAR) algorithm in reconfigurable hardware, originally proposed by the authors. The design is based on a parallel processing scheme employing extensive data reuse and synchronized sliding windows over the input data sequence. A scalable parallel structure is designed and mapped on *Xilinx Virtex II Pro* and *Altera Stratix I* technology. Synthesis and post place and route results from the *Xilinx ISE* and *Quartus II* toolset suggest a linear speedup and resource utilization. More specifically, a single CFAR implementation utilizes 1.4% of the VIRTEX II Pro XC2VP30 chip and 2% for Altera EP1S25F780C5 chip, providing a throughput of 974 Mbps. The power consumption of the design is evaluated per technology. The maximum allowed frequencies are determined and compared, as well.**

Keywords- parallel CFAR processor, Field programmable gate arrays, Parallel processing, Reconfigurable architectures, Signal processing, power analysis

I. INTRODUCTION

We address the problem for parallel hardware design of a CFAR algorithm for signal detection in a noisy environment and its power consumption, utilization and maximal frequency on reconfigurable hardware. The simplest approaches for radar signal detection are the fixed threshold methods. The main advantage there is the fast signal processing. The main disadvantage is not providing reliable detection or not keeping the probability of false alarm. In other words, a random interference appearing and exceeding the detection threshold is detected as a target. Recently, the CFAR solution becomes more popular as a possible solution of this problem [1-6]. The CFAR processor uses a dedicated signal window (learning window) for previously noise and interference estimation. Therefore, the estimation is multiplied by a scalar factor, which keeps the probability of false alarm constant. Then the result is compared to the testing signal cell. As a result the threshold is adapted in concordance with the interference environment [1,2,3]. Such processing based on preliminary noise assessment, can be employed in communications, radar, and GPS systems. It is obvious that the elaborated signal detection processing requires much computational power and its real time implementation could be disputable. A substantial design challenge is that the CFAR algorithm demands significant computational power to perform the whole algorithm in real-time.

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Due to its inherent spatial parallelism, the reconfigurable technology has the potential to support design solutions that meet these high computational requirements. Hence, in this paper, we consider it as our targeted implementation technology. In contrast to earlier sequential CA-CFAR proposals and implementations our work considers a comparative parallel Cell Average (CA) CFAR implementation on two different reconfigurable technologies (*Xilinx* and *Altera*).

This paper explores the dependencies between the speed-up of a parallel realization of a particular CA-CFAR algorithm on reconfigurable hardware and the corresponding power consumption. This paper encompasses a comprehensive comparison between Xilinx and Altera technology considering the realization of k parallel CA-CFAR algorithm and comprehensive power consumption analysis. Our previous work proved that a considerable throughput is possible. A k-parallel CA-CFAR design was demonstrated, *Xilinx Virtex II Pro* technology was used [9]. The demonstrated design obtained a throughput of 974Mbps for a single CA-CFAR and 31Gbps for 32 parallel CA-CFAR on for 60 MHz clock frequency. The resource utilization was estimated from 1.4%, for single and 37.5% for a 32 parallel design considering the *Xilinx XC2VP30* chip. According to the *Xilinx Power Analyzer tool,* after *18* parallel CFAR structures the power consumption was increased dramatically. The main contributions of this paper are:

- The power consumption comparison of the particular k-parallel CA-CFAR design between *Xilinx Virtex II Pro* and *Altera Stratix I* shows different and linear dynamic power increase for the *Altera Stratix I* technology.
- For this particular design, the *Xilinx Virtex II Pro* is more energy efficient in lower degree of parallelization ($k<18$).
- For this particular design, the *Altera* technology has higher working frequency.

The remainder of the paper is organized as follows. Section 2 presents the algorithm in details. Section 3 describes the design implementation. Section 4 presents the obtained experimental comparison results and provides related discussions. Finally, section 5 concludes this paper with some final remarks.

II. PROBLEM FORMULATION AND ALGORITHM DESCRIPTION

A. Problem formulation

The contemporary radar signal processing poses very high requirements for the signal processing computational power. Being used new, elaborate algorithms and large bandwidth, the trade-off is often the computational performance. The CFAR processors are such devices. Considering the state-of-the art signal bandwidth 500MHz and 16bits data structure, the analogue to digital conversion should cover 1Gsample/s. That leads to throughput 16Gbits/s. One of the implementation solutions, which provide high processing speed, scalability and adjustability, is the implementation on reconfigurable hardware [7]. Choosing the correct reconfigurable technology is however, problem of design trade-offs. When designing the algorithm, it is not only important to obtain the necessary throughput, but also to obtain a complete view of the design: maximum resource utilization, the power dissipation, market price etc. The power consumption of the design plays an important role. For example, from an engineering point of view, the bigger power consumption causes device overheat, which should be considered and optimally dissipated. The device lasts more on autonomous battery supply. Hence, the lower consumption provides obvious market benefit and last, but not least, has less environment impact, because the electricity produce harms the nature. Furthermore, it is well known that the device working frequency is closely connected to the heat dissipation.

The purpose of this work is to compare the CA-CFAR parallelisation on two reconfigurable technologies and to reveal the dependences between the algorithm parallelisation, power consumption and the maximal possible frequencies. We believe that these results will be valuable for future CFAR hardware engineering solutions.

B. CA CFAR description

The CFAR is a well-known computational structure. This is: "a property of threshold or gain control devices that maintain an approximately constant rate of false target detections when the noise, and/or clutter levels, and/or ECM (electronic countermeasures) into the detector are variable" [10]. Those devices are used in the signal detection to decrease the possibility of false alarm caused by jamming, clutter etc. The computational structure is defined previously in various works [1,2,3,9]. It consists of two windows: learning and testing. The learning window estimates the noise and the interference. The detection threshold is established by a multiplication by a scalar factor *TA*. Next, a comparison of the result with the testing window value gives the detection decision.

Figure 1 depicts the computational structure of a common CFAR structure. Particularly, the Cell Averaging CFAR is one of the simplest CFAR processor. The noise assessment is made through mean value of the consistence in the learning window. It is based on the sum value estimation

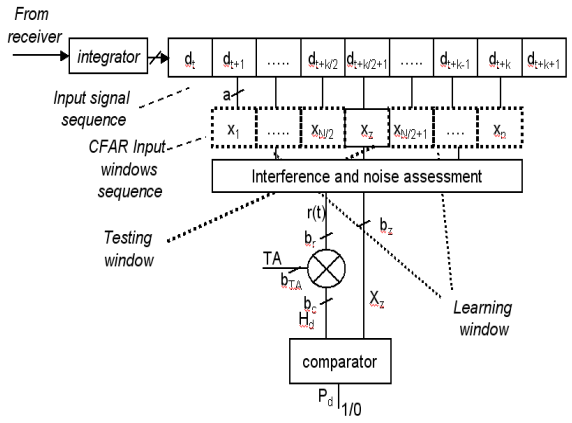

Figure 1. The Constant False Alarm Ratio (CFAR) structure [2,3]

$$r(t) = \sum_{i=1}^{n} x_i(t) \tag{1}$$

The threshold is formed according to

$$Hd = TA * r(t) \tag{2}$$

where *TA* is the pre-tabulated scalar factor, keeping the probability of false alarm. The decision for target detection is made according to:

$$Pd = \begin{cases} 1 \ , \ Hd \le x_z \\ 0 \ , \ Hd > x_z \end{cases} \tag{3}$$

III. DESIGN DESCRIPTION

The parallelism of the CFAR structure is described in [9]. Additional units before and after the computational structures, such as (buffers, integrator, and receiver) are not considered. Thus, only the pure CAFR computational structure is studied and a full parallelisation is assured. Figure 2 shows the explored *k* parallel CA-CFAR.

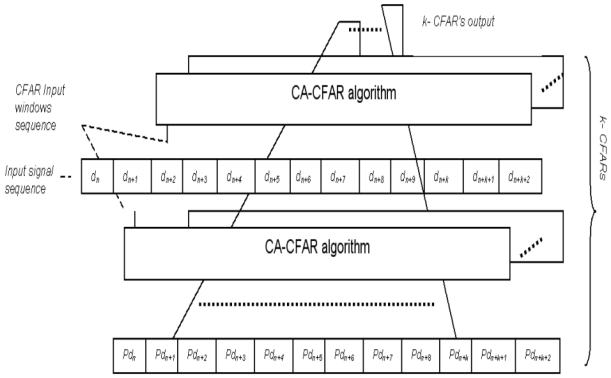

Figure 2. Parallel CA-CFAR computational structure [9]

k- parallel windows slide synchronously along the incoming data, and output *k* simultaneous results. Consequently, *k*-parallel CFAR processing is done or *k*- speed up is obtained. We consider learning CAFR length *n=17* and 16bit data length, the corresponding design data flow diagram of is depicted in Fig.3.

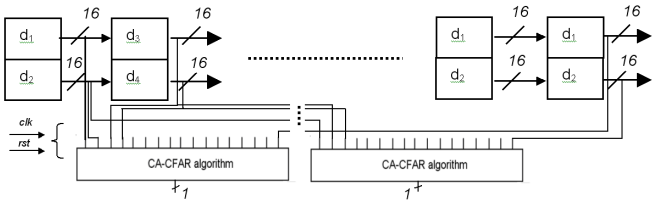

Figure 3. Hardware Data structure of two parallel CA-CFAR [9]

IV. EXPERIMENTAL RESULTS

The design is implemented on *Xilinx ISE 10.1,* and *Altera Quartus II,* and simulated through *Modelsim*. The design is tested at the maximum frequency reported by the aforementioned design tools. The VIRTEX II and the *Stratix* technologies are considered. The CA- CFAR algorithm is previously implemented in MATLAB simulation environment, a test bench is generated, which is used for hardware design verification. In the previous work [9] the approximate power analysis for the VIRTEX II technology has been made through *XPower Analyzer* tool. The chips XC2VP2-7fg256; XC2VP30-7ff1152 and XC2VP70-7ff1517, have been tested. In this work a power analysis of *Stratix* technology is made through the *PowerPlay Power Analyzer.* The Altera chip for EP1S25F780C5 is tested. A meticulous comparison between the hardware utilization and power consumption in both technologies on the same CA-CFAR design is made. The CA-CAFR implementation has a learning window size $n= 16$ and data bit width of 16.

Table I and table II depict the device utilization summary and the total power consumption distribution in the signal and logic for the *Xilinx Virtex II* technology [9].

TABLE I. DEVICE UTILIZATION SUMMARY FOR XILINX VIRTEX II PRO (XC2VP30, XC2VP70, XC2VP2) [9]

k	Number of					
	slice Flip Flops	*of 4 input LUTs*	*occupied Slices*	*total 4 input LUTs*	*used as logic*	*used as a route-thru*
1	329	371	385	385	371	14
2	402	742	587	770	742	28
4	548	1380	989	1436	1380	56
8	862	2609	1781	2721	2609	112
	840*	2401*	1406*	2513*	2401*	112*
10	1005	3215	2170	3355	3215	140
12	1165	3779	2551	3947	3779	168
16	1483	5011	3342	5235	5011	224
18	1660	5618	3754	587	5618	252
32	2778	9857	6498	10305	9857	448

**Xilinx Virtex II Pro* XC2VP2 chip

Table III provides the total utilization factor of the same design implementation on the *Stratix* technology. Table IV reveals the corresponding power consumption of the design as a function of the *k*-parallel structures for the *Stratix* technology. The *Power Play Power Analyzer* is used. During the simulation a Value Change Dump (VCD) file was generated for each parallel structure, and loaded into the power analyzer tool. The default toggle rate for the unspecified signals and the default toggle rate for the remaining signals were set to 50%. It is seen that the Stratix device utilization is linear as the Xilinx one. The power consumption has the similar linear trend. Because Xilinx and Altera use different technologies (RAM vs. flash based) the direct comparison is a complicated and disputable procedure.

TABLE II. LOGIC AND SIGNALS POWER CONSUMPTION (W) ACCORDING TO THE *XPOWER ANALYZER* [9]

k	DEVICE					
	XC2VP70		*XC2VP30*		*XC2VP2*	
	Signal	Logic	Signal	Logic	Signal	logic
1	0,127	0,072	0,126	0,069	0.117	0,074
2	0,168	0,072	0,176	0,072	0.112	0,051
4	0,197	0,083	0,191	0,088	0.177	0,079
8	0,21	0,073	0,225	0,087	0.258	0,127
10	0,201	0,06	0,27	0,096		
12	0,315	0,08	0,319	0,115		
16	0,284	0,097	0,29	0,082		
18	2,712	1,278	2,976	1,343		
32	2,992	1,395	2,918	1,282		

TABLE III. DEVICE UTILIZATION SUMMARY FOR ALTERA STRATIX I TECH (EP1S25F780C5)

k	Number of				
	Total logic elements	*Total registers*	*total LUTs*	*Total logic cells in carry chains*	*Total fan-out*
1	589 (2%)	323	300	299	1787
2	922 (4%)	390	600	598	2806
4	1367 (5%)	524	979	975	4220
8	2223 (9%)	792	1703	1695	6952
10	2651 (10%)	926	2066	2055	8318
12	3042 (12%)	1060	2390	2378	9580
16	3750 (15%)	1328	2966	2950	11896
18	4104 (16%)	1462	3254	3236	13054
32	6582 (26%)	2400	5270	5238	21160

The power consumption, the maximum allowed frequency and the market price are the parameters that could be relevantly compared.

TABLE IV. THE STRATIX I POWER CONSUMPTION ACCORDING TO THE *POWERPLAY POWER ANALYZER*

k	**DEVICE**		
	EP1S25F780C5		
	Total thermal power, mW	***Core dynamic, mW***	***Core static power consumption, mW***
1	1062.25	177.72	450.00
2	1238.20	298.40	450.00
4	1504.48	454.17	450.00
8	2023.74	752.46	450.00
10	2283.34	901.59	450.00
12	2528.60	1036.40	450.00
16	2990.45	1277.40	450.00
18	3221.35	1397.89	450.00
32	4837.13	2241.29	450.00

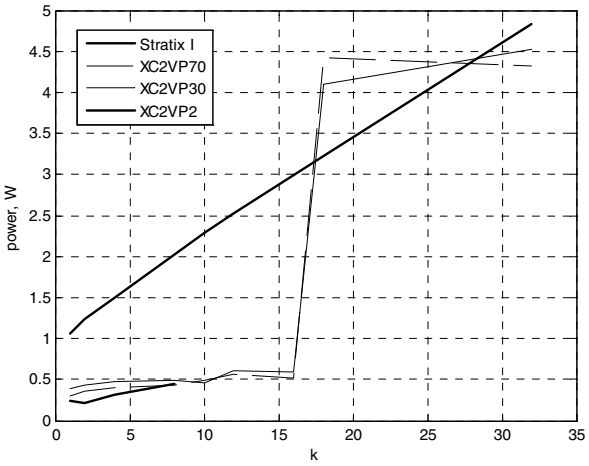

Figure 4. Total power consumption for XC2VP2, XC2VP70, XC2VP30 and *Stratix I* EP1S25F780C5 as a function of *k*

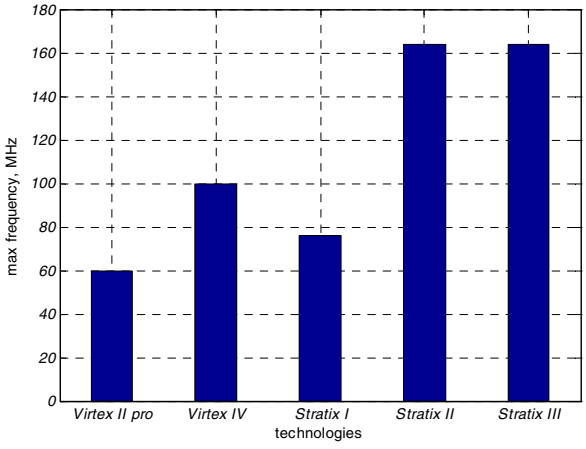

Figure 5. Maximum frequency obtained for five different technologies

Figure 4 depicts the power consumption comparison of the *k* parallel CA-CFAR design made on *Xilinx Virtex II Pro* and *Altera Stratix* technologies. It can be observed that the *Stratix I* has almost linear power consumption, whereas the *Virtex II Pro* power consumption has huge incense after *k=18.* As it was concluded in [9], this stepped growth in *Virtex II* is due to the increase of the buffers and interconnections and concerns the particular organizations of the chip resources. Considering the default toggle rate for the remaining signals as 50%, Xilinx has lower power consumption for small parallel structures ($k<18$). Figure 5 indicates the maximum frequency obtained for various *Xilinx* and *Altera* technologies. Generally, it is obvious that the *Altera* technology has better frequency performance.

V. CONCLUSIONS

This paper suggested some experience on Constant False Alarm Ratio algorithm implementations in hardware. A parallel *k*-stage CA CFAR algorithm implementation on reconfigurable hardware has been studied. The algorithm has been fully parallelized. An *Altera Stratix I* device has been studied. The power consumption comparison between *Xilinx Virtex II Pro* chips and *Altera Stratix I* chip has been performed. The power consumption of *Stratix I* has linear behavior, whereas the *Virtex II Pro* has a dramatic incense after $k=18$. The *Altera Stratix* technology has an advantage in the maximum frequency obtained. This work could be helpful in choosing the particular technology for CFAR algorithm parallelisation on reconfigurable hardware aiming the computational performance augmentation.

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