

# Bit Line Coupling Memory Tests for Single-Cell Fails in SRAMs

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## Abstract

*Due to the decreasing dimensions of manufactured devices, the effect of bit line capacitive coupling on the behavior of faulty memory cells cannot be ignored. Neighboring cells influence the faulty behavior of defective cells through coupling. This paper analyzes and validates this behavior theoretically and through electrical simulations. The paper evaluates the impact of bit line coupling in SRAMs on cell faulty behavior and identifies necessary conditions to induce worst-case coupling effects. We present a test that guarantees detecting all single-cell static faults in the presence of capacitive coupling and worst-case neighborhood data for any possible open defect.*

Keywords: Memory tests, parasitic capacitance, bit line coupling, open defects, SRAM.

## I. Introduction

Continued scaling for cell area optimization has been the driving force behind the developments of semiconductor devices, though resulting in an accelerated increase of coupling noise. Process variations make the memory very sensitive to failure, especially because of capacitive coupling among signal lines, power and ground lines, thereby resulting in high sensitivity level to open defects, shorts and bridges within the memory cell and other parts of the memory. *Bit line (BL)* coupling results in the development of small coupling voltages on adjacent BLs, which, for example, influence proper sense amplifier operation. This has a huge impact on the faulty behavior of the memory, potentially causing readily detectable memory faults to become undetectable with several tests. In fact, BL coupling and the resulting crosstalk noise is strongly considered as a limiting factor in designing high speed, low power SRAM devices [5]. Research on the impact of parasitic capacitance on the faulty behavior has up till now addressed faults in peripheral memory circuits as well as address decoders [16] A number of solutions, such as BL twisting, have been proposed to reduce cross talk noise and increase the *signal-to-noise ratio* [7], [8]. However,

such solutions focus mainly on overcoming BL coupling from a design perspective and are expensive to implement making them infeasible in many applications [9], [6].

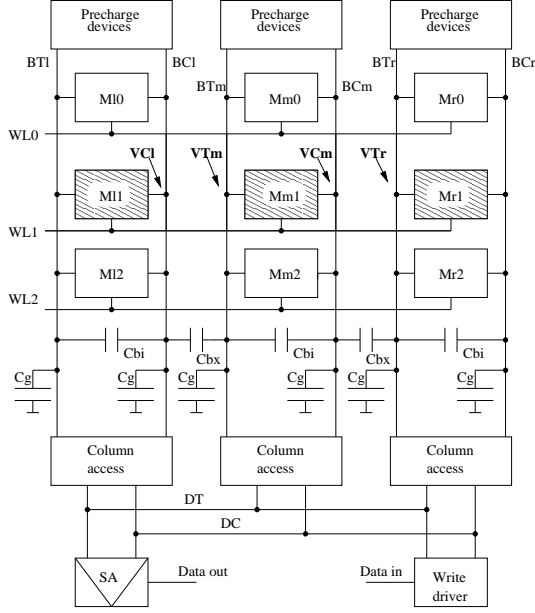
From a testing perspective, it is possible to use BL coupling to introduce extra stress on specific faults, thereby making them easier to detect by a given test [4]. Furthermore, it is essential to understand how a specific initialization of a neighborhood of cells affects the sensing of a given faulty cell, in order to write such worst-case values in the neighboring cells (worst stress condition) during testing. All of these will increase fault/defect coverage.

The contributions of this paper are as follows. A detailed evaluation of SRAM faulty behavior in the presence of both parasitic capacitance between BLs as well as varied faulty cell's neighborhood data. It shows how coupling can reduce the fault coverage of well-known memory tests, and identifies the conditions needed to ensure proper detection of memory faults while taking BL capacitive coupling into consideration. In addition, it presents a test, March SSSc that detects all single-cell static faults in the presence of BL coupling.

The rest of the paper is organized as follows. Section 2 presents an electrical Spice SRAM simulation model and shows how to analytically evaluate BL coupling capacitance. Section 3 gives a theoretical analysis of the impact of coupling on the faulty behavior of the memory. Section 4 uses Spice simulations to show how fault coverage can decrease as a result of coupling, while Section 5 derives the needed SRAM test to detect the faulty behavior while considering BL coupling in the presence of worst neighborhood data. Section 6 ends with the conclusions.

## II. Modeling of BL coupling

An electrical Spice SRAM model, is presented in Figure 1, which is used in the evaluation of BL coupling effects in this paper. The model transistor parameters are based on the 65nm BSIM4 model card as described by the Predictive Technology Model [17]. The memory has a 3x3 cell array to enable simulation of all neighboring coupling effects. These cells are connected to three BL pairs: *left BL (BLl)*, which has the *left true (BTl)* and *left complementary (BCl)* BLs, *middle BL (BLm)*, which has the *middle true (BTm)*



**Fig. 1. SRAM electrical Spice model**

and *complementary* ( $BCm$ ) BLs, and the *right BL* ( $BLr$ ), which has  $BTr$  and  $BCr$  BLs.

Each *word line* ( $WL$ ) or cell array row in the model has 3 cells: left (l), middle (m) and right (r); while each BL or cell array column has 3 cells numbered as 0, 1 and 2. The cell in the center of the array (i.e., memory cell  $Mm1$ ) is the faulty cell under analysis. Each BL is also connected to precharge devices to ensure proper initial BL voltages. Read/write access to different BLs is controlled by the column access devices, which ensure that only one BT gets connected to the *true data line* ( $DT$ ) and only one BC gets connected to the *complementary data line* ( $DC$ ) during each memory operation. The model also contains a *sense amplifier* ( $SA$ ) to inspect the read output (data out), as well as a write driver to drive input data (data in).

The total BL capacitance ( $C_t$ ) is divided into three components: internal coupling to complementary BL ( $C_{bi}$ ), external coupling to a neighboring BL ( $C_{bx}$ ) and an inherent BL capacitance to ground ( $C_g$ ) composed of coupling to all other parts of the memory (cells, WLs, substrate, etc). This is expressed as:

$$C_t = C_{bi} + C_{bx} + C_g \quad (1)$$

The exact values of these capacitances depend on the layout of the memory and its manufacturing technology. In general, the value of  $C_g$  accounts for a large portion of  $C_t$ . In literature, reported  $C_g/C_t$  ratios range from 40% to over 90% [9]. On the other hand, due to the symmetry of the layout implementation of the BLs, the values of  $C_{bi}$  and  $C_{bx}$  are rather close to each other, and therefore we consider them to be equal ( $C_{bi} = C_{bx} = C_b$ ) such that:

$$C_t \approx 2C_b + C_g \quad (2)$$

In this paper, we focus on read operations. The reason is that read operations are more sensitive to the impact of coupling than write operations. During a read operation, the WL accesses the cell and connects it to the precharged BLs. Based on the value stored in the cell, a voltage differential develops on the BLs that the sense amplifier subsequently attempts to detect. The presence of  $C_b$  causes neighboring BLs to influence the voltage development during a read. If we assume that a defective BL is totally floating, while the neighboring BL develops a voltage  $V$ , then the amount of coupling voltage ( $\Delta V$ ) induced on the floating BL can be expressed as:

$$\frac{\Delta V}{V} \approx \frac{1}{(C_g/C_b) + 1} \quad (3)$$

### III. Effects of coupling

When a specific victim cell is accessed, the only neighboring cells also being accessed at the same time are those that belong to the same row as the victim, that is, those cells connected to the same WL as the victim cell. In the model shown in Figure 1, when the middle memory cell ( $Mm1$ ) is accessed, the only other influential cells are the left memory cell ( $Ml1$ ) and the right memory cell ( $Mr1$ ) connected to the same  $WL1$ ; these are highlighted in Figure 1.

**Impact of  $Ml1$  on  $Mm1$ .** Now, we explain the impact of the data contents of the neighboring cells referred to as *coupling backgrounds* ( $CBs$ ) on the sensing of  $Mm1$ .

If cell  $Ml1$  contains a 1, then when it is accessed, it pulls  $BCl$  down by some voltage  $VCl$ . Due to BL coupling, this in turn pulls the voltage on  $BTm$  down by  $VTm$  (Figure 1). Thus, the presence of a logic 1 in  $Ml1$  makes the detection of logic 1 in  $Mm1$  more difficult while it makes the detection of logic 0 easier. On the other hand, having a 0 in cell  $Ml1$  does not modify the voltage on  $BCl$ , which in turn does not modify the voltage on  $BTm$ . In brief,

- In order to maximally stress logic 1 in  $Mm1$ ,  $Ml1$  must contain a logic 1.
- In order to stress a logic 0 in  $Mm1$ ,  $Ml1$  must *not* contain a logic 1, thereby requiring a stored logic 0 instead.

**Impact of  $Mr1$  on  $Mm1$ .** If cell  $Mr1$  contains a 0, then when it is accessed, it pulls  $BTr$  down by some voltage  $VTr$ . Due to BL coupling, this in turn pulls the voltage on  $BCm$  down by  $VCm$  (Figure 1). Thus, the presence of a logic 0 in  $Mr1$  makes the detection of logic 0 in  $Mm1$  more difficult while it makes the detection of logic 1 easier. On the other hand, having a 1 in cell  $Mr1$  does not modify the voltage on  $BTr$ , which in turn does not modify the voltage on  $BCm$ . In brief,

- In order to maximally stress logic 0 in  $Mm1$ ,  $Mr1$  must contain a logic 0.

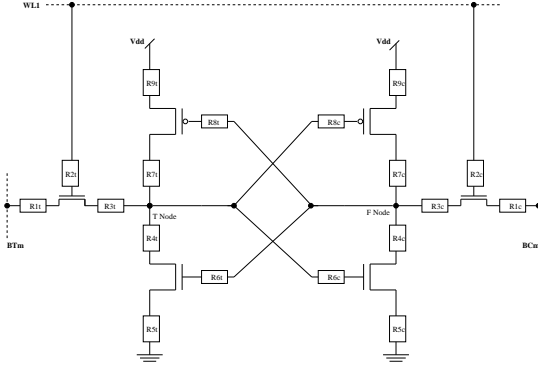


Fig. 2. 18 OD positions in SRAM cell.

- In order to stress a logic 1 in Mm1, Mr1 must *not* contain a logic 0, thereby requiring a stored logic 1 instead.

In conclusion, the most stressful background to detect parasitic BL coupling in an SRAM cell containing a logic 1 is 11 in both neighboring cells connected to the same WL (we refer to this as CB11). In contrast, the most stressful background to detect a logic 0 is CB00. These are referred to as *worst-case CBs*.

## IV. Simulations and analysis

### A. Simulated open defects

At the layout level, open defects (ODs) are usually caused by broken lines or particle contamination that results in increasing line resistivity at the open position. ODs in the memory cell array can be either opens within the cell, opens on BLs or opens on WLs.

In this paper, we focus on ODs within the SRAM cell. Figure 2 shows all possible OD positions within the SRAM cell, on which our analysis is based. As shown in Figure 2, an open resistor  $R_{\text{def}}$  is injected on the defective signal line denoted in the figure as  $R_{1t}, R_{2t}, \dots, R_{1c}, R_{2c}, \dots$ , where  $t$  and  $c$  represent the T Node and F Node sides of the cell.  $R_{\text{def}}$  can vary from  $0\Omega$  to  $\infty\Omega$ . Despite the symmetry that exists between the T and F nodes in SRAM cells, defects on both sides can exhibit different behaviors, therefore full simulations for each OD have been performed and analyzed.

For each OD evaluated, all scenarios are considered namely, read 0 and read 1 operations performed for each CB for a number of  $\frac{C_g}{C_b}$  values. The value of  $C_g$  is considered to be a typical 500fF [10], while  $\frac{C_g}{C_b}$  values are modified for each simulation in the range  $1 \leq C_g/C_b \leq 20$  [4], with used  $C_b$  values as 500fF, 100fF, 50fF, 30fF and 25fF.

In general, both the value of  $R_{\text{def}}$  as well as the amount of the coupling capacitance influence the BL voltage differential and therefore decide the eventual output logic value at the sense amplifier. This creates a space of possible  $(\frac{C_g}{C_b}, R_{\text{def}})$  values, where the defective cell can either function properly or fail. The specific resistive value in the  $R_{\text{def}}$

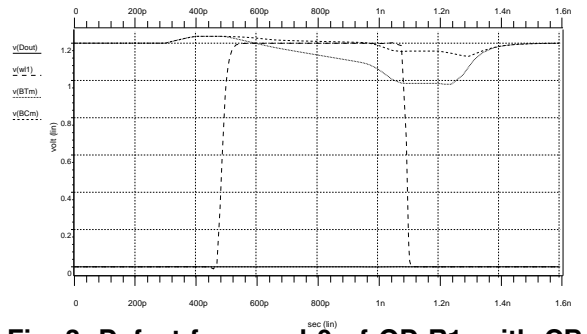


Fig. 3. Defect-free read 0 of OD-R1<sub>t</sub> with CB 00,  $\frac{C_g}{C_b} = 10$ .

range, beyond which a fail occurs is the *critical resistance* ( $R_{cr}$ ). Our analysis is based on detecting the differences in behavior between a properly functional circuit and its behavior after an OD has been injected.

### B. Simulations of OD-R1<sub>t</sub> and OD-R1<sub>c</sub>

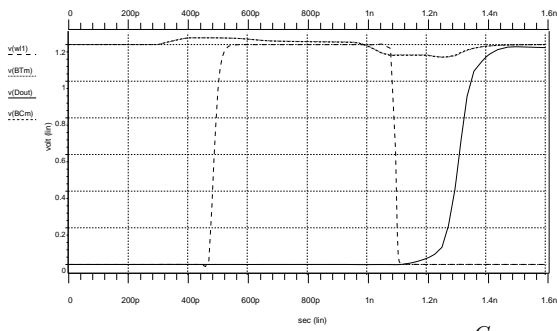
In this section, we analyze the simulated results for each read operation for OD-R1<sub>t</sub> and OD-R1<sub>c</sub> using all CBs.

**Read at Mm1 with OD-R1<sub>t</sub>.** OD-R1<sub>t</sub> is injected between the access transistor and BTm, which limits the ability of the cell to discharge BTm, thereby reducing the voltage differential between BTm and BCm, and making the sense amplifier more prone to crosstalk errors.

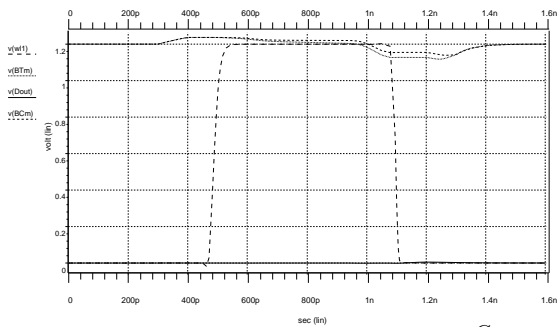
Figure 3 shows the simulation result of a defect-free read 0 in cell Mm1, with  $\frac{C_g}{C_b} = 10$  and CB 00. Once WL1 is accessed, a differential voltage starts to develop between BTm and BCm, which is then detected by the sense amplifier and amplified as a full 0, thereby leaving the data out (Dout) line at 0.

Figure 4 shows the defective simulation results of a read 0 performed on Mm1, with  $R_{\text{def}} = 110\text{K}\Omega$  and  $\frac{C_g}{C_b} = 10$  using CB 00. Comparing these with the defect-free simulation results in Figure 3, we identify a number of differences. First, the differential voltage developing on BLs is significantly reduced in the defective case between  $t = 0.4 \text{ ns}$  and  $t = 1.4 \text{ ns}$ , making it extremely difficult for the sense amplifier to identify the correct stored value in the cell. Adding to that the BL coupling voltage from neighboring cells causes the sense amplifier to detect an incorrect logic 1 in the cell rather than a logic 0, as indicated by the Dout signal in the figure. For all simulated  $\frac{C_g}{C_b}$ , OD-R1<sub>t</sub> behavior is plotted and depicted as curve CB000t in Figure 6. In the plot, the  $x$ -axis denotes  $\frac{C_g}{C_b}$ , while the  $y$ -axis represents  $R_{\text{def}}$  values. Each curve in the figure divides the  $(\frac{C_g}{C_b}, R_{\text{def}})$  plane into two regions. The region above the curve is the *fail* region while the region below is the *pass* region. Note that only CBs for which fails have been observed are included in the plot.

As curve CB000t in Figure 6 indicates, the fail region expands gradually as the amount of coupling capacitance increases (i.e., decreasing  $\frac{C_g}{C_b}$  values).



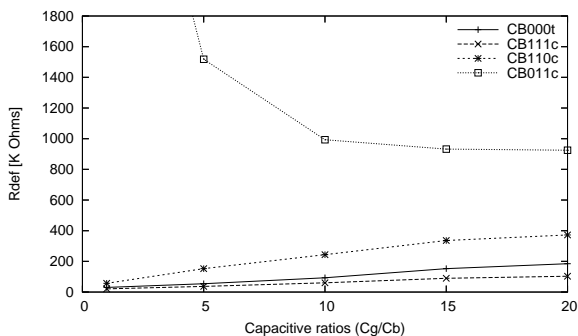
**Fig. 4. Read 0 of OD-R1<sub>t</sub>, with CB 00,  $\frac{C_g}{C_b} = 10$ ,  $R_{def} = 110K\Omega$ .**



**Fig. 5. Read 0 of OD-R1<sub>t</sub>, with CB 11,  $\frac{C_g}{C_b} = 10$ ,  $R_{def} = 110K\Omega$ .**

This buttresses the importance of keeping the amount of BL coupling capacitance small relative to the total capacitance of BL. It also indicates that with continued technology scaling, the importance of testing for coupling effects will increase.

Result of a read 0 using CB 11 is as shown in Figure 5. Again, due to the defect in the memory cell, the differential voltage on BLs is very limited. However, as a result of the CB pattern in the neighboring cells and BL coupling effects, the differential voltage is biased towards detecting a logic 0 in the cell. This bias corrects the faulty behavior and prevents detecting a fail. In the same way, using other CBs (10 and 01) corrects the faulty behavior and prevents any fault from being detected.



**Fig. 6. Pass and fail regions for OD-R1<sub>t</sub> and OD-R1<sub>c</sub>**

A read 1 in the presence of OD-R1<sub>t</sub> will produce a correct logic 1 at the output irrespective of CBs used. The reason is that for a read operation, BL voltages are influenced by the cell node voltages. Since BLs are precharged to  $V_{dd}$ , only one BL is discharged during the operation, in this case BCm. Since BTm is not discharged, a read 1 operation will yield a correct logic 1 output.

**Read at Mm1 with OD-R1<sub>c</sub>.** OD-R1<sub>c</sub> lies between BCm and the pass transistor at the F Node side (symmetric counterpart of OD-R1<sub>t</sub>) of the cell.

For a read 1 using CB 11, the differential voltage developing on BLs is significantly reduced in the defective case between  $t = 0.4$  ns and  $t = 1.4$  ns. An increase in coupling capacitance results in making the faulty behavior more dominant causing the sense amplifier to record an incorrect logic 0 instead of a logic 1. Plots of  $R_{cr}$  at varying  $\frac{C_g}{C_b}$  for OD-R1<sub>c</sub> for CB 11 is shown in Figure 6 depicted by curve CB111c. Coupling due to both CBs 01 and 10 also yielded incorrect read outputs as depicted by curves CB011c and CB110c.

Thus, CBs 01, 10 and 11 are stressful, while the use of CB 00 corrects the faulty behavior. A read 0 in the presence of OD-R1<sub>c</sub> succeeds irrespective of the CB used.

### C. Analysis of other ODs

In this section, we present a behavioral summary for the rest of the open defects in the cell. The simulation results and analysis for OD-R2<sub>t</sub> ... OD-R9<sub>t</sub> (all on the T Node side) are listed in the upper part of Table I, while those for OD-R2<sub>c</sub> ... OD-R9<sub>c</sub> (all on the F Node side) are listed in the lower part of Table I. The first column of Table I lists the ODs, while the second column lists the corresponding worst case CB. The third column gives the values of  $R_{cr}$  at  $\frac{C_g}{C_b}=10$  for the worst case CB. The fourth column lists whether other CBs are also stressful (+) or not (-) for each given OD.

As listed in Table I, for OD-R4<sub>t</sub> and OD-R5<sub>t</sub> very low  $R_{cr}$  values were recorded. This underscores the high sensitivity to a resistive open on the pull-down transistor, which is on the current path for a read 0. This is also the case for OD-R4<sub>c</sub> and OD-R5<sub>c</sub> at the F Node side of the cell while performing a read 1 where BCm is discharged. In the presence of OD-R7<sub>t</sub> ... OD-R9<sub>t</sub> the cell exhibits a defect-free behavior irrespective of the CB used. These 3 ODs represent broken connections on the source, gate and drain of the pull-up transistor. For a read 0 in SRAM, when WL1 is activated, current flows through the NMOS pass transistor on the BT side, through the pull-down NMOS transistor to ground. Since this necessary current path for a read 0 does not pass through OD-R7<sub>t</sub> ... OD-R9<sub>t</sub>, the cell exhibits a defect-free behavior such that the sense amplifier gives a correct logic 1 output for all performed simulations. Here, a delay fault occurs, which takes place a while after the operation is performed. Special tests are used to detect these faults [11]. In the same way, OD-R7<sub>c</sub> ... OD-R9<sub>c</sub>

**TABLE I. Simulation results of the 18 ODs**

Defects Read 0	Worst CB	$R_{cr}$ of CB00 at $\frac{C_g}{C_b}=10$	Stressful CBs		
			01	10	11
OD-R1 <sub>t</sub>	00	93KΩ	-	-	-
OD-R2 <sub>t</sub>	00	2.43MΩ	-	+	-
OD-R3 <sub>t</sub>	00	45KΩ	-	+	-
OD-R4 <sub>t</sub>	00	2.28KΩ	+	+	+
OD-R5 <sub>t</sub>	00	1.54KΩ	+	+	+
OD-R6 <sub>t</sub>	00	38GΩ	+	+	+
OD-R7 <sub>t</sub>	-	-	-	-	-
OD-R8 <sub>t</sub>	-	-	-	-	-
OD-R9 <sub>t</sub>	-	-	-	-	-
Read 1	Worst CB	$R_{cr}$ of CB 11	00	01	10
OD-R1 <sub>c</sub>	11	61KΩ	-	+	+
OD-R2 <sub>c</sub>	11	2.08MΩ	-	+	+
OD-R3 <sub>c</sub>	11	29KΩ	-	+	+
OD-R4 <sub>c</sub>	11	8KΩ	+	+	+
OD-R5 <sub>c</sub>	11	3.86KΩ	+	+	+
OD-R6 <sub>c</sub>	11	207GΩ	+	+	+
OD-R7 <sub>c</sub>	-	-	-	-	-
OD-R8 <sub>c</sub>	-	-	-	-	-
OD-R9 <sub>c</sub>	-	-	-	-	-

**TABLE II. Single-cell static FFMs and their corresponding FPs**

Fault	FP	Fault	FP
SF <sub>0</sub>	< 0/1/- >	RDF <sub>0</sub>	< 0r0/1/1 >
SF <sub>1</sub>	< 1/0/- >	RDF <sub>1</sub>	< 1r1/0/0 >
TF <sub>0</sub>	< 0w1/0/- >	DRDF <sub>0</sub>	< 0r0/1/0 >
TF <sub>1</sub>	< 1w0/1/- >	DRDF <sub>1</sub>	< 1r1/0/1 >
WDF <sub>0</sub>	< 0w0/1/- >	IRF <sub>0</sub>	< 0r0/0/1 >
WDF <sub>1</sub>	< 1w1/0/- >	IRF <sub>1</sub>	< 1r1/1/0 >

on the F Node side exhibit a complementary behavior for a read 1 operation.

## V. Testing approach

This section describes the targeted fault models, and how these faults can be tested for, while taking CBs and BL coupling into consideration.

### A. Targeted fault models

In order to specify a certain memory fault, one has to represent it in the form of a *fault primitive (FP)*, denoted as  $\langle S/F/R \rangle$ .  $S$  describes the operation sequence that sensitizes the fault,  $F$  describes the logic level in the faulty cell ( $F \in \{0, 1\}$ ), and  $R$  describes the logic output level of a read operation ( $R \in \{0, 1, -\}$ ).  $R$  has a value of 0 or 1 when the fault is sensitized by a read operation, while ‘-’ is used when a write operation sensitizes the fault. For example, in the FP  $\langle 0w1/0/- \rangle$ , which is the up-transition fault,  $S = 0w1$  means that a  $w1$  operation is applied to a cell initialized to 0. The fault effect  $F = 0$  indicates that after performing  $w1$ , the cell remains in state 0. The output of the read operation ( $R = -$ ) indicates that there is no expected output for the memory.

*Functional fault models (FFMs)* can be defined as a non-empty set of FPs. The most important FFM class is single-cell static FFMs. Single-cell static FFMs consist of FPs sensitized by performing at most one operation on only

one faulty cell. Table II lists all single-cell static FFMs and their corresponding FPs. In total, the FFMs are state fault (SF), transition fault (TF), write destructive fault (WDF), read destructive fault (RDF), deceptive read destructive fault (DRDF) [2], and incorrect read fault (IRF).

Now, we present March SSS, which is an optimal march test that detects all single-cell static faults.

$$\text{March SSS} = \left\{ \begin{array}{ll} \Downarrow(w0); & \text{ME0} \\ \Downarrow(w1, w1, r1, r1); & \text{ME1} \\ \Downarrow(w0, w0, r0, r0) \} & \text{ME2} \end{array} \right.$$

Time complexity of this test is  $9n$ . All single-cell static faults are detected as follows. March element ME0 initializes the memory to 0. ME1 starts by sensitizing TF<sub>1</sub> during the first  $w1$  operation, then WDF<sub>1</sub> during the second  $w1$  operation. These two faults are detected during the first  $r1$  of ME1, which also sensitizes and detects SF<sub>1</sub>, RDF<sub>1</sub> and IRF<sub>1</sub>. Finally, the second  $r1$  operation of ME1 sensitizes and detects DRDF<sub>1</sub>. The complementary counterparts of these faults are sensitized and detected in the same way by ME2.

### B. Tests for BL coupling

In order to ensure the detection of a given type of faulty behavior in the presence of BL coupling, the test needs to ensure the most stressful coupling background  $\text{CB} = xxx$  as already described in Section III. This means that in case a test is supposed to detect a 1 from a given cell, then both neighboring cells on the same WL should contain a 1. The same is true when the test is supposed to detect a 0 from a given cell. For a solid (i.e., /0000.../1111...) and a row stripes (i.e., /0000...1111 or /1111...0000) data background, this means that each cell should retain the same logic value at the beginning and at the end of the march element that detects BL coupling.

Table III compares the *fault coverage (FC)* of a number of memory tests for single-cell static FFMs in Table II. The first column lists the tests, while the first row lists the FFMs. Under each FFM, the notation  $x/y$  is used.  $x$  shows whether the fault is detected (+) or not (-) by the listed test in the absence of BL coupling, while  $y$  shows if the fault is detected (+) or not (-) in the presence of BL coupling. FC lists the fault coverage of the tests without/with BL coupling for the FFMs (12 in all).  $TL$  is the *test length*.

For detecting simple single-cell static faults, one test that satisfies the BL coupling detection requirement is March SR =  $\{\Downarrow(w0); \Uparrow(r0, w1, r1, w0); \Uparrow(r0, r0); \Uparrow(w1); \Downarrow(r1, w0, r0, w1); \Downarrow(r1, r1)\}$  [14], since each accessed cell retains the same logic value at the beginning and at the end of each march element. However, this test does not detect all targeted FFMs. Another well-known test that satisfies the BL coupling detection requirement is Scan =  $\{\Downarrow(w0); \Downarrow(r0); \Downarrow(w1); \Downarrow(r1)\}$  [1], [3]. Again, Scan can only detect a limited number of single-cell static faults.

TABLE III. Comparison of tests fault coverage

Tests	SF <sub>0</sub>	SF <sub>1</sub>	TF <sub>0</sub>	TF <sub>1</sub>	WDF <sub>0</sub>	WDF <sub>1</sub>	RDF <sub>0</sub>	RDF <sub>1</sub>	DRDF <sub>0</sub>	DRDF <sub>1</sub>	IRF <sub>0</sub>	IRF <sub>1</sub>	FC	TL
Scan	+/-	+/-	-/-	+/-	-/-	-/-	+/-	+/-	-/-	-/-	+/-	+/-	7/0	4n
March SSS	+/-	+/-	+/-	+/-	+/-	+/-	+/-	+/-	+/-	+/-	+/-	+/-	12/0	9n
March SR	+/+	+/+	+/+	+/+	-/-	-/-	+/+	+/+	+/+	+/+	+/+	+/+	10/10	14n
March SS	+/-	+/-	+/-	+/-	+/-	+/-	+/-	+/-	+/-	+/-	+/-	+/-	12/0	22n
March SSSc	+/+	+/+	+/+	+/+	+/+	+/+	+/+	+/+	+/+	+/+	+/+	+/+	12/12	12n

One other test that detects all single-cell faults in the absence of BL coupling is March SS [13]. However, in the presence of BL coupling, the test fails to detect these faults. This is because March SS does not fulfill the requirement that the cell must retain the same logic value at the beginning and end of the march element. In the same way, our proposed March SSS test, which is an optimal test for detecting all single-cell static faults detects no faults when BL coupling is in effect. This is true since each march element in the test inverts the value of the cell, thereby preventing the *xxx* pattern from taking place.

Therefore, we present a more efficient test, March SSSc, that can detect all single-cell static faults both with and without the influence of BL coupling. This is done by modifying March SSS to March SSSc in the following way:

$$\text{March SSSc} = \left\{ \begin{array}{ll} \uparrow(w0); & \text{ME0} \\ \uparrow(w1, w1, r1, r1, w0); & \text{ME1} \\ \uparrow(w1); & \text{ME2} \\ \uparrow(w0, w0, r0, r0, w1) \} & \text{ME3} \end{array} \right.$$

The test should be performed using the checkerboard data background (i.e., /0101...1010...) or the column stripes (i.e., /0101.../0101...). March SSSc has a time complexity of  $12n$ , which is  $3n$  higher than March SSS due to the added 3 operations. This test ensures that each read operation is performed on a given cell when the neighboring cells contain exactly the same value by resetting the value of the tested cell at the end of ME1 and ME3. This ensures the worst-case conditions necessary for detecting single-cell static faults in the presence of BL coupling as follows. March element ME0 initializes the memory to 0. ME1 starts by sensitizing TF<sub>1</sub> during the first  $w1$  operation, then WDF<sub>1</sub> during the second  $w1$  operation. These two faults are detected during the first  $r1$  of ME1, which also sensitizes and detects SF<sub>1</sub>, RDF<sub>1</sub> and IRF<sub>1</sub>. The second  $r1$  operation of ME1 sensitizes and detects DRDF<sub>1</sub>. Thereafter, the content of the cell is reset to 0, thereby maintaining the worst-case detecting condition. The complementary counterparts of these faults are sensitized and detected in the same way by ME2 and ME3.

## VI. Conclusion

This paper discussed BL coupling and the way it impacts the faulty behavior of SRAM devices. The paper derived a model for BL coupling and estimated the amount of BL coupling voltage expected. The effects of coupling

were first analytically evaluated and then using a Spice memory simulation model. The results show that the coupling mechanisms require the coupling background *xxx* in neighboring cells to ensure the worst case coupling conditions, something that is important to take into consideration when designing SRAM tests. It has been shown that well-known tests such as Scan, can be used in combination with the solid or row stripes data background to detect worst-case BL coupling effects for a limited number of faults. This paper introduced March SSS that detects all single-cell static faults. March SSS is further modified to March SSSc to take worst-case CBs and BL coupling effects into consideration while detecting all the faults in question.

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