Trends and Challenges of SRAM Reliability in the Nano-scale Era

Seyab Khan Said Hamdioui
Delft University of Technology, Computer Engineering Laboratory
Mekelweg 4, 2628 CD Delft,The Netherlands
E-mail: {M.S.K.Seyab, S.Hamdioui}@tudelft.nl

***Abstract*—According to the International Technology Roadmap for Semiconductors (ITRS), embedded Static Random Access Memory (SRAM) will continue to dominate the area of System on Chips (SoCs) approaching 90% in the next 10 years. Therefore, SRAM reliability will have a significant impact on overall SoC reliability. This paper presents state-of-the-art transistor failure mechanisms and their impact on SRAM reliability parameters including cell stability, cell read failures, and cell access time failures. Furthermore, different techniques currently employed in industry, to mitigate the impacts of the failure mechanisms are presented. Finally, based on the current scaling trends reliability challenges of future transistors and embedded SRAM are discussed. The discussion concludes that the reliability challenges in future embedded SRAM will increase significantly.**

I. Introduction

In 1965 Moore predicted that in order to double on chip functionality, the transistor area should scale by 50% every 2 years with 20% design and process improvements [1]. Semiconductor industry turned this prediction into commitment by developing smaller, faster, and cheaper Metal Oxide Semiconductor (MOS) transistors. Currently, transistor has been scaled to nanometer range and it is predicted that 10nm transistor will be produced in the next decade [2]. Controlling fabrication of the minimum sized transistor is becoming a challenge. Process variations during the fabrication cause transistor parameters variations, higher defect densities, and new reliability failure mechanisms. These challenges not only impact transistor quality and yield, but also decrease its reliability. Since reliability brings degradations during operation [4], the reliability challenge demands designers to find its countermeasures in an early design stage.

SRAM has been used for a long time to push the state-of-the-art transistor in the semiconductor industry. The SRAM's transistors are scaled upto or near to the minimum available size to achieve the desired bit density, power, and performance. As a consequence, SRAM's transistors become more vulnerable to failures causing reliability problems [3]. The most critical reliability failure mechanisms for transistors are related to oxide layer [3], [4]. They consist mainly of:

- **Negative bias temperature instability (NBTI)**: In P-type MOS (PMOS) transistor negative oxide field produce interface traps at silicon-oxide layers (Si-SiO_2) interface. The interface traps increase the threshold voltage, degrades transconductance, and decreases the saturation current of the transistor.
- **Time dependent dielectric breakdown (TDDB)**: Electric field applied across the gate oxide layer degrades the oxide material and results in the formation of conducting path between the gate and the channel of the MOS transistor.
- **Hot Carrier Degradation (HCI)**: Energetic electrons and holes in the channel entering oxide layer produce interface states and oxide charges, which in turn degrade MOS transistor's threshold voltage, transconductance, and saturation current.

The oxide layer failures cause transistor malfunctions that express themselves at the SRAM circuit level, by degrading SRAM reliability parameters [5]. Examples are: (1) stability reduction (flipping of cell data due to voltages lower than nominal one), (2) unstable read (flipping of the cell data while reading), and (3) an increase in cell access time [3].

This paper discusses the reliability challenges of current and future embedded SRAM from transistor failure point of view. The analysis particularly focuses on the memory cell array since it typically occupies 70% of total SRAM resources. We review failure mechanisms related to transistor oxide layer and their impacts on SRAM cell reliability parameters. Furthermore, we survey major industrial techniques currently employed to mitigate such failure mechanisms. Finally, based on analysis of the current failure mechanism models, we present trends and challenges of SRAM reliability in future nano-scale MOS era. The outline of the rest of the paper is as follows. Section II reviews failure mechanisms related to MOS transistor oxide layer. Section III analyzes impacts of the failure mechanisms on SRAM cell reliability. Section IV reviews different industrial techniques currently employed to minimize impacts of the failure mechanisms. Section V describes reliability challenges of future embedded SRAM, and finally Section VI concludes the paper.

II. Oxide Layer Failure Mechanisms

Reliability failure mechanisms cause transistor failures during operation. Major classes of the failure mechanisms are environmental, process, and technology. The failures induced by environmental mechanisms are detected using parity checks, and corrected with error correcting codes [6],[13]. Process and technology related failure mechanisms include electrostatic discharge, latchup, and oxide layer failures. In nanoscale

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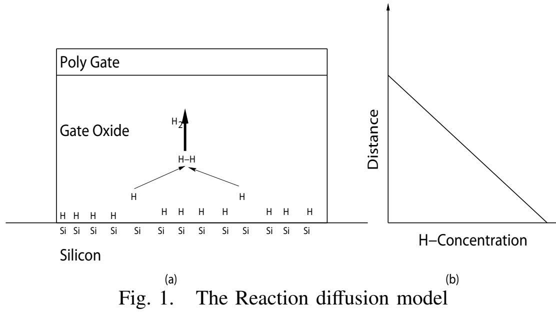

Fig. 1. The Reaction diffusion model

regime, the oxide layer mechanisms are/will be a threat to MOS transistor reliability [3],[4],[7]. The other mechanisms (electrostatic discharge, and latchup) are less critical and are mitigated using e.g. Silicon On Insulator (SOI) technology, protection circuits, and supply voltage scaling.

In the rest of the paper, we will focus on failure mechanisms related to oxide layer. As mentioned in Section 1, the oxide layer failure mechanisms include, NBTI, TDDB, and HCI.

A. Negative Bias Temperature Instability (NBTI)

NBTI mechanism refers to threshold voltage shift in PMOS transistor. Conditions for NBTI are negative oxide field in the range from 2 to 6MV/cm and temperature range from 100 to 250°C [8],[10]. The mechanism causes carriers mobility degradation, transconductance decrease, and threshold voltage increase [7]. Unlike the other mechanisms NBTI is self annealing, and PMOS recovers when the oxide field is removed.

NBTI mechanism has been explained by the Reaction Diffusion model (RD model) [9], which matches with the experimental verifications. According to the model negative oxide field breaks Silicon-Hydrogen (Si-H) bonds at the Si-SiO_2 interface, resulting in atomic hydrogens (H) and silicon dangling bonds (Si) as shown in Fig. 1(a). The H released convert to hydrogen molecules (H_2) and diffuse towards poly gate. The concentration of H_2 decreases with increasing distance from interface as shown in the Fig. 1(b). The Si produce interface traps (N_{IT}) that decrease PMOS carriers mobility, transconductance, and increase threshold voltage [10].

In RD model, it is assumed that the N_{IT} generation rate initially depends on Si-H bond breaking rate (forward reaction) and bond recovery rate (reverse reaction) [11]. The N_{IT} generation rate is as follows,

$$\frac{dN_{IT}}{dt} = k_f.(N_o - N_{IT}(t)) - k_r.N_{IT}(t).N_H^o(t), \tag{1}$$

where N_o is the initial number of Si-H bonds, k_f, and k_r are forward and reverse reaction rates, and N_H^o is the concentration of hydrogen at Si-SiO_2 interface. After some time, N_{IT} generation rate is limited by diffusion of H_2 towards poly gate [10]. Under such condition N_{IT} generation rate is,

$$\frac{dN_{IT}}{dt} = D_{H_2}.\frac{dN_H(x,t)}{dx}, \tag{2}$$

where D_{H_2} is the diffusion coefficient of H_2. The net interface traps generated by considering diffusion have been obtained by solving Eq.1 and 2 and are given by [11],

$$N_{IT}(t) = (0.5 \times k_f.N^o/k_r)^{1/2}.(D_{H_2}.t)^{1/6}. \tag{3}$$

The equation show that N_{IT} mainly depend upon the k_f, k_r, D_{H_2} and time exponent. The net threshold voltage V_{th} shift in PMOS due to N_{IT} generated can be expressed as [7],

$$\Delta V_t(t) \propto \frac{q}{C_{ox}}.(\Delta N_{IT}(t)), \tag{4}$$

where C_{ox} is oxide capacitance. Similarly mobility and transconductance dependence on N_{IT} are given in [13].

B. Time Dependent Dielectric Breakdown (TDDB)

In TDDB, oxide layer that isolates gate and substrate suffers from short circuit failure due to higher oxide field. The aftereffects of TDDB are loss of gate control on channel current, and increase in leakage currents [12], [18], [19].

TDDB is a two steps process consisting e.g. wear out and thermal runway. In the first step, charges accumulate inside oxide layer. The charges include interfacial oxide charges, fixed oxide charges, and oxide trapped charges [13] ,[14]. In the second step, the charges follow Fowler-Nordheim (FN) current [15], Direct tunneling [16], or Percolation theory [17] to initiate breakdown in oxide layer. The main TDDB models include the E-model, 1/E model, and power law model [13].

The E-model: The E-model states that TDDB is due to breaking of Si-Si bonds inside oxide layer [18]. Oxide field plays main role in breaking of the bonds. The Mean Time To Fail (MTTF) dependence on oxide field is given by [19],

$$MTTF = A.exp\,(-\gamma E)\,.exp\left(\frac{E_a}{kT}\right), \tag{5}$$

where A is a constant, γ is field acceleration parameter, E is oxide field, E_a is activation energy, k is Boltzmann constant, and T is absolute temperature. The E-model is frequently used and is consistent with experimental results upto oxide field of 4.8MV/cm [19]. However the model ignores role of tunneling current and is in-adequate for ultra-thin oxides [20].

The 1/E model: The model states that TDDB is driven by FN current in oxide layer [12], [18]. Electrons injected from the gate into oxide layer cause impact ionization to produce holes. Additional holes are injected from drain, that increase local oxide field and produce Stress Induced Leakage Current (SILC) [12]. MTTF depends inversely on SILC, while SILC depends linearly on field (E), thus the model gets the name (1/E) model. The model can be expressed as [19],

$$MTTF = A.exp\left(\frac{G}{E}\right).exp\left(\frac{E_a}{kT}\right), \tag{6}$$

where G is a constant. The model explains current driven degradation in FN region [18]. However, the model ignores direct tunneling current and thermal/diffusion activities that take place in oxide layer over time even in the absence of the oxide field [19].

Power Law Model: The power law model states that the MTTF of oxide layer (1.7-6.8nm) decreases inversely with the oxide leakage current at constant voltage stress [21]. The

MTTF dependence of the oxide leakage current I_{avg} can be written as,

$$MTTF = \frac{A}{I_{avg}^{n}}.exp\left(\frac{E_a}{kT}\right), \tag{7}$$

where A is a constant and n is thickness dependent variable. The value of n increases from 1 to about 10 when oxide thickness reduces from 6.8 to 1.7nm. The power law model is universal to fit in different oxide thickness, and even different conduction mechanisms, where E or 1/E models are less successful [17], [21].

C. Hot Carriers Degradation (HCI)

Hot carriers are energetic electrons and holes in NMOS channel that enter into oxide layer. The carriers entered into layer decrease NMOS transconductance, saturation current, and increase threshold voltage [13].

Hot carrier degradation is a two stage process. In the first stage, carriers gain energy in channel by impact ionization. Majority of them are collected at the drain, however few continue to gain energy. In the second stage, the energetic carriers overcome the oxide layer barrier and enter into oxide layer. The main modes of carrier entrance into oxide include, Channel Hot Electron (CHE) injection, Drain Avalanche Hot Carrier (DAHC) injection, and Secondary Generated Hot Carrier (SGHC) injection [34]. FN and direct tunneling current may also cause carrier injection especially at deep sub micron level [22]. Interface trap generation model explains hot carrier degradation.

Interface Trap Generation Model: Interface trap generation model is based on *lucky carriers* that gain sufficient energy and are directed toward oxide layer to generate interface traps. For a given drain source current I_{ds}, the interface traps generated ΔN_{it}, are given by [23],

$$\Delta N_{it} = C_1.\left[\frac{I_{ds}}{W}.exp\left(-\frac{\phi_{it,e}}{q.\lambda_e.E_m}t\right)\right]^n, \tag{8}$$

where W is the channel width, $\phi_{it,e}$ is the critical energy for electrons to create an interface trap, E_m is the channel lateral electric field, λ_e is the electron mean free path, t is time, and C_1 is the process dependent constant. The exponent n is variable with a the value, ranging from 0.5 to 1. The interface traps decrease gate hold on the channel carriers mobility, saturation current, and degrades NMOS threshold voltage [24].

III. SRAM Cell Reliability Failure Analysis

SRAM is mainly formed by an array of cells consisting four or six transistors. The most commonly used cell is a six transistor (6T SRAM) cell as shown in Figure 2. The word line WL controls M_5 and M_6 that enable charging/discharging paths between nodes V_L/V_R and bit lines BL/BR [26].

Gain of any cell MOS transistor (β) is given by $\mu_{eff}C_{ox}W/L$, where μ_{eff} is effective mobility, C_{ox} is oxide thickness, and L is length of MOS channel. An important parameter is cell ratio r, which is equal to ratio between β of the pull down (e.g, M_2) and the access transistor (e.g, M_5) i.e. $r = \beta_d/\beta_a$.

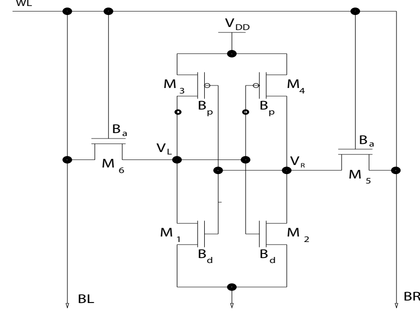

Fig. 2. 6T SRAM cell

Similarly, q is the β ratio between the pull up and access transistor i.e. $q = \beta_p/\beta_a$[27].

Oxide layer failure mechanisms of MOS transistor described in the previous section, express themselves at circuit level by affecting SRAM cell reliability. Major affects include signal noise margin (SNM) reduction, read stability failure, and access time failure. These affects are described in the next subsections.

A. Static Noise Margin (SNM)

SNM is the minimum dc noise voltage necessary to flip the state of a cell [27]. To analyze the impact of NBTI, SNM of a 6T SRAM [Figure 2] is derived analytically. It is assumed that M_1 and M_6 operate in saturation. While M_2 and M_5 remain in linear region. Under these conditions [27], SNM of the cell can be written as,

$$\begin{aligned} SNM &= V_{th}\left[\frac{1}{k+1}\right] + \left[\frac{V_{DD} - \frac{2r+1}{r+1}V_{th}}{1 + \frac{r}{k(r+1)}}\right] \\ &+ \left[\frac{V_{DD} - 2V_{th}}{1 + k\frac{r}{q} + \sqrt{\frac{r}{q}(1 + 2k + \frac{r}{q}k^2)}}\right], \end{aligned} \tag{9}$$

where k is a constant that mainly depend on cell ratios and V_{DD} is supply voltage. Second and third terms of the equation show that SNM degrades with V_T increase. Eq. 4 shows PMOS transistor V_{th} increase due to NBTI, that causes SNM reduction. The SNM reduction due to NBTI induced V_{th} increment is very significant during read operation and nearly follow $t^{1/6}$ law like degradation of a single transistor [5].

SNM of a cell can be graphically computed from the Voltage Transfer Curve (VTC). SNM is equal to the side length of larger square nested between curves of the two inverters as shown in the Fig. 3(a). VTC of an inverter changes with change in its input or output. In SRAM cell output of one inverter is connected to input of the other. TDDB event in PMOS or NMOS transistors of any inverter [Fig. 2] does not change VTC of that inverter (dotted line in Fig. 3(b) and solid line in Fig. 3(d)) but raises(lowers) the output voltage of the opposite inverter (solid line in Figure 3(b) and dotted in Fig. 3(d)) [31]. The variations disturb symmetry of the VTC curves of Fig.3(a) and hence degrade the SRAM cell SNM.

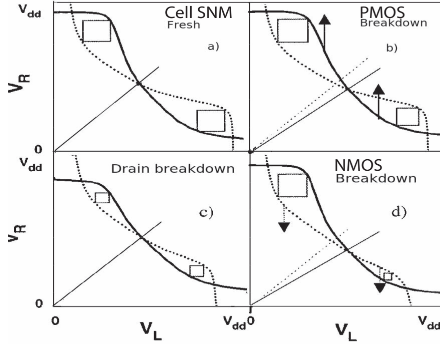

Fig. 3. Static noise margin of 6T SRAM cell and impacts of TDDB at different cell transistors [31]

HCI disturbs symmetry of VTC curves Fig. 3(a), causing cell SNM degradation. The degradation is due to increases threshold voltage and decreases drain current of access transistors (M_5 and M_6) and pull down transistors (M_1 and M_2). Generally HCI damage access transistors more due to bidirectional stresses during read and write operations, and reduce their drain currents [7]. The current reduction, decreases voltages at nodes V_L and V_R, resulting in SNM reduction.

B. Read stability failure

Read stability failure is the probability in SRAM that, the state of a cell will flip when word line is turned on during read operation [29]. In case of read failure voltage rise, V_{read}, at the storing node exceeds trip voltage, V_{trip}, of the opposite inverter and flips the original data [30]. The probability can be written as,

$$P_{RF} = P[V_{read} > V_{trip}]. \tag{10}$$

The main source of V_{read} increment is V_{th}'s mismatch of SRAM cell transistors. Major contributors to the V_{th} mismatch are Random Dopant Fluctuation (RDF) and NBTI induced PMOS threshold voltage increment. The threshold voltage deviation, σ_{Vt}, due to RDF is given by,

$$\sigma_{Vth} = \sigma_{Vth_o} \sqrt{\frac{L_{min}.W_{min}}{L.W}} \tag{11}$$

where σ_{Vth_o} is the standard deviation of V_{th} of the minimum sized transistor i.e. L_{min} and W_{min} in a certain technology. The time dependent NBTI induced V_{th} degradation [in Eq. 4], adds to the σ_{Vth}. The modified σ_{Vth} deviation increases V_{read}, resulting in increased read stability failure.

TDDB in MOS transistors cause SRAM cell read failure or false read depending on the breakdown transistor location. TDDB event in the access transistors decreases bit line differential voltage. When the cell is accessed during read operation, the voltage difference is below nominal value that results in read failure. TDDB event in inverter's transistors increases input of the opposite inverter. In worst case output of the opposite inverter changes, as a result false value is read during read operation [31].

Hot carrier degradation effects read operation in positive way. The threshold voltage increase of access transistors decrease read voltage V_{read}. When the cell is accessed during read operation, the lower V_{read} decreases probability of read failures.

C. Access Time Failure

The SRAM cell access time refers to the interval between activation of word line and development of pre-defined differential voltage between bit-lines. The access time failure occurs, if the access time of cell T_{access} of the cell is larger than the maximum tolerable limit T_{max}. The probability of access time failure P_{AF} can be expressed as, [30]

$$P_{AF} = P[T_{access} > T_{max}]. \tag{12}$$

The development of bit line differential voltage and T_{access} mainly depends on the strength of the pull down NMOS transistor, therefore NBTI induced V_T increment of the pull up PMOS transistors will have a negligible impact on the access time [32].

TDDB event in SRAM transistors changes bit line differential voltage and cell nodal voltages. Depending on breakdown location, SRAM cell T_{access} may increase or decrease. Breakdown event in M_5 and M_6 decreases time for BL and BR to reach the necessary voltage difference hence the cell becomes faster. On the other hand, TDDB event in the pull down transistors reduce difference between nodal voltages [V_L and V_R] and increases T_{access} of the cell [36].

HCI decrease saturation current in the access and pull down transistors. The reduction in access transistor's current is more significant, than pull down transistors, due to bi-directional stress during read and write operations [28]. Due to decrease in saturation current, the bit lines take longer times to discharge through access transistors, resulting in access time failure.

IV. Oxide Layer Failure Mechanisms Mitigation

In order to ensure reliable SRAM cell operation it is necessary to enhance immunity of individual transistors against all the failure mechanisms. Different techniques are employed in industry to mitigate NBTI, TDDB, and HCI and ensure SRAM reliability, as described below.

NBTI Mitigation

The magnitude of NBTI damage depends on the interface traps given by, $N_{IT} \propto (D_{H_2}t)^n$ [Eq.3]. Diffusion D_{H_2} inside oxide layer plays main role in the N_{IT} generation. Hydrogen diffusion in oxides is attenuated by using two methods. Firstly, amorphous oxides with longer hoping distances and timings for diffusing species are used as gate oxide material [10]. Diffusing hydrogens penetrate deeper into amorphous oxide traps and takes longer longer time to come out of the traps, hence delaying diffusion toward the gate, and mitigate NBTI [37]. Under these conditions, diffusion is,

$$D_{H2} = D_{oH_2}(\omega t)^{-a}. \tag{13}$$

The interface trap generated with amorphous oxides are obtained by modifying Eq.4, and is given by [37],

$$N_{IT} = (0.5 \times k_f N_o/k_R)^{1/2}(D_{H2}t)^{n'}, \quad (14)$$

where $n' = n - a/4$ with a=0.1-0.2, the power exponent reduces, which in turn causes less N_{IT} and hence increases immunity to NBTI degradation.

Secondly, nitrogen presence in oxide layer accelerates NBTI degradation due to ease of hydrogen diffusion in nitride oxide. The hydrogen diffusion is reduced by using plasma nitride instead of nitride oxide [38]. In plasma nitride the nitrogen concentration decreases while moving toward gate. The decreasing nitrogen concentration attenuates hydrogen diffusion toward gate and reduce NBTI degradation.

TDDB Mitigation

The oxide breakdown of MOS transistor is due to higher oxide field and pre-breakdown leakage. Currently, the problem related with higher field is alleviated by introduction of high-*k* dielectrics such as, oxinitrides or oxide-based compounds of Hafnium/Aluminum. To overcomes the high-*k* dielectrics compatibility issues with silicon substrate, a Hafnium layer (with dielectric constant 17-25 F/m and 0.5nm thickness) is introduced between silicon and high-*k* dielectric layer . The layer lowers leakage current, increases contact stability with Si, and decreases equivalent oxide thickness [35]. The pre-breakdown leakage current is due to non uniform structure of oxide layer. In order to avoid the current, oxide structure is fabricated more uniformly.

HCI Mitigation

The main source of carrier energy causing HCI is the channel lateral electric field. The field is more intense near the drain region of MOS transistor. Currently, the field E_m [Eq. 8] is reduced by introduction of a Lightly Doped Drain (LDD) region [25]. The region increases overlapping between gate and drain, which lead to a smaller value of E_m. The smaller E_m reduces the carrier injection into oxide layer. However, voltage drop in the LDD lateral resistance degrade current flow in the channel. In order to minimize the side effects, modified LDD structures are efficiently used [35].

V. Future Transistor and SRAM Reliability Challenges

Silicon oxide's scaling ability and process integration capability are key factors of MOS transistor and embedded SRAM reliability. However, silicon oxide fundamental limitations are projected to degrade transistor, and in turn SRAM reliability. Impacts of scaling on future transistor and SRAM reliability are described next.

Transistor Reliability Challenges

In future voltage scaling cannot follow oxide layer scaling due to threshold voltage constraints [10]. Therefore, field inside oxide layer will increase. The NBTI defining field dependent k_f parameter will increase significantly. The k_f can be expressed as [37],

$$k_f = k_o \times \sigma \times p \times T \times e^{-(E_{Fo} - a \times E_{ox})/k_B T}. \quad (15)$$

The k_f increment will be due to its three fold field dependence due to,

- The weaker bonds at the interface p will increase with field increment by following the relation $p \propto E_{ox}$.
- The holes will tunnel deeper in Si-H bond due to the transmission coefficient T increment. The coefficient will increase exponentially with oxide field by following, $T \propto exp^{\gamma_T E_{ox}}$ [37].
- The barrier potential E_{Fo} required to generate N_{IT} will decrease by factor $a \times E_{ox}$ with E_{ox} (as shown in Eq.15).

The above issues will increase the number broken bonds at $Si\text{-}SiO_2$ interface. Therefore, NBTI degradation will become more severe in the future.

In future transistors scaling will reduce oxide layer thickness and increase oxide field and hence TDDB, as described below,

- Oxide thickness will be a major issue, because Percolation model states that TDDB occurs if a conducting path is formed in oxide. For a given defect density the path formation will be more likely for thinner oxides [17].
- The TDDB activation energy E_a [in Eq. 5,6,7] will decreases with field increment. The decrease will follow E_a fundamental equation [33],

  $$E_a = E^*_{ao} - p_o(1 + L_\chi)E_{ox}, \quad (16)$$

  where E^*_{ao} is the activation energy in absence of applied field, p_o is the dipole movement, L_χ is the Lorentz factor, and E_{ox} is the oxide field. The equation shows that E_a will degrade with increasing E_{ox} and thus shorten MTTF.
- Direct tunneling J_{PF} will increases by one order of magnitude for every 0.2-0.3nm reduction in oxide thickness by following Poole Frenkel emission model [33],

  $$J_{PF} \propto Eexp\left[\frac{-q(\phi_B - \sqrt{qE/\pi\varepsilon})}{kT}\right] \quad (17)$$

  where ϕ_B is the trap barrier height, ε is the dielectric constant, and E is the applied field.

As technology scales down these issue will become more significant, and MTTF due to TDDB will take place earlier than expected.

In future, channel length will reduce significantly. Therefore, carriers will get energy from oxide as well as channel field E_{ch} i-e electric field between source edge and pinch off region. The E_{ch} will increase with decrease in channel effective length L_{eff} by following the relation [25],

$$E_{ch} = (V_{dsat} - V_s)/L_{eff} = \frac{V_{dsat} - V_s}{\sqrt{3X_{OX}X_j'}}, \quad (18)$$

where X_j' is a constant and X_{OX} is the gate length. These factors will increase carrier energy and they will easily cross the oxide layer barrier to increase the hot carrier degradation in future MOS transistors [25].

In future transistors the above issues will be mitigated by introduction of new material e.g. high K, silicon nitrides,

strained silicon, and process improvement. Research on the new materials and process improvement will introduce new reliability challenges. The challenges will be either introduction of new reliability failure mechanisms or more complex analysis and mitigation techniques of the known mechanisms. Analyzing the failure mechanisms and their mitigation will ensure ultra scaled, but yet reliable transistors in the future.

SRAM Reliability Challenges

From the previous subsection we conclude that as we look forward to the next 5-10 years of MOS transistor scaling, the transistor reliability threats will increase. As a consequence, SRAM reliability is becoming a major challenge,

- Sensitivity of SRAM cell SNM will be a major issue. The SNM will shrink significantly and will be more sensitive to transistor leakage, mismatching, and process variations. Transistors degradation due to reliability issues like, NBTI, TDDB, and HCI will distrub transistor matching and degrade the SNM.
- NBTI and HCI induced V_{th} shift as well as TDDB stimulated leakage currents will significantly effect the read stability and will cause SRAM failure.
- The SRAM speed and compatibility with other standard logic processes will also be a challenge. HCI and frequent TDDB events in the access and pull down transistors will significantly effect the SRAM access time, therefore widening speed gape.

In order to mask the transistor failures and their impact on SRAM reliability it is necessary to come up with the novel solutions at transistor and/or circuit level e.g.,

- Continuous monitoring of the SRAM circuit by sensing e.g. current, temperature, or speed.
- Optimized solutions for on-line correction and/or repair and/or reconfiguration.

VI. Conclusion

In this paper, we reviewed state-of-the-art reliability challenges of embedded SRAM from the viewpoint of transistor failures. The impacts of oxide layer failure mechanisms including NBTI, TDDB, and HCI on several SRAM cell reliability parameters including SNM, read failure, and access time are discussed. These mechanisms significantly degrade SRAM cell reliability parameters. Oxide layer scaling in future will accelerate transistor reliability and will have a large impact on SRAM reliability. As the failure rate during the lifetime of SRAM is expected to increase, new measures need to be taken. For instance on-line monitoring schemes to detect reliability problems on time and prevent catastrophic errors are required. Moreover, techniques and schemes for on-line correction and/or repair to recover and/or replacement with redundant hardware have to be developed to ensure reliable SRAM operation thorought whole lifetime of the application.

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