Detecting Memory Faults in the Presence of Bit Line Coupling in SRAM Devices

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Abstract

The fault coverage of otherwise efficient memory tests can be dramatically reduced due to the influence of bit line coupling. This paper, analyzes the impact of parasitic bit line coupling and neighborhood coupling data backgrounds on the faulty behavior of SRAMs. It investigates and determines the worst case coupling backgrounds required to induce worst case coupling effects, and validates the analysis through defect injection and circuit simulation of all possible spot defects in the SRAM cell array. The paper clearly demonstrates the inadequacies and limitations of several industrial tests in detecting memory faults in the presence of bit line coupling. Finally, it shows how to detect all single-cell and two-cell faults, both in the absence and in the presence of bit line coupling for any possible spot defect.

Keywords: Memory tests, parasitic capacitance, bit line coupling, defects, SRAMs.

I. Introduction

Undesired connections can cause several faults in the memory circuit. Due to the continuous decrease of cell area, the amount of coupling noise and sensitivity to defects has continued to increase.

Bit line (BL) coupling results in the development of small coupling voltages on adjacent BLs, which for example, can influence proper sense amplifier operation. This has a huge impact on the faulty behavior of the memory, potentially causing readily detectable memory faults to become undetectable with several tests. BL coupling and the resulting crosstalk noise is strongly considered as a limiting factor in designing high speed, low power SRAM devices [6].

Research on the impact of parasitic capacitance on the faulty behavior of SRAMs has up till now addressed faults in peripheral memory circuits as well as address decoders [14], [22], [12], [3], [4]. BL twisting as well as BL segmentation (global and local bit lines) have been proposed to prevent cross talk noise and increase the *signal-to-noise ratio* [7], [8]. Despite these solutions, BL coupling remains a problem due to the expensive implementation cost of such solutions.

This paper presents a detailed and comprehensive evaluation of the SRAM faulty behavior under the influence of both parasitic capacitance between BLs and varied neighborhood data. The paper presents the conditions necessary to ensure proper detection of memory faults, while taking BL capacitive coupling into consideration and clearly shows how BL coupling can reduce the fault coverage of well-known memory tests. Finally, it shows how to detect all single-cell and two-cell static faults in the presence of BL coupling.

The rest of the paper is organized as follows. Section II shows how to analytically evaluate BL coupling capacitance. Section III presents the theoretical framework and analysis of the impact of BL coupling on the faulty behavior of the memory and identifies the worst case coupling data backgrounds. Section IV defines defects and their locations in the memory, while in Section V Spice simulations are used to validate the analysis for all spot defects, and the results discussed. Section VI shows how the fault coverage of memory tests can decrease as a result of BL coupling, and thus shows how to detect all single-cell and two-cell faults in the absence and presence of BL coupling. Section VII gives the conclusions.

II. Modeling of BL coupling

An electrical Spice SRAM model is presented in Figure 1, which is used in the evaluation of BL coupling effects in this paper. The model transistor parameters are based on the 65nm BSIM4 model card as described by the Predictive Technology Model [23]. The memory has a 3x3 cell array to enable simulation of all neighboring coupling effects. These cells are connected to three BL pairs: *left BL (BLl)*, which has the *left true (BTl)* and *left complementary (BCl)* BLs, *middle BL (BLm)*, which has the *middle true (BTm)* and *complementary (BCm)* BLs, and the *right BL (BLr)*,

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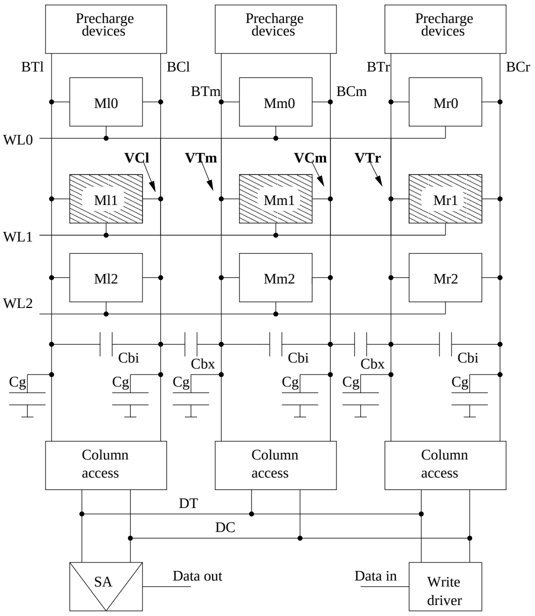

Fig. 1. SRAM electrical Spice model

which has *BTr* and *BCr* BLs.

Each *word line (WL)* or cell array row in the model has 3 cells: left (l), middle (m) and right (r); while each BL or cell array column has 3 cells numbered as 0, 1 and 2. The cell in the center of the array (i.e., memory cell Mm1) is the faulty cell under analysis. Each BL is also connected to precharge devices to ensure proper initial BL voltages. Read/write access to different BLs is controlled by the column access devices, which ensure that only one BT gets connected to the *true data line (DT)* and only one BC gets connected to the *complementary data line (DC)* during each memory operation. The model also contains a *sense amplifier (SA)* to inspect the read output (data out), as well as a write driver to drive input data (data in).

The total BL capacitance (C_t) is divided into three components: internal coupling to complementary BL (C_bi), external coupling to a neighboring BL (C_bx) and an inherent BL capacitance to ground (C_g) composed of coupling to all other parts of the memory (cells, WLs, substrate, etc). This is expressed as:

$$C_\text{t} = C_\text{bi} + C_\text{bx} + C_\text{g} \tag{1}$$

The exact values of these capacitance depend on the layout of the memory and its manufacturing technology. In general, the value of C_g accounts for a large portion of C_t. In literature, reported C_g/C_t ratios range from 40% to over 90% [9]. On the other hand, due to the symmetry of the layout implementation of the BLs, the values of C_bi and C_bx are rather close to each other, and therefore we consider them to be equal (C_bi = C_bx = C_b) such that:

$$C_\text{t} \approx 2C_\text{b} + C_\text{g} \tag{2}$$

This is also because BT and BC are not distinguishable at design time since they are identical, and only become BT or BC due to their connections, which is inherent in the design.

In this paper, we focus on read operations. The reason is that the read operations are more sensitive to the impact of coupling than write operations.We also assume that BL twisting is not used in the memory under analysis. During a read operation, the WL accesses the cell and connects it to the precharged BLs. Based on the value stored in the cell, a voltage differential develops on the BLs that the sense amplifier subsequently attempts to detect. The presence of C_b causes neighboring BLs to influence the voltage development during a read. If we assume that a defective BL is totally floating, while the neighboring BL develops a voltage *V*, then the amount of coupling voltage (ΔV) induced on the floating BL can be expressed as:

$$\frac{\Delta V}{V} \approx \frac{1}{(C_\text{g}/C_\text{b}) + 1} \tag{3}$$

III. Theoretical framework and analysis

In this section, we present a complete theoretical analysis of the impact of BL coupling. Section III-A analyzes the effect of BL coupling due to the data in the neighboring cells of a given victim, while Section III-B presents the fault models analyzed.

A. BL coupling effects

When a specific victim cell is accessed, the only neighboring cells also being accessed at the same time are those that belong to the same row as the victim, that is, those cells connected to the same WL as the victim cell. As shown in the highlighted portion of the model in Figure 1, when the middle memory cell (Mm1) is accessed, the only other influential cells are the left memory cell (Ml1) and the right memory cell (Mr1) connected to the same WL1.

For this reason, our work is focused on the effect of coupling and varied data in Ml1 and Mr1 on the faulty behavior of Mm1, in the presence of spot defects.

Now, we explain the impact of the data contents of the neighboring cells, Ml1 and Mr1, referred to as *coupling backgrounds (CBs)* on the sensing of Mm1.

If cell Ml1 contains a 1, then when it is accessed, it pulls BCl down by some voltage VCl. Due to BL coupling, this in turn pulls the voltage on BTm down by VTm (Figure 1). Thus, the presence of a logic 1 in Ml1 makes the detection of logic 1 in Mm1 more difficult while it makes the detection of logic 0 easier. On the other hand, having a 0 in cell Ml1 does not modify the voltage on BCl, which in turn does not modify the voltage on BTm. In brief,

- In order to maximally stress logic 1 in Mm1, Ml1 must contain a logic 1.
- In order to stress a logic 0 in Mm1, Ml1 must *not* contain a logic 1, thereby requiring a stored logic 0 instead.

If cell Mr1 contains a 0, then when it is accessed, it pulls BTr down by some voltage VTr. Due to BL coupling, this in turn pulls the voltage on BCm down by VCm (Figure 1). Thus, the presence of a logic 0 in Mr1 makes the detection of logic 0 in Mm1 more difficult while it makes the detection of logic 1 easier. On the other hand, having a 1 in cell Mr1 does not modify the voltage on BTr, which in turn does not modify the voltage on BCm. In brief,

- In order to maximally stress logic 0 in Mm1, Mr1 must contain a logic 0.
- In order to stress a logic 1 in Mm1, Mr1 must *not* contain a logic 0, thereby requiring a stored logic 1 instead.

In conclusion, the most stressful background to detect parasitic BL coupling in an SRAM cell containing a logic 1 is 11 in both neighboring cells connected to the same WL (we refer to this as CB11). In contrast, the most stressful background to detect a logic 0 is CB00. These are referred to as *worst case coupling backgrounds (WCB).*

B. Functional Fault Models

In this paper, single-cell and two-cell faults are targeted. This section describes these functional fault models, and their fault primitives as already presented in [21].

In order to specify a certain memory fault, one has to represent it in the form of a *fault primitive (FP)*, denoted as $< S/F/R >$. S refers to a value or the operation sequence that sensitizes the fault, F describes the logic value in the faulty cell ($F \in \{0, 1\}$), and R describes the logic output value of a read operation ($R \in \{0, 1, -\}$). R has a value of 0 or 1 when the fault is sensitized by a read operation, while '$-$' is used when a write operation sensitizes the fault. For example, in the FP $< 1w0/1/- >$, which is the down-transition fault, $S = 1w0$ means that a $w0$ operation is applied to a cell initialized to 1. The fault effect $F = 1$ indicates that after performing $w0$, the cell remains in state 1. The output of the read operation (R = $-$) indicates that there is no expected output for the memory.

Functional fault models (FFMs) can be defined as a non-empty set of FPs. Two important FFM classes are the *single-cell* and *two-cell static* FFMs.

TABLE I. Single-cell static FFMs and their corresponding FPs

Fault	FP	Fault	FP
SF_0	$< 0/1/- >$	RDF_0	$< 0r0/1/1 >$
SF_1	$< 1/0/- >$	RDF_1	$< 1r1/0/0 >$
TF_0	$< 0w1/0/- >$	$DRDF_0$	$< 0r0/1/0 >$
TF_1	$< 1w0/1/- >$	$DRDF_1$	$< 1r1/0/1 >$
WDF_0	$< 0w0/1/- >$	IRF_0	$< 0r0/0/1 >$
WDF_1	$< 1w1/0/- >$	IRF_1	$< 1r1/1/0 >$

TABLE II. Two-cell static FFMs and their corresponding FPs ($x, y \in \{0, 1\}$)

#	FFM	FP = $<S_a; S_v/F/R>$
1	CF_{st}	$<0; 0/1/->$, $<0; 1/0/->$, $<1; 0/1/->$, $<1; 1/0/->$
2	CF_{ds}	$<xwy; 0/1/->$, $<xwy; 1/0/->$, $<xrx; 0/1/->$, $<xrx; 1/0/->$
3	CF_{wd}	$<0; 0w0/1/->$, $<1; 0w0/1/->$, $<0; 1w1/0/->$, $<1; 1w1/0/->$
4	CF_{tr}	$<0; 0w1/0/->$, $<1; 0w1/0/->$ $<0; 1w0/1/->$, $<1; 1w0/1/->$
5	CF_{drd}	$<0; 0r0/1/0>$, $<1; 0r0/1/0>$, $<0; 1r1/0/1>$, $<1; 1r1/0/1>$
6	CF_{ir}	$<0; 0r0/0/1>$, $<1; 0r0/0/1>$ $<0; 1r1/1/0 >$, $<1; 1r1/1/0>$
7	CF_{rd}	$<0; 0r0/1/1>$, $<1; 0r0/1/1>$, $<0; 1r1/0/0>$, $<1; 1r1/0/0>$

1) ***Single-cell static FFMs****:* These consist of FPs sensitized by performing at most one operation on only one faulty cell. Table I lists all single-cell static FFMs and their corresponding FPs. In total, the FFMs are state fault (SF), transition fault (TF), write destructive fault (WDF), read destructive fault (RDF), deceptive read destructive fault (DRDF) [2], and incorrect read fault (IRF).

2) ***Two-cell static FFMs****:* These consist of FPs that are sensitized by performing an operation on a cell *a*, referred to as an *aggressor*, such that a fault is sensitized on a *victim* cell, *v*. FPs of two-cell static faults can be represented as follows $< S/F/R >$ = $<S_a; S_v/F/R>_{a,v}$. S_a and S_v denote the sensitizing operation or state of *a* and *v*. The second column of Table II enumerates all two-cell static FFMs, namely, state coupling faults (CF_{st}), disturb coupling faults (CF_{ds}), transition coupling faults (CF_{tr}), write destructive coupling faults (CF_{wd}), read destructive coupling faults (CF_{rd}), incorrect read coupling faults (CF_{ir}) and deceptive read destructive coupling faults (CF_{dr}). Their corresponding FPs are listed on the third column. Rows of the third column show the operations on *v* when *a* is in a given state. In addition, the rows of CF_{ds} shows the operations performed on *a*, with *v* in a given state.

IV. Location of spot defects

Spot defects can be classified as opens, bridges or shorts, and can cause faults in the memory cell array.

TABLE III. Description of open defects on the T & F Node sides

OD	**Position on T Node side**
$R1_t$	Pass transistor connection to BL broken (drain)
$R2_t$	Pass transistor connection to WL broken (gate)
$R3_t$	Pass transistor connection to T-Node broken (source)
$R4_t$	NMOS down transistor connection to T-Node broken (drain)
$R5_t$	NMOS down transistor connection to ground broken (source)
$R6_t$	NMOS down transistor connection to F-Node broken (gate)
$R7_t$	PMOS up transistor connection to T-Node broken (drain)
$R8_t$	PMOS up transistor connection to F-Node broken (gate)
$R9_t$	PMOS up transistor connection to Vdd broken (source)
OD	**Position on F Node side**
$R1_c$	Pass transistor connection to BL broken (drain)
$R2_c$	Pass transistor connection to WL broken (gate)
$R3_c$	Pass transistor connection to F-Node broken (source)
$R4_c$	NMOS down transistor connection to F-Node broken (drain)
$R5_c$	NMOS down transistor connection to ground broken (source)
$R6_c$	NMOS down transistor connection to T-Node broken (gate)
$R7_c$	PMOS up transistor connection to F-Node broken (drain)
$R8_c$	PMOS up transistor connection to T-Node broken (gate)
$R9_c$	PMOS up transistor connection to Vdd broken (source)

TABLE IV. Position of shorts

Shorts within the cell	**Position**	**complement**
SHC-R1	T_m - V_{DD}	SHC-$R1_c$: F_m - V_{DD}
SHC-R2	T_m - GND	SHC-$R2_c$: F_m - GND
Shorts at BL	**Position**	**complement**
SHB-R1	BT_m - V_{DD}	SHB-$R1_c$: BC_m - V_{DD}
SHB-R2	BT_m - GND	SHB-$R2_c$: BC_m - GND
Shorts at WL	**Position**	**complement**
SHW-R1	WL - V_{DD}	
SHW-R2	WL - GND	

TABLE V. Position of bridges

Bridges within the cell				
BrDC	position	complement	interchange	int. comp
BrDC-R_1	T_m - F_m			
BrDC-R_2	T_m - BT_m	F_m - BC_m		
BrDC-R_3	T_m - BC_m	F_m - BT_m		
BrDC-R_4	T_m - WL1	F_m - WL1		
BrDC-R_5	BT_m - BC_m			
BrDC-R_6	BT_m - WL1	BC_m - WL1		
Bridegs between cells on the same row (left side)				
BrDL	BrDL	complement	interchange	int. comp
BrDL-R_1	T_l - T_m	F_l - F_m		
BrDL-R_2	T_l - F_m	F_l - T_m		
BrDL-R_3	T_l - BT_m	F_l - BC_m	BT_m - T_r	BC_l - F_m
BrDL-R_4	T_l - BC_m	F_l - BT_m	BC_1 - T_m	BT_1 - F_m
BrDL-R_5	BT_l - BT_m	BC_l - BC_m		
BrDL-R_6	BT_l - BC_m		BC_l - BT_m	
Bridges between cells on the same row (right side)				
BrDR	BrDR	complement	interchange	int. comp
BrDR-R_1	T_m - T_r	F_m - F_r		
BrDR-R_2	T_m - F_r	F_m - T_r		
BrDR-R_3	T_m - BT_r	F_m - BC_r	BT_m - T_r	BC_m - F_r
BrDR-R_4	T_m - BC_r	F_m - BT_r	BC_m - T_r	BT_m - F_r
BrDR-R_5	BT_m - BT_r	BC_m - BC_r		
BrDR-R_6	BT_m - BC_r		BC_m - BT_r	
Bridges between cells on the same column				
BrDU	BrDU	complement	interchange	int. comp
BrDU-R_1	T_m - T_{m0}	F_m - F_{m0}		
BrDU-R_2	T_m - F_{m0}	F_m - T_{m0}		
BrDU-R_3	T_m - WL_{m0}	F_m - WL_{m0}	WL_m - T_{m0}	WL_m - F_{m0}
BrDU-R_4	WL_m - WL_{m0}			
Bridges between cells on the same diagonal				
BrDG	BrDG	complement	interchange	int. comp
BrDG-R_1	T_m - T_{r0}	F_m - F_{r0}		
BrDG-R_2	T_m - F_{r0}	F_m - T_{r0}		

A. Open defects

Open defects (OD) are usually caused by broken lines or particle contamination that results in increasing line resistivity at the open position. Opens within the cell [19] and their complements are listed in Table III. Two defects are said to be *complementary, (c)* when their locations are symmetrical to each other within the cell, with the difference being that all 1s are replaced with 0s and vice versa.

B. Short defects

Short defect (SH) can be defined as a connection between one memory node and V_{DD} or GND. Shorts in the memory cell array can generally be classified as shorts within the cell, shorts at BLs and shorts at WLs. A list of shorts is given in Table IV.

C. Bridge defects

Bridges (BrD) can connect any arbitrary pair of nodes. We identify two categories of bridges namely, bridges within the cell and bridges between cells. Nodes need to be located close to each other in a way that bridges can be categorized in this way [13], [20].

*1) **Bridges within the cell:*** BrDs within the cell connect two nodes of the same cell, and this includes the pair of BLs (i.e., BT and BC) and WL to which the cell is connected. Each cell consists of five nodes, {True node (T), False node (F), BT, BC, WL}. Thus, the number of bridges resulting from pairing the listed nodes is 10 as enumerated in Table V, denoted as *BrDC (t)*. BrDCs with complementary behavior have been listed on the same row.

However, despite the symmetry that exists between the T and F nodes in SRAM cells, complementary defects can exhibit different behaviors [18], therefore full simulations for each BrDC and the corresponding complement have been simulated and analyzed.

*2) **Bridges between cells:*** BrDs between cells connect nodes of adjacent cells, which include BL pairs and WL to which they are connected. BrDs between the cells include BrDs between cells on the *same row*, BrDs between cells on the *same column*, and BrDs between cells on the *same diagonal*.

Cells on the same row

For adjacent cells on the same row, first we consider all possible BrDs between Ml1 and Mm1, and refer to them as BrDLs, and next we consider all possible BrDs between Mm1 and Mr1, and refer to them as BrDR. Table V lists all BrDs. It lists the BrDs on the first column, and indicates the BrD position on the second column. The third column lists the complementary behavior, the fourth column lists the interchange behavior *(i)*, while the last column lists the interchange complement*(ic)*. An interchange behavior (involving two cells) occurs if the faulty behavior of one of the cells is similar to that of the other cell, such that the difference is an interchange of the aggressor and the victim.

To determine the full space of BrDL, each cell consists of five nodes, where the nodes of cell Ml1 are $\{T_l, F_l, BT_l, BC_l, WL1\}$, and nodes of cell Mm1 are $\{T_m, F_m, BT_m, BC_m, WL1\}$.

However, because WL1 is common to both Ml1 and Mm1, only $\{T_l, F_l, BT_l, BC_l\}$ and $\{T_m, F_m, BT_m, BC_m\}$ can form bridges. Thus, the possible number of BrDLs is 16. In the same way, the possible number of BrDRs between Mm1 and Mr1 is also 16 as shown in Table V.

Cells on the same column

These are denoted as BrDUs. To determine all possible BrDUs we consider BrDs between Mm0, Mm1. Both Mm0 and Mm1 contain five nodes each. The nodes of cell Mm0 are $\{T_{m0}, F_{m0}, BT_{m0}, BC_{m0}, WL0\}$, while the nodes of cell Mm1 are $\{T_m, F_m, BT_m, BC_m, WL1\}$. Since Mm0 and Mm1 share the same BL, only 9 BrDUs exist between Mm0 and Mm1. Note that BrDs between the nodes T_m and F_m have not been included. The reason is that they have been considered earlier and included while determining BrDCs. The lower part of Table V lists all BrDUs.

Cells on the same diagonal

We denote adjacent cells on the same diagonal as BrDGs. Here, we consider all possible BrDGs between diagonal cells such as Mm1 and Mr0. Both Mm1 and Mr0 consists of five nodes, where the nodes of cell Mm1 are $\{T_m, F_m, BT_m, BC_m, WL1\}$, and nodes of cell Mr0 are $\{T_{r0}, F_{r0}, BT_{r0}, BC_{r0}, WL0\}$. Since BrDs connecting WL and BLs of Mm1 have been already considered, only four bridges are derived for BrDGs as listed also in the lower part of Table V.

V. Simulation analysis of defects

In this section, simulation results for bridges, opens and shorts are discussed. For each evaluated defect, all scenarios are considered namely, read 0 and read 1 operations performed using all CBs for $\frac{C_g}{C_b}$ values. The value of C_g is considered to be a typical 500fF [10], while $\frac{C_g}{C_b}$ values are modified for each simulation in the range $1 \leq C_g/C_b \leq 20$ [15], with C_b values as 500fF, 100fF, 50fF, 30fF and 25fF.

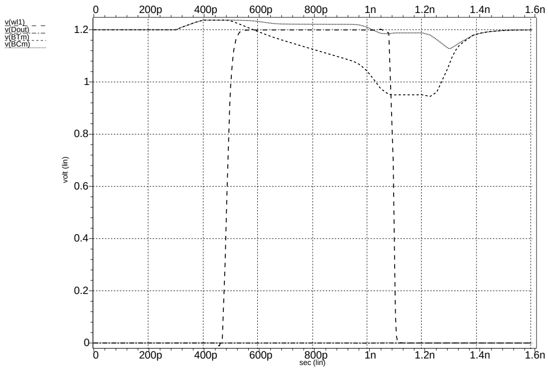

Fig. 2. Defect-free read 0 with BL coupling

In general, both the value of the injected resistance for the defect, R_{ir}, as well as the amount of the coupling capacitance influence BL voltage differential and therefore decide the eventual output logic value at the sense amplifier. $R_{ir} \in \{ R_{od}, R_{br}, R_{sh}\}$, and is the injected resistance for open, bridge or short defects. This creates a space of possible ($\frac{C_g}{C_b}$, R_{ir}) values, where the defective cell can either function properly or fail. The specific resistive value in the R_{ir} range, demarcating the pass and fail regions is referred to as the *critical resistance (R_{cr})*.

Our analysis is based on detecting the differences in behavior between a properly functional circuit and its behavior after each defect has been injected.

A. Simulation analysis of bridge defects

In this section, analysis of the bridges are discussed. The injected resistances for each bridge can vary within the range of $0 \leq R_{br} \leq \infty$.

*1) **Simulation analysis of BrDC-R1**:* Here, we analyze the simulated results for read operations for BrDC-R1 using all CBs and $\frac{C_g}{C_b}$ values.

BrDC-R1: Read 0 at Mm1

BrDC-R1_t is injected between the T and F nodes of cell Mm1. In order to clearly demonstrate the impact of BL coupling and influence of CBs, we simulate three scenarios as follows. First, a defect-free read 0 on Mm1 depicted in Figure 2, then, a defective read 0 on Mm1 with CB00 as shown in Figure 3 and a defective read 0 on Mm1 with CB10 as depicted in Figure 5. Once WL1 is accessed, a differential voltage starts to develop between BTm and BCm, which is detected by the sense amplifier. This voltage is amplified as a full 0, thereby leaving the data out (Dout) line at 0.

Figure 3 shows a read 0 performed on Mm1, when bridge BrDC-R1_t is injected with BL coupling ($\frac{C_g}{C_b}$ = 10),

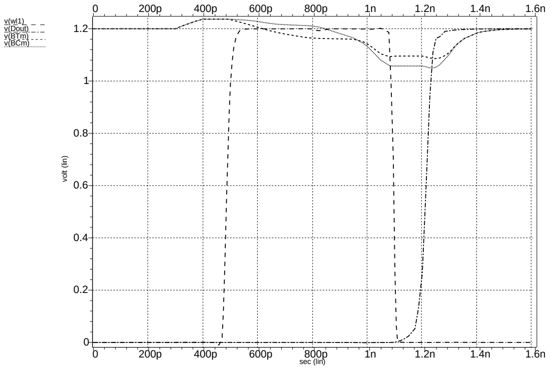

Fig. 3. Read 0 with BrDC-R1$_t$ and BL coupling, at CB00, $\frac{C_g}{C_b}$ = 10 and R_{br}=18.40KΩ

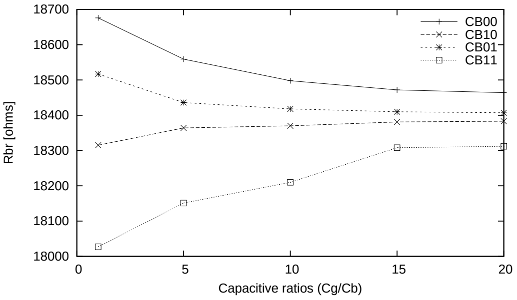

Fig. 4. Pass and fail regions for read 0 with BrDC-R1$_t$

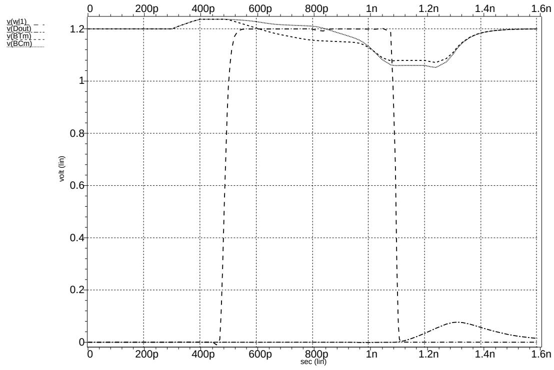

Fig. 5. Read 0 with BrDC-R1$_t$ and BL coupling, at CB10, $\frac{C_g}{C_b}$ = 10 and R_{br}=18.40KΩ

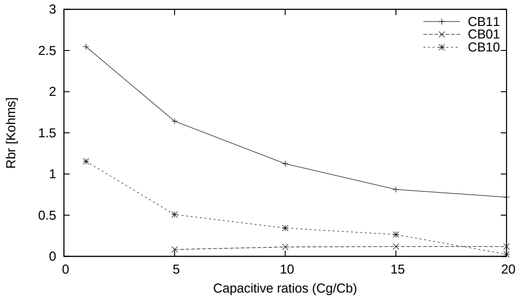

Fig. 6. Pass & fail regions for read 1 with BrDC-R1

at CB00. The value of the injected bridge is R_{br}=18.40KΩ.

At this particular R_{br} value, comparing Figure 3 with Figure 2, readily shows a number of differences. First, the differential voltage developing on the BLs is significantly reduced in this case as shown in Figure 3 between $t = 0.4$ ns and $t = 1.4$ ns, thereby making it extremely difficult for the sense amplifier to identify the correct stored value in the cell. Thus, the BL coupling voltage from neighboring cells causes the sense amplifier to detect an incorrect logic 1 in the cell rather than a logic 0, as shown by the Dout signal in the figure.

For all simulated $\frac{C_g}{C_b}$, R_{cr} of BrDC-R1 is plotted and depicted as curve *CB00* in Figure 4. In the plot, the $x-$axis indicates $\frac{C_g}{C_b}$, while the $y-$axis represents R_{br} values. The curve in the figure divides the ($\frac{C_g}{C_b}$, R_{br}) plane into two regions. The region above the curve is the *pass* region while the region below is the *fail* region. Note that only CBs for which fails have been recorded are included in the plot.

As curve CB00 in Figure 4 indicates, the fail region expands gradually as the amount of coupling capacitance increases. Thus, at resistances above R_{cr}, the cell exhibits a defect-free behavior, whereas at resistances below R_{cr}, the faulty behavior manifests.

Likewise, using CB01, due to BrD at 18.40KΩ in the memory cell, the differential voltage on BLs is very limited and the differential voltage is biased towards detecting an incorrect logic 1 in the cell. However, using other CBs (10 and 11) corrects the faulty behavior and prevents a fail from being detected, as indicted by the Dout signal in Figure 5 for CB10. Thus, WCB is CB00 due to the high R_{br} value at which CB00 necessitated a fail.

BrDC-R1: Read 1 at Mm1

For a read 1 using CB11, the differential voltage developing on BLs is significantly reduced in the defective case between $t = 0.4$ ns and $t = 1.4$ ns. An increase in coupling capacitance causes the sense amplifier to record an incorrect logic 0 instead of a logic 1. Plots of R_{cr} at varying $\frac{C_g}{C_b}$ for BrDC-R1 for CB11 is shown in Figure 6 depicted by curve *CB11*.

Coupling due to both CBs 01 and 10 also yielded incorrect read outputs as depicted by curves CB01 and CB10. Thus, CBs 01, 10 and 11 caused a fail, while CB00 rather corrects the faulty behavior. CB00 is not included in Figure 6 since it did not necessitate a fail. Thus, CB11 is the WCB because it returned R_{cr} values higher than the rest of the CBs.

*2) **Analysis of all other BrDCs, BrDL and BrDRs:*** In this section, we present a behavioral summary for the rest of the bridge defects within the cell (i.e., BrDC), and

TABLE VI. Simulation results for bridges

Results for BrDs within the cell						
Defects		R_{cr} of WCB	Stressful CBs			
BrD	WCB	at $\frac{C_g}{C_b}$=10	01	10	11	00
BrDC-$R1_t$	00	18.498KΩ	+	+	+	+
BrDC-$R2_t$	00	4.18KΩ	+	+	+	+
BrDC-$R2_c$	−	−	−	−	−	−
BrDC-$R3_t$	00	8.046KΩ	+	+	+	+
BrDC-$R3_c$	−	−	−	−	−	−
BrDC-$R4_t$	−	−	−	−	−	−
BrDC-$R4_c$	00	7.946KΩ	+	+	+	+
BrDC-$R5_t$	−	−	−	−	−	−
BrDC-$R6_t$	−	−	−	−	−	−
BrDC-$R6_c$	−	−	−	−	−	−
Results for BrDs of two cells on the same row(L)						
BrD	WCB	R_{cr} of WCB	11	01	00	10
BrDL-$R1_t$	−	−	−	−	−	−
BrDL-$R1_c$	10	21.212KΩ	+	−	−	+
BrDL-$R2_t$	00	18.198KΩ	−	+	+	−
BrDL-$R2_c$	−	−	−	−	−	−
BrDL-$R3_t$	−	−	−	−	−	−
BrDL-$R3_c$	10	6.621KΩ	+	−	−	+
BrDL-$R3_i$	00	4.478KΩ	+	+	+	+
BrDL-$R3_{ic}$	−	−	−	−	−	−
BrDL-$R4_t$	00	6.286KΩ	−	+	+	−
BrDL-$R4_c$	−	−	−	−	−	−
BrDL-$R4_i$	10	4.440KΩ	+	+	+	+
BrDL-$R4_{ic}$	−	−	−	−	−	−
BrDL-$R5_t$	−	−	−	−	−	−
BrDL-$R5_c$	−	−	−	−	−	−
BrDL-$R6_t$	−	−	−	−	−	−
BrDL-$R6_i$	−	−	−	−	−	−
Results for BrDs of two cells on the same row (R)						
BrD	WCB	R_{cr} of WCB	11	00	10	01
BrDR-$R1_t$	−	−	−	−	−	−
BrDR-$R1_c$	01	21.316KΩ	+	−	−	+
BrDR-$R2_t$	−	−	−	−	−	−
BrDR-$R2_c$	00	18.194KΩ	−	+	+	−
BrDR-$R3_t$	01	4.488KΩ	+	+	+	+
BrDR-$R3_c$	−	−	−	−	−	−
BrDR-$R3_i$	−	−	−	−	−	−
BrDR-$R3_{ic}$	01	6.716KΩ	+	−	−	+
BrDR-$R4_t$	00	4.457KΩ	+	+	+	+
BrDR-$R4_c$	−	−	−	−	−	−
BrDR-$R4_i$	00	6.133KΩ	−	+	−	−
BrDR-$R4_{ic}$	−	−	−	−	−	−
BrDR-$R5_t$	−	−	−	−	−	−
BrDR-$R5_c$	−	−	−	−	−	−
BrDR-$R6_t$	−	−	−	−	−	−
BrDR-$R6_i$	−	−	−	−	−	−

between adjacent cells. The read 0 results and analysis for BrDC-$R1_t$ … BrDC-$R6_t$ with their complement, interchange and comp interchange behaviours are listed in the upper part of Table VI. Likewise, results for BrDL-$R1_t$ … BrDL-$R6_t$, their complement, interchanged and interchanged comp behaviours are listed in the middle part of Table VI, while for BrDR-$R1_t$ … BrDR-$R6_t$, with their complement, interchange and comp interchange behaviours are listed in the lower part of Table VI.

The first column of Table VI lists the BrDs, while the second column lists their corresponding WCBs. The third column gives the values of R_{cr} at $\frac{C_g}{C_b}$=10 for the WCBs. The fourth column lists whether other CBs necessitated a fail (+) or not (−) for each given BrD.

For bridges within the cell, as listed in Table VI, WCB for BrDC-$R1_t$, BrDC-$R2_t$, BrDC-$R3_t$ and BrDC-$R4_c$ is CB00. However, for the rest of the BrDCs, correct logic outputs were recorded and no fails occurred. These results can be explained as follows.

For example, for BrDC-$R2_c$, where the bridge defect lies between the false node (F_m) and the BCm, since the content of Mm1 is 0, irrespective of the content of Ml1 and Mr1, the cell will not be modified to yield an incorrect logic 1. The reason is that during a read 0, BCm remains unchanged whereas only BTm is discharged, Since the position of this bridge is located along this unmodified path, influence on the content of Mm1 is very minimal and does not modify the content of the cell. More so, the impact of VCl, (which develops on BCl) will also not have any modifying effect on Mm1 due to the position of the bridge thus, the read 0 operation succeeds.

BrDLs, BrDL-$R1_c$, BrDL-$R2_t$, BrDL-$R3_c$, BrDL-$R3_i$, BrDL-$R4_t$ and BrDL-$R4_i$ necessitate incorrect logic 1 outputs, whereas the rest of the BrDLs as listed in Table VI all yielded correct logic 0 outputs. However, For BrDL-$R1_c$ and BrDL-$R3_c$ WCB is CB10. The reason is for this behavior is that VTr has no obvious impact on the content of Mm1 due to the location of the bridge, since both cells contain a logic 0, and BCm is not discharged. A logic 0 in Ml1 would as well not be impactful in changing the content of Mm1. However, a logic 1 in Ml1 will cause the content of Mm1 to flip due to the coupling effect of some voltage VCl, which pulls BTm up by some voltage VTm. This therefore explains why CBs 00 and 01 would not necessitate a fail using this bridge. Note that the position of BrDRs are symmetric to those of BrDLs relative to Mm1, thus they have exhibited complementary behaviors as shown by our results.

B. Simulation analysis of open defects

In this section, we present a behavioral summary of the open defects. The simulation results and analysis for OD-$R1_t$ … OD-$R9_t$ (all on the T Node side) are listed in the upper part of Table VII, while those for OD-$R1_c$ … OD-$R9_c$ (all on the F Node side) are listed in the lower part of Table VII. The first column of Table VII lists the ODs, while the second column lists their corresponding worst case CBs. The third column gives the values of R_{cr} at $\frac{C_g}{C_b}$=10 for the worst case CB. The fourth column lists whether other CBs also cause a fail (+) or not (−) for each given OD. Complete analysis has been provided in [19].

As listed in Table VII, for OD-$R4_t$ and OD-$R5_t$ very

TABLE VII. Simulation results for opens

Defects	Worst	R$_\text{cr}$ of CB00	Stressful CBs		
Read 0	CB	at $\frac{C_\text{g}}{C_\text{b}}$=10	01	10	11
OD-R1$_\text{t}$	00	93KΩ	−	−	−
OD-R2$_\text{t}$	00	2.43MΩ	−	+	−
OD-R3$_\text{t}$	00	45KΩ	−	+	−
OD-R4$_\text{t}$	00	2.28KΩ	+	+	+
OD-R5$_\text{t}$	00	1.54KΩ	+	+	+
OD-R6$_\text{t}$	00	38GΩ	+	+	+
OD-R7$_\text{t}$	−	−	−	−	−
OD-R8$_\text{t}$	−	−	−	−	−
OD-R9$_\text{t}$	−	−	−	−	−
Read 1	WCB	R$_\text{cr}$ of WCB	00	01	10
OD-R1$_\text{c}$	11	61KΩ	−	+	+
OD-R2$_\text{c}$	11	2.08MΩ	−	+	+
OD-R3$_\text{c}$	11	29KΩ	−	+	+
OD-R4$_\text{c}$	11	8KΩ	+	+	+
OD-R5$_\text{c}$	11	3.86KΩ	+	+	+
OD-R6$_\text{c}$	11	207GΩ	+	+	+
OD-R7$_\text{c}$	−	−	−	−	−
OD-R8$_\text{c}$	−	−	−	−	−
OD-R9$_\text{c}$	−	−	−	−	−

low R$_\text{cr}$ values were recorded. This underscores the high sensitivity to a resistive open on the pull-down transistor, which is on the current path of a read 0. This is also the case for OD-R4$_\text{c}$ and OD-R5$_\text{c}$ at the F Node side of the cell while performing a read 1 where BCm is discharged. In the presence of OD-R7$_\text{t}$ . . . OD-R9$_\text{t}$ the cell exhibits a defect-free behavior irrespective of the CB used. These three ODs represent broken connections at the source, gate and drain of the pull-up transistor. Since for a read 0, current flows through the NMOS pass transistor on the BT side, through the pull-down NMOS transistor to ground, and this necessary current path does not pass through OD-R7$_\text{t}$ . . . OD-R9$_\text{t}$, the cell exhibits a defect-free behavior such that the sense amplifier gives a correct output for all performed simulations. Here, a delay fault occurs, which takes place a while after the operation is performed. Special tests are used to detect these faults [11]. Likewise, OD-R7$_\text{c}$ . . . OD-R9$_\text{c}$ on the F Node side exhibit a complementary behavior for a read 1 operation.

C. Simulation analysis of short defects

In the same way as the analysis in the previous sections, this section presents the simulation results for short defects. For each evaluated short defect, all scenarios are considered namely, read 0 and read 1 operations performed using all CBs for $\frac{C_\text{g}}{C_\text{b}}$ values. Table VIII gives a summary of the results for read 0 and 1 operations.

TABLE VIII. Simulation results for Shorts

Shorts		R$_\text{cr}$ of WCB	Stressful CBs			
Read 0	WCB	at $\frac{C_\text{g}}{C_\text{b}}$=10	01	10	11	00
SHC-R1	00	5.017KΩ	+	+	+	+
SHC-R1$_\text{c}$	−	−	−	−	−	−
SHC-R2	−	−	−	−	−	−
SHC-R2$_\text{c}$	00	23.183KΩ	+	+	+	+
SHB-R1	00	0.047KΩ	+	+	+	+
SHB-R1$_\text{c}$	−	−	−	−	−	−
SHB-R2	−	−	−	−	−	−
SHB-R2$_\text{c}$	00	7.738KΩ	+	+	+	+
SHW-R1	−	−	−	−	−	−
SHW-R2	−	−	−	−	−	−
Read 1	WCB	R$_\text{cr}$ of WCB	01	10	11	00
SHC-R1	−	−	−	−	−	−
SHC-R1$_\text{c}$	11	0.915KΩ	+	+	+	+
SHC-R2	11	7.272KΩ	+	+	+	+
SHC-R2$_\text{c}$	−	−	−	−	−	−
SHB-R1	−	−	−	−	−	−
SHB-R1$_\text{c}$	11	0.052KΩ	+	+	+	+
SHB-R2	11	6.488KΩ	+	+	+	+
SHB-R2$_\text{c}$	−	−	−	−	−	−
SHW-R1	−	−	−	−	−	−
SHW-R2	11	2.101KΩ	+	+	+	+

The first column of Table VIII lists the shorts, while the second column lists their corresponding WCBs. The third column gives the values of R$_\text{cr}$ at $\frac{C_\text{g}}{C_\text{b}}$=10 for each WCB, while the fourth column lists whether other CBs cause a fail (+) or not (−) for each given short. As shown, CB00 and CB11 are the WCBs for read 0 and read 1 operations. These WCBs represent the worst case coupling backgrounds required for stressing the operations, something that is important to consider while deriving tests that would detect faults in the presence of BL coupling.

VI. Memory testing for BL coupling

In order to ensure the detection of a given type of faulty behavior in the presence of BL coupling, the memory test needs to ensure that the worst case coupling backgrounds are applied. For single-cell static faults, where WCB is CBxx, this means that in case a test is supposed to detect a 1 from a given cell, then both neighboring cells (CBs) should contain a logic 1. Also, to detect a 0 from a given cell, both neighboring cells should contain a logic 0.

However, for two-cell static faults, the worst case coupling backgrounds could be xx, xy or yx. An important condition for detection in this case is that all possible WCBs must be generated for the read operations during testing, in order to ensure the highest fault coverage.

A. Limitations of existing memory tests

Table IX and Table X compare the *fault coverage (FC)* of a number of memory tests for single-cell and two-cell static faults. The tables clearly show how the presence of BL coupling reduces the fault coverage of memory tests that can otherwise detect certain static faults. In Table IX and Table X, the first column lists the tests, while the first row lists the FFMs. Under each FFM, the notation x/y :

a/b is used. x shows how many faults out of the y specified FPs are detected by the listed test in the *absence* of BL coupling, while a shows if all such faults out of b specified FPs are detected in the *presence* of BL coupling. $\mathrm{CF}_{\mathrm{ds}_{\mathrm{wx}}}$ indicates faults caused by non-transition write operation, while $\mathrm{CF}_{\mathrm{ds}_{\mathrm{rx}}}$ indicates faults caused by read. In the last column the fault coverage, FC is listed. Again, the notation x/y is used. Here, x indicates if *all* faults are detected in the presence of BL coupling, while y denotes the total number of FFMs listed.

For single-cell faults, one test that satisfies the BL coupling detection requirement is March SR = $\{\Downarrow(w0); \Uparrow(r0, w1, r1, w0); \Uparrow(r0, r0); \Uparrow(w1); \Downarrow(r1, w0, r0, w1); \Downarrow(r1, r1)\}$ [16]. In this test, each accessed cell retains the same logic value at the beginning and at the end of each march element, thereby generating the background xx. However, this test does not detect all single-cell static faults, nor all two-cell static faults, since variations in the contents of the coupling cells are required to completely test for worst case conditions.

An industrial test that satisfies the condition for BL coupling detection of single-cell faults (with WCBs xx) is Scan = $\{\Updownarrow(w0); \Updownarrow(r0); \Updownarrow(w1); \Updownarrow(r1)\}$ [1]. However, Scan can only detect a limited number of single-cell static faults, and does not detect any two-cell static FFM.

March MSS [17] also effectively detects all single-cell and two-cell static faults. However, in the presence of BL coupling, this optimal memory test fails to detect all such faults. The reason is due to the absence of the necessary WCBs required to detect the faults under the influence of BL coupling. Again, this clearly shows how BL coupling has limited the fault coverage of this otherwise efficient march test.

Another well-known industrial test, which is used for detecting unique faults that are not detected by other tests is the galloping pattern (GALPAT) test [5]. This tests has long been used in industry, but vaguely understood. It effectively detects most (but not all) single and two-cell faults in the presence of BL coupling. The reason why GALPAT can detect certain unique faults in the presence of BL coupling is that it performs tests for each cell, using all possible neighborhood combinations (thereby generating the worst case coupling backgrounds xx, xy and yx). However, GALPAT is expensive in test time and complexity, therefore cheaper and more efficient tests are required.

B. Modifying March MSS

This paper therefore presents a modified version of March MSS [17] (listed as *March m-MSS* in the tables) by implementing a number of different data backgrounds used with the test, such that all single-cell and two-cell static faults, in the absence or presence of BL coupling are detected. This is achieved by using the following data backgrounds in combination with the test:

1) Solid-0 data background (00000000...)
2) Solid-1 data background (11111111...)
3) Double-column stripes data background (00110011...)
4) Double-column stripes data background (11001100...)
5) Shifted double-column stripes data background (01100110...)
6) Shifted double-column stripes data background (10011001...)

$$\begin{array}{lll} \text{March m-MSS} = \{ & \Updownarrow(w0); & \text{ME0} \\ & \Uparrow(r0, r0, w1, w1); & \text{ME1} \\ & \Uparrow(r1, r1, w0, w0); & \text{ME2} \\ & \Downarrow(r0, r0, w1, w1); & \text{ME3} \\ & \Downarrow(r1, r1, w0, w0); & \text{ME4} \\ & \Updownarrow(r0)\} & \text{ME5} \end{array}$$

The modified test detects all single-cell faults in the presence of BL coupling as follows. March element ME0 initializes the memory to 0. ME1 starts by sensitizing and detecting SF_0, RDF_0 and IRF_0, while the second $r0$ sensitizes and detects DRDF_0. ME1 also sensitizes TF_0 during the first $w1$ operation, and then WDF_1 during the second $w1$ operation. These two faults are detected during the first $r1$ of ME2, as well as SF_1, RDF_1 and IRF_1, while the second $r1$ detects DRDF_1 and so on. The complementary counterparts of the faults are sensitized and detected in the same way by ME3, ME4 and ME5. Likewise, March m-MSS detects all two-cell faults. This test is performed using a different data background each time. This ensures that the worst case conditions necessary for detecting faults in the presence of BL coupling are applied. The time complexity of March m-MSS is $108n$, since the test is performed six times with each of the six different data backgrounds.

VII. Conclusion

In this paper, the impact of BL coupling and neighborhood data on faulty behavior in SRAMs have been presented. A theoretical analysis of the impact, its validation through electrical simulations using injected defects in the memory cell array were presented. The results show that the required worst case coupling background in neighborhood cells could be xx, xy and yx, something that is important to take into consideration when generating SRAM tests. The paper demonstrated that due to these worst case conditions for detecting BL coupling, several memory tests are limited in detecting all static faults in the presence of BL coupling and varied neighborhood data.

TABLE IX. Comparison of tests fault coverage for single-cell FFMs

Tests	$\mathbf{SF_0}$	**TF**	**WDF**	**RDF**	**DRDF**	**IRF**	FC
GalPat	2/2 : 2/2	2/2 : 2/2	0/2 : 0/2	2/2 : 2/2	0/2 : 0/2	2/2 : 2/2	0/6
MATS+	2/2 : 0/2	1/2 : 0/2	0/2 : 0/2	2/2 : 0/2	0/2 : 0/2	2/2 : 0/2	0/6
March SR	2/2 : 0/2	2/2 : 0/2	0/2 : 0/2	2/2 : 0/2	2/2 : 0/2	2/2 : 0/2	0/6
March C-	2/2 : 0/2	2/2 : 0/2	0/2 : 0/2	2/2 : 0/2	0/2 : 0/2	2/2 : 0/2	0/6
March B	2/2 : 0/2	2/2 : 0/2	0/2 : 0/2	2/2 : 0/2	0/2 : 0/2	2/2 : 0/2	0/6
PMOVI	2/2 : 0/2	2/2 : 0/2	0/2 : 0/2	2/2 : 0/2	2/2 : 0/2	2/2 : 0/2	0/6
March MSS	2/2 : 0/2	2/2 : 0/2	2/2 : 0/2	2/2 : 0/2	2/2 : 0/2	2/2 : 0/2	0/6
March m-MSS	2/2 : 2/2	2/2 : 2/2	2/2 : 2/2	2/2 : 2/2	2/2 : 2/2	2/2 : 2/2	6/6

TABLE X. Comparison of tests fault coverage for two-cell FFMs

Tests	$\mathbf{CF_{st}}$	$\mathbf{CF_{ds_{rx}}}$	$\mathbf{CF_{ds_{wx}}}$	$\mathbf{CF_{id}}$	$\mathbf{CF_{wd}}$	$\mathbf{CF_{rd}}$	$\mathbf{CF_{drd}}$	$\mathbf{CF_{ir}}$	$\mathbf{CF_{tr}}$	FC
GalPat	8/8 : 8/8	8/8 : 8/8	8/8 : 8/8	8/8 : 8/8	0/8 : 0/8	8/8 : 8/8	0/8 : 0/8	8/8 : 8/8	8/8 : 8/8	0/9
MATS+	4/8 : 0/8	3/8 : 0/8	0/8 : 0/8	3/8 : 0/8	0/8 : 0/8	4/8 : 0/8	0/8 : 0/8	4/8 : 0/8	2/8 : 0/8	0/9
March SR	8/8 : 0/8	8/8 : 0/8	0/8 : 0/8	8/8 : 0/8	0/8 : 0/8	8/8 : 0/8	8/8 : 0/8	6/8 : 0/8	8/8 : 0/8	0/9
March C-	8/8 : 0/8	8/8 : 0/8	0/8 : 0/8	8/8 : 0/8	0/8 : 0/8	8/8 : 0/8	0/8 : 0/8	8/8 : 0/8	8/8 : 0/8	0/9
March B	6/8 : 0/8	7/8 : 0/8	0/8 : 0/8	8/8 : 0/8	0/8 : 0/8	4/8 : 0/8	0/8 : 0/8	4/8 : 0/8	4/8 : 0/8	0/9
PMOVI	8/8 : 0/8	8/8 : 0/8	0/8 : 0/8	7/8 : 0/8	0/8 : 0/8	8/8 : 0/8	0/8 : 0/8	8/8 : 0/8	8/8 : 0/8	0/9
March MSS	8/8 : 0/8	8/8 : 0/8	8/8 : 0/8	8/8 : 0/8	8/8 : 0/8	8/8 : 0/8	8/8 : 0/8	8/8 : 0/8	8/8 : 0/8	0/9
March m-MSS	8/8 : 8/8	8/8 : 8/8	8/8 : 8/8	8/8 : 8/8	8/8 : 8/8	8/8 : 8/8	8/8 : 8/8	8/8 : 8/8	8/8 : 8/8	9/9

The paper therefore presented a modified version of March MSS, (March m-MSS), which detects all single-cell and two-cell faults in the absence and presence of BL coupling.

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