Dynamic Profiling Framework in the Delft Workbench

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Abstract

Heterogeneous reconfigurable systems provide an efficient platform via an integrated utilization of different processing elements, allowing each processor to perform the task(s) for which it is the most appropriate. These systems offer incomparable potentials as they combine both the flexibility of a software-based design with the productivity of a hardware-based execution. However, the widespread utilization of heterogeneous reconfigurable systems is currently difficult due to the shortage of sophisticated tools to help developers fully unleash the performance gain of these systems. The required tools not only need to facilitate the development of new applications on heterogeneous platforms, but also need to help developers gain a comprehensive overview of the runtime behavior of existing applications. Addressing the well-known processor/memory bottleneck, which turns out to be the primary performance obstacle of these hybrid systems, requires a thorough inspection of the memory access patterns of applications for optimal performance gain.

The Delft Workbench is a semi-automatic tool platform for integrated hardware/software co-design, targeting heterogeneous computing systems containing reconfigurable components. It addresses the entire design cycle from application profiling to the code generation for a target architecture. We present the current status of the dynamic profiling framework within the Delft Workbench. The main focus is on the introduction of the sophisticated memory access profiling toolset that provides a detailed overview of the runtime behavior of an application for code optimizations. The extracted information is vital for porting an application to a heterogeneous reconfigurable platform. We also investigate the possible utilization of this information in subsequent stages of application development process.

Keywords: Heterogeneous Reconfigurable Computing, Hardware/Software Co-design, Dynamic Profiling, Performance Evaluation.

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