Test Cost Analysis for 3D Die-to-Wafer Stacking

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Abstract

The industry is preparing itself for three-dimensional stacked ICs (3D-SICs); a technology that promises heterogeneous integration with higher performance and lower power dissipation at a smaller footprint. Several 3D stacking approaches are under development. From a yield point of view, Die-to-Wafer (D2W) stacking seems the most favorable approach, due to the ability of Known Good Die stacking. Minimizing the test cost for such a stacking approach is a challenging task. Every manufactured chip has to be tested, and any tiny test saving per 3D-SIC impacts the overall cost, especially in high-volume production. This paper establishes a cost model for D2W SICs and investigates the impact of the test cost for different test flows. It first introduces a framework covering different test flows for 3D D2W ICs. Subsequently, it proposes a test cost model to estimate the impact of the test flow on the overall 3D-SIC cost. Our simulation results show that (a) test flows with pre-bond testing significantly reduce the overall cost, (b) a cheaper test flow does not necessary result in lower overall cost, (c) test flows with intermediate tests (performed during the stacking process) pay off, (d) the most cost-effective test flow consists of pre-bond tests and strongly depends on the stack yield; hence, adapting the test according the stack yield is the best approach to use.

Keywords: *3D test flow, 3D test cost, Die-to-Wafer stacking, 3D manufacturing cost, Through-Silicon-Via.*

I. Introduction

The popularity of 3D Stacked ICs (3D-SICs) is rising among industry and research institutes [1–8]. 3D-SICs are emerging as one of the main contesters to continue the trend of Moore's Law. Currently, a number of methods have been proposed to implement the interconnection of stacked dies [1]. One of the most promising and perhaps the most reliable way to achieve this is with *Through-Silicon Vias (TSVs)*. TSVs are holes going through the chip silicon substrate filled with a conducting material. They enable short interconnections in 3D-SICs.

The prospects of the research [1–8] show many 3D-SICs benefits compared to planar dies [2], and include (a) improved performance due to short TSVs that connect IPs on different layers, (b) heterogeneous integration (for example, DRAM memory can be manufactured in separate layers), and (c) a better form factor and package volume density due to vertical stacking.

3D-SICs with TSVs can be manufactured using three different stacking approaches: Wafer-to-Wafer (W2W), Die-to-Wafer (D2W) or Die-to-Die (D2D) stacking [2]. In W2W, complete wafers are stacked and bonded together. The major benefit of W2W is the high manufacturing throughput and the ability to handle small dies. In D2D, a high yield can be obtained due to Known Good Die (KGD) stacking [2], but the throughput is expected to be less. The manufacturing throughput in D2W settles between D2D and W2W, and results in similar yields as in D2D due to the same ability of KGD stacking. This paper focuses on D2W stacking as it is the most relevant stacking approach in industry.

To guarantee high 3D-SIC product quality at lower cost, appropriate test flows need to be developed. For example, in D2W stacking dies may not only require testing before they are stacked (i.e., pre-bond testing), but also during and after stacking (post-bond test). The question arises, whether it is justifiable to perform a pre-bond test as well as a post-bond test after each created temporary stack; i.e. are the dies still functionally operating and are the TSVs created properly. Sources of die failures during stacking could be introduced by thinning, bonding and TSV failures including misalignment and opens [9]. If it is known beforehand that a particular stack is corrupted, silicon, TSV and stacking costs can be prevented for the successive die that has to be stacked in D2W stacking. This paper investigates the impact of different test flows on the overall

3D cost in D2W stacking. The emphasis is on the impact of the different test flows, rather than on the analysis of the impact of different manufacturing processes. The contributions of this paper are the following.

- A new framework that covers different test flows.
- A cost model for 3D D2W-stacked 3D-SICs.
- An investigation of the impact of different 3D D2W test flows on the overall 3D cost.

The remainder of the paper is organized as follows. Section II presents the test flow framework. Section III introduces the cost model used for the evaluation of the various test flows. Section IV discusses our simulation results; it first describes the parameters of the experiments, and thereafter presents the experimental results. Section V concludes the paper.

II. Test Flow Framework

This section first defines a test flow for 3D-SICs by extending the 2D test flow. Thereafter, it provides a framework for 3D test flows.

A. 2D versus 3D Test Flow

A conventional 2D test flow for planar wafers is depicted in Figure 1(a) [10]. Here, usually two *test moments* are applicable; i.e., a wafer test prior to packaging and the final test after packaging. The wafer test can be cost-effective when the yield is low, since it prevents unnecessary assembly and packaging costs. The goal of the final test is to guarantee the required quality of the final packaged chip. For 3D-SICs, four test moments can be distinguished in time as depicted in Figure 1(b). We categorize all different test moments in these four test phases, as given next:

1) T_{pb}: n *pre-bond* wafer tests for each individual die on the wafer (n is the number of stacked layers). T_{pb} tests prevent faulty dies from being stacked. Besides testing for dies, TSVs (in case of via-first [2]) can be tested for as well. Although the bonding is not performed yet, capacitance tests can detect some faulty TSVs [11].

2) T_{in}: n-2 *intermediate* tests applicable during the intermediate stacking and bonding. In this case, either the dies, the interconnects, their combination or none of them can be tested for. Good tested dies in the pre-bond test phase could get corrupted during the stacking process as a consequence of e.g, die thinning, or bonding [9]. In the simulation model of our test flows, first the interconnects are tested and thereafter the dies in bottom up order (in case both are tested for); if a fault is detected in the interconnects, then there is no need to test the dies as the SIC will be faulty anyway. The
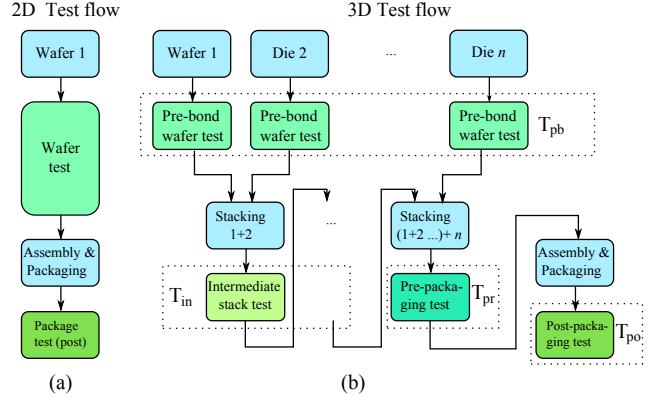

Fig. 1. 2D versus 3D D2W test flows.

reason for this particular order is that the test cost for interconnects is considered cheaper, as will be explained in Section III.

3) T_{pr}: one *pre-packaging* test. This test can be applied after the complete stack is formed. Analogous to wafer testing in the 2D test flow, T_{pr} can be seen as a way to prevent unnecessary assembly and packaging cost.

4) T_{po}: one final *post-packaging* test can be applied after assembly and packaging to ensure the required quality of the complete 3D-SIC. Other specific packaging related tests could be applied here as well.

Note that in total there are $2 \cdot n$ different test moments.

Depending on either one or more companies are involved in the manufacturing of 3D-SICS, different requirements can be set for the pre-bond wafer test quality [12]. If the wafers are produced by one or more companies and the final 3D-SIC product is processed and manufactured by another company, a high pre-bond wafer test quality (e.g. a KGD) often is agreed upon. If a KGD contract is in place, high-quality pre-bond testing is required. If such a contract is not in place, the pre-bond test quality is subject to optimization. This mean, there is not only the option to perform pre-bond testing or not, but also to perform pre-bond testing at a higher or lower test quality. Faulty undetected dies can be detected in a later stadium, e.g., in higher quality post-packaging tests. Similarly, a high quality pre-packaging test (Known Good Stacks test) can be applied.

B. 3D Test Flow Framework

The test flow framework for 3D D2W stacking can be extracted from the test flow moments depicted in Figure 1(b). Depending on whether no or at least one test is performed at each possible test moment, we can distinguish 2^{2n} possible test flows out of $2n$ test moments. This number will further increase if we consider that tests

TABLE I. Test flow framework

T_{pb}	T_{in}	T_{pr}			
		$d_t i_t$	$d_t i_a$	$d_a i_t$	$d_a i_a$
n	n	–	–	–	TF1
n	i_t	–	–	TF2	–
n	d_t	–	TF3	–	–
n	$d_t i_t$	TF4	–	–	–
y	n	–	–	–	TF5
y	i_t	–	–	TF6	–
y	d_t	–	TF7	–	–
y	$d_t i_t$	TF8	–	–	–

"–" denotes non-applicable

of each phase may target different faults; e.g., if we assume that T_{in} may test (1) one or more dies, (2) one or more interconnects, (3) a combination of (1) and (2), or (4) none, then the number of possibilities for T_{in} will be 4^{n-2}. This increases the number of test flows from 2^{2n} to 2^n (T_{pb}) $\times 4^{n-2}$ (T_{in}) $\times 2$ (T_{pr}) $\times 2$ (T_{po}) $= 2^{3n-2}$. It is clear that considering all 'theoretical' possible test flows will result in an unmanageable space. Therefore realistic assumptions have to be made in order to create a clear overview (without loss of generality) for the work presented in this paper. Our assumptions consist of the following.

1) During stacking, it is assumed that only the *top* two dies could get corrupted since these dies are most susceptible to the stacking/bonding steps like heating, thinning, pressure, and TSV-related defects.
2) Each test flow has to guarantee that a 3D-SIC is fault free before it is packaged to prevent unnecessary costs. The test phases 'T_{pb}+T_{in}+T_{pr}' test each die and each interconnect of the SIC at least once.
3) For the T_{in} test phase, the *same* test content is assumed to be applied among all $n-2$ test moments.
4) The tests performed during T_{po} are assumed to be the same for all test flows.

Because of Assumption 1, T_{in} will test only for one of the following:

- Only for the *top dies* (d_t= dies top)
- Only for the *interconnect* between the top dies (i_t= interconnect top).
- For both the *top dies* and *top interconnects* ($d_t i_t$).
- none (n)

This results into $T_{in} \in \{d_t, i_t, d_t i_t, n\}$.

Table I contains the test flow framework of all possible test flows based on the above assumptions. The first column denotes the two possibilities for T_{pr} (pre-bond test), either it is performed ('y') or not ('n'). The second column gives the four possible values of $T_{in} \in \{d_t, i_t, d_t i_t, n\}$. The second row of the rest of the columns list the different possible values of T_{pr} required in combination with T_{pb} and T_{in} to satisfy Assumption 2; these are:
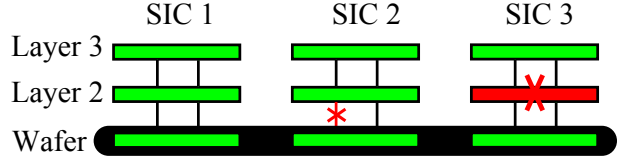
Fig. 2. Faults during stacking

- $d_t i_t$: test for both top dies and top interconnects.
- $d_t i_a$: test for top dies and *all* interconnects.
- $d_a i_t$: test for *all* dies and top interconnects.
- $d_a i_a$: test for *all* dies and *all* interconnects.

Each possible test flow is given a name in the table; e.g., TF1 denotes a test flow based on no T_{bp}, no T_{in} and $T_{pr} = d_a i_a$. There are in total eight test flows, i.e., TF1 to TF8. The entries with '–' denote non-applicable combinations, as they do not satisfy Assumption 2 or more tests are applied than required by Assumption 1.

The framework of test flows clearly indicates that an appropriate 3D DfT test architecture has to support independent testing of dies and interconnects, both for intermediate and final stacks. In [13], an architecture providing these functionalities is proposed.

In order to provide more insight into the different test flows and their impact on the total cost of 3D-SICs, we consider the example shown in Figure 2. It consists of three SICs with n=3 layers each. For simplicity, it is assumed that all dies in the pre-bond phase were manufactured with 100% yield and that two faults occurred during stacking of Layer 2 on the bottom layer, one in SIC2 and the other one in SIC3. In SIC2, a fault occurred in the interconnects between the bottom die (i.e, Layer 1) and the die at Layer 2 (e.g., due to TSV failures), while in SIC3 a fault occurred in Layer 2 (e.g., because of thinning). It is assumed that during the intermediate and pre-packaging tests, first interconnects are tested, followed by the dies in bottom up order.

Table II shows the impact of four test flows TF1, TF2, TF3 and TF4 on three different cost factors: manufacturing, test, and packaging. Each entry in the table is composed out of three numbers, associated with SIC1, SIC2 and SIC3 respectively, followed by their sum. The costs are explained next.

The manufacturing cost is considered to include the number of used dies (the second column of the table) and the number of stacking operations performed (the third column of the table). For example, in TF1 only $T_{pr}=d_a i_t$ is performed (see Table I); therefore this will result in: (a) stacking of three dies per 3D-SIC, hence 3+3+3=9 dies, and (b) two stacking operations per SIC, thus a total of 2+2+2=6.

TABLE II. Impact of Test Flows

TF	Manufacturing cost		Test cost					Packaging cost
	#dies	#stacking operations	T_{pb} #dies	T_{in} #inter	T_{in} #dies	T_{pr} #inter	T_{pr} #dies	#packaged SICs
TF1	3+3+3=9	2+2+2=6	0+0+0=0	0+0+0=0	0+0+0=0	2+1+2=5	3+0+2=5	1+0+0=1
TF2	3+2+3=8	2+1+2=5	0+0+0=0	1+1+1=3	0+0+0=0	1+0+1=2	3+0+2=5	1+0+0=1
TF3	3+3+2=8	2+2+1=5	0+0+0=0	0+0+0=0	2+2+2=6	2+1+0=3	2+2+0=3	1+0+0=1
TF4	3+2+2=7	2+1+1=4	0+0+0=0	1+1+1=3	2+0+2=4	1+0+0=1	2+0+0=2	1+0+0=1

The test cost is categorized according to the test phases defined in Section II-A; i.e., pre-bond wafer tests T_{pb}, intermediate tests T_{in}, pre-packaging tests T_{pr} and post-packaging tests T_{po}. Note that T_{po} is not included in the table as we assumed that post-packaging tests are the same for all test flows (Assumption 4). Except for the T_{pb} phase, each test phase distinguishes between tests for interconnects and tests for dies. Consider test flow TF4, which performs the following tests (see also Table I):

- No pre-bond test (i.e., $T_{pb}=n$): no tests are executed and therefore no pre-bond tests for the three SICs are performed.
- Intermediate tests consisting of (a) tests for top dies and (b) tests for top interconnects (i.e., $T_{in}=d_t i_t$). Note that there is $n-2=1$ test moment. Hence, in this phase TF4 tests for the interconnects between the bottom layer and Layer 2 of each SIC, resulting in $1+1+1=3$ tests. In addition, TF4 tests for two bottom dies of SIC1 (i.e., the first two layers), no die from SIC2 (since the interconnect found to be faulty during i_t tests) and two bottom dies of SIC3 resulting into $2+0+2=4$ tests.
- Pre-package tests consisting of testing top dies and top interconnects of the SIC ($T_{pr}=d_t i_t$). In this phase, TF4 tests only for the top interconnects and the two top dies of SIC1, not those of SIC2 and SIC3 as they are already considered faulty after the intermediate tests were applied. This results into a total test of one interconnect and two dies during this phase.

The packaging cost is given in the last column of Table II. Because of Assumption 2, the packaging cost are the same for all the four test flows. Only SIC1 will be packaged, while the other two SICs will be discarded.

III. 3D Cost Model

To evaluate the impact of the different test flows on the overall 3D-SIC cost, an appropriate cost model is built. Figure 3 shows the block diagram of the cost model; it considers three major inputs:

- Manufacturing cost: It includes wafer cost, costs required for wafer processing, TSVs and 3D stacking.
- Test cost: The cost related to testing of dies and interconnects. Test flows have a large impact on this cost since they determine when and what to test for.
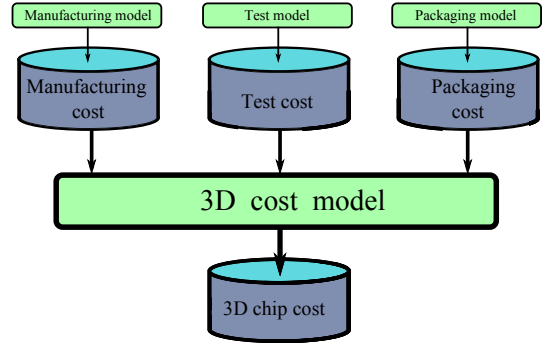

Fig. 3. Test cost model 3D D2W Stacking.

- Packaging cost: The cost to package stacked 3D-SICs.

The cost model calculates the overall 3D cost per test flow. In addition, it also determines the share of the test cost as compared to the overall cost. In fact, the model performs more elaborated and comprehensive calculations of those explained in the example of Section II-B (shown in Figure 2 and Table II). The model collects statistical data (in our case based on 1000 wafers) while considering the different costs. The monitored data includes e.g., the number of used dies, the number of stacking/bonding operations, the number of packaged SICs, the number of tests performed (for dies and interconnect), etc.

Since the purpose of this work is to investigate the impact of different test flows rather than to observe the impact of different manufacturing processes (e.g., transistor feature size, TSV via-first or via-last, Face-to-Face or Back-to-Face bonding orientation, the number of TSVs etc.), the manufacturing costs are assumed to be constant, as discussed in Section IV. However, the test cost strongly depends on other parameters like die yield, interconnect yield, stacking yield, number of stacked layers, etc. Section IV provides more details about our experiment.

In the rest of this section, more details about the three major inputs of the cost model are given.

a) Manufacturing Cost: It includes wafer cost, costs required for wafer processing, TSV fabrication and 3D stacking/bonding. For wafers and their processing, we used the cost models of [14] and [15]; the total price of a 300 mm wafer is estimated at approximately $2779.

The model in [14] considers a variety of costs, including installation, maintenance, lithography and material. For TSV fabrication, the work of EMC-3D consortium [16] is used; the cost to fabricate 5 μm TSVs in a single wafer is assumed to be \$190 and these cost are additive to the wafer cost. To estimate the cost of the 3D stacking/bonding process, the 3D cost model in [17,18] is used.

b) Test Cost: This cost is related to testing of dies and interconnects. To estimate the test cost per die, the model in [19] is used; it includes depreciation, maintenance and operating cost and assumes five ATE machines operating simultaneously. The derived test cost equals 3.82 \$cent/second per die. Assuming a test time of 6 seconds per die, the test cost will be \$0.23 per die. To estimate the interconnect test cost, a ratio of 1:100 between the test time of dies and interconnects is assumed (as in [20]).

c) Packaging Cost: The packaging cost for 3D SICs used in our model is based on oral conversations with Boschman BV [21] and DIMES [22]. The costs are comprehensive and include machine, maintenance, labor and material cost.

IV. Case Study

In this section, the test flows of Table I are analyzed and evaluated based on the cost model of Figure 3. Section IV-A defines the parameters considered in our experiments, while Section IV-B presents the results.

A. Model Parameters

The impact of the test cost on the overall 3D cost depends on several parameters, e.g., stack size, die yield, number of dies per wafer, stacking yield, interconnect yield, packaging yield, fault coverage, etc. Due to space limitations, in this paper we restrict ourselves to the impact of three main parameters (i.e., stack size n, die yield Y_D and stack yield Y_S) on the test and overall cost. Note that for each experiment, only one parameter is considered to be variable, while the others are set to fixed values. These fixed values are derived from our reference process, which is described next.

In our reference process, the die yield is based on the stacking process in [20], where a standard $300\ mm$ diameter wafer is used with an edge clearance of 3 mm. The work assumes a defect density of $d_0 = 0.5$ defects/cm^2 and a defect clustering parameter $\alpha = 0.5$. With a die area $A = 50\ mm^2$ and a 300 mm wafer, the number of Gross Dies per Wafer (GDW) can be estimated to 1278 [23]. With the negative binomial formula for yield, a die yield of $Y_D = (1 + \frac{A \cdot d_0}{\alpha})^{-\alpha} = 81.65\%$ is expected [19]. For the stack size we assume a default stack size $n=5$.
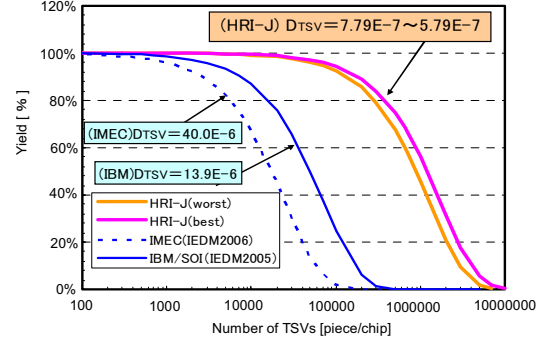

Fig. 4. TSV yield based on a Poisson Distribution [24].

The stacking yield is considered to be composed out of two parameters: the TSV interconnect yield Y_{TSV} and the stacked-die yield Y_{SD}. Figure 4 is used to estimate Y_{TSV} [24]. It shows the TSV yield decrease as a function of the number of TSVs per chip for three manufacturers. In our simulations, the TSV yield Y_{TSV} is assumed to be 95%. Dies that enter the stack could get corrupted during stacking. This is modeled by the stacked-die yield Y_{SD} and is assumed to be 95% as well. Several research works assume a complete stack yield of approximately 95% [20,25].

As already mentioned, three main parameters are considered to be variable in our experiment; these are:

1) **Stack size.** The stack size is considered to vary between $2 \leq n \leq 6$.
2) **Die yield.** The die yield assumes to take values between $60\% \leq Y_D \leq 90\%$.
3) **Stacking yield.** Here, we assume both the Y_{TSV} and Y_{SD} to take values of 93% and 99%.

B. Results

In this section, the simulation results are presented. First, the impact of the test flows on the overall 3D D2W cost is covered, followed by the impact of the test flows on the share of test cost.

1) Impact of Test Flows on Overall Cost: To evaluate the impact on the overall cost, the simulation is performed three times: (1) by varying the stack size while keeping the wafer and stack yield constant, (2) by varying the die yield while keeping the stack size and stack yield constant, and (3) by varying the stack yield while keeping the stack size and die yield constant.

a) Varying the stack size: Figure 5 depicts the relative 3D cost of the test flows for $2 \leq n \leq 6$. Here, the 3D cost for each test flow is normalized to the 3D cost of TF1 for each stack size. For $n=2$, test flows TF1, TF2, TF3 and TF4 result in equal cost; the same thing applies to test flows TF5, TF6, TF7 and TF8. The reason is that
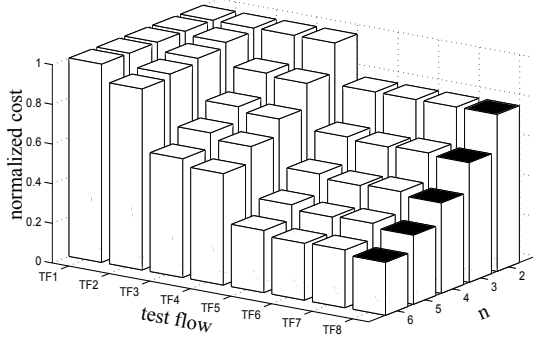
Fig. 5. Normalized test cost for the test flows by considering different stack sizes.

Fig. 6. Normalized test cost for the test flows by considering variable die yield.

in this case, the test flows are the same. The following conclusions can be drawn from the figure:

- Test flows with pre-bond tests significantly reduce the overall cost. The larger n, the larger the reduction.
- TF8 is the most cost-effective test flow irrespective of n. The bars with black tops represent the test flows with the lowest costs per layer.
- TF2 has a marginal impact on the cost reduction irrespective of n. This is because TF2 neither performs pre-bond tests nor die tests during the intermediate phase. This is not the case for TF3 and TF4, as they both test for dies in the intermediate phase.
- While test flow TF2 results in higher cost than test flow TF3, the reverse occurs for the test flows TF6 and TF7. Note that TF1 and TF3 are similar to TF6 and TF7, respectively, except that the TF6 and TF7 also include pre-bond testing. In case of TF6 and TF7 only good dies will be stacked. Hence, it is cost-wise cheaper to test the interconnects (TF6) than to re-test the dies (TF7) during the intermediate phase. Nevertheless, testing both interconnects and dies during the intermediate phase is the most cost-effective test flow (i.e., TF8).

b) Varying the die yield: Figure 6 depicts the relative 3D cost of the test flows with a die yield varying between $60\% \leq Y_D \leq 90\%$. Here, the 3D cost for each test flow is normalized to the 3D cost of TF1. The stack size is fixed to $n=5$ and the interconnect and stacked-die yield are set both to 95%. From the figure we conclude the following.

- Test flows with pre-bond tests significantly reduce the overall cost. The lower the die yield the larger the reduction (except for TF2 since this test flow does not test for dies during the pre-bond and intermediate phases).
- TF2 has a marginal impact on the cost, irrespective of the die yield. This is not the case for TF3 and TF4, as they both test for dies in the intermediate phase.
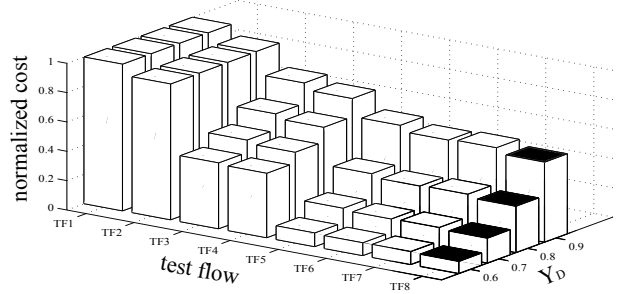- Similar conclusions can be drawn as those from

Figure 5 for the test flows enabled with pre-bond testing. It is cheaper to test for interconnects only (TF6) than to test for dies only (TF7) during the intermediate test phase. Nevertheless, testing both for interconnects and dies during the intermediate phase is the most cost-effective test flow (i.e., TF8).

c) Varying the stack yield: Figure 7 depicts the overall 3D cost versus stacked yield (i.e., interconnect Y_{TSV} and stacked-die Y_{SD}) for the test flows. In the figure, Y_{TSV} and Y_{SD} are set both to 93% and 99%. The 3D cost of the flows are normalized to the cost of TF1 where $Y_{TSV}=Y_{SD}=93\%$. The bars with black tops presents test flows with the least impact on the overall cost per stacking yield. For example, for a stack yield of $[Y_{TSV}, Y_{SD}] = [0.99, 0.99]$, TF6 is the most cost-effective test flow.

From the figure we conclude that TF6 and TF8 are the most cost-effective test flows. If Y_{SD} is very high (i.e., 99%), then TF6 is the best as it tests only for interconnect. However, in case $Y_{SD}=93\%$, TF8 performs better, since it tests for dies during the intermediate phase. Therefore, it is able to prevent unnecessary stacking of dies in faulty partial stacks.

2) Impact of Test Flows on Test Cost: The relative impact of the test cost on the overall cost is depicted in Figure 8 for the reference process. There are two bars per test flow. The first bar presents the overall cost normalized to TF1, while the second bar presents the ratio of test cost with respect to the overall cost. The figure clearly shows that a cheap test flow does not necessary result in lower overall cost. For example, while TF8 reduces the overall cost with 11% as compared to TF5, the share of test cost of TF8 is 35% higher than that of TF5.

V. Conclusion

This paper investigates the impact of several 3D test flows on the total 3D cost in D2W stacking. It introduces a framework of test flows for 3D testing; each flow is based on a combination of tests applied at four test moments, i.e., the pre-bond wafer test, the intermediate stack test, the
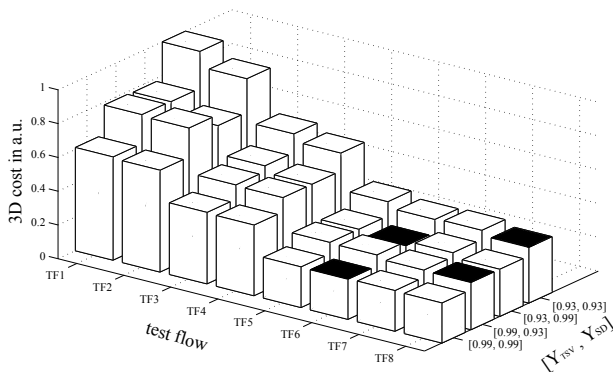
Fig. 7. Normalized test cost for the test flows by considering variable stack yield.
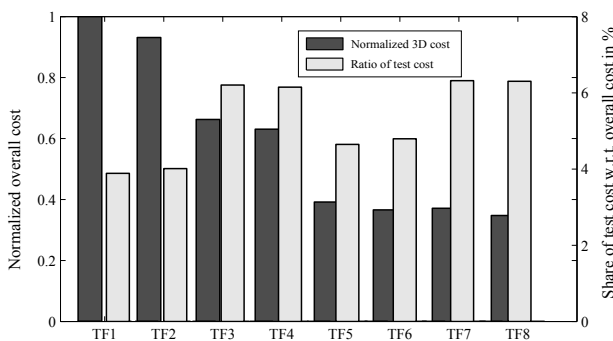

Fig. 8. Test cost versus overall cost.

pre-package test and the post-package test. An appropriate cost model (considering manufacturing, test and packaging cost) is introduced in order to evaluate the impact of different test flows on the overall cost. Different stack sizes, die yield, and stack yield are considered for the evaluation.

The simulation results show that test flows with pre-bond testing significantly reduces the overall cost. Test flows with the intermediate tests enabled with interconnect tests outperform the rest. Moreover, a cheaper test flow does not necessary results in lower overall 3D-SIC cost. The best cost-effective test flow consists of the pre-bond and strongly depends on the stack yield. This requires the adaptation of the test flow during the yield learning of the 3D-SIC process manufacturing. Moreover, test architectures should provide access to all dies as well as all interconnects of the SIC in order to be able to perform intermediate tests.

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