Temperature Impact on NBTI Modeling in the Framework of Technology Scaling

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Abstract. Negative Bias Temperature Instability (NBTI) has become an important reliability concern for nano-scaled Complementary Metal Oxide Semiconductor (CMOS) devices. This paper presents an analysis of the temperature impacts on various sub-processes that contribute to NBTI degradation, for different nano-scaled technologies. We analyze 90nm, 65nm, and 45nm P-type Metal Oxide Semiconductor (PMOS) transistor operating in the temperature range 25-125°C. Experimental results show that the temperature increment substantially rises the PMOS transistor Threshold voltage (Vth) shift due to NBTI and that this shift becomes worst as the technology shrinks. E.g., the Vth shift for 90nm is 34% while this rises with about 4% for each new technology generation (i.e., 38% for 65nm and 42% for 45nm). In addition, the results show that the temperature increment moderately reduces the drain current, and this reduction becomes more severe with technology scaling. E.g., the current reduction is about 5% for 90nm while this is 8% for 45nm.

1 Introduction

The sustained growth in Integrated Circuits (IC) density and speed has been accomplished by CMOS scaling [1]. The scaling reduces gate oxide thickness by 30% in each successive technology generation [2]. Industrial data reveal that as oxide thickness reaches 4nm, reliability concerns (especially NBTI) becomes a major challenge [3, 4]. NBTI degrades the performance of a PMOS transistor under a negative gate stress. The aftereffects of NBTI include: (a) threshold voltage increase of PMOS transistor, (b) drain current degradation, and (c) speed degradation [5, 6]. Experimental analysis shows that these aftereffects increase exponentially with rise in temperature [4].

CMOS scaling meets the demands of integrating more functions on a single chip and speeding up by operations at higher current density and higher gate

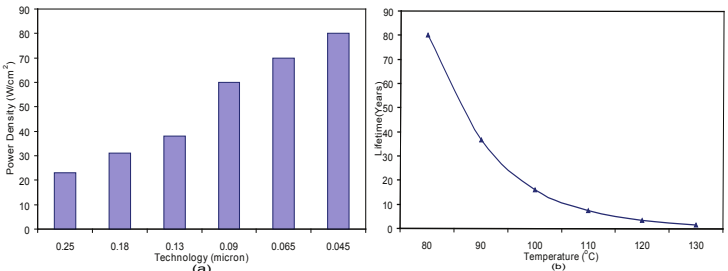


Fig. 1. (a)Microprocessor power density increment with technology scaling (b) NBTI defined lifetime degradation of an inverter under temperature variation

oxide electric field [1]. This leads to continuing increase of the power density of chips in successive technology generations [2],[7]. For example, Fig. 1(a) shows how the power density of microprocessor chips increases with technology scaling [2]. The power density increase and consequent temperature rise accelerate transistor degradations. Experimental results show that NBTI degradation increases exponentially with the temperature increase [8, 13]. For example, Fig. 1(b) illustrates how the NBTI defined lifetime of an inverter reduces by 2.2× for every 10°C increase in temperature [8]. Therefore it is expected that the impact of NBTI will be worse as technology scales down than previously presumed [5]. Hence an accurate analysis of temperature impact on NBTI in various technologies is needed.

Modeling NBTI and analyzing the temperature impact on the transistor degradation have been subject of research for many scientists. In [5, 9–12] NBTI is modeled in terms of different sub-processes contributing to transistor degradation. However, these models do not explicitly consider the temperature impact on NBTI sub-processes. In [13, 14] the temperature impact on NBTI has been studied but the analysis is limited to few sub-processes e.g diffusion. However, other NBTI temperature dependent sub-processes (e.g. atomic and molecular Hydrogen interconversion, bond breaking) were not researched. Additionally, the temperature increment in scaling technologies and its impact on NBTI degradations is not investigated. Overall, the physical basis of the temperature impact on NBTI sub-processes and the impact of increasing temperature in scaling technologies has so for not been fully explored.

In this paper, we analyze temperature impact on NBTI sub-processes and investigate the effect of temperature increment on NBTI degradation for different technologies. The main contributions of this paper are:

- A calibrated analytical investigation of temperature dependencies of all known sub-processes that contribute to NBTI degradation. Our analysis uses NBTI generalized RD model [9], however, it is applicable to any NBTI model.
- An experimental analysis of the temperature impact on the NBTI while considering temperature dependencies of all the sub-processes.
- An experimental analysis of temperature increment impact on NBTI for different technology nodes. The technology nodes used are 90nm, 65nm, and 45nm. The temperature ranges from 25°C to 125°C.

Our analysis shows that the rise in temperature exacerbate threshold voltage increment and drain current degradation. These effects becomes more significant as technology scales down.

The rest of the paper is organized as follows. Section 2 describes RD model and its behavior as technology scales down. Section 3 presents an analytical study of the temperature impact on different NBTI sub-processes including bond breaking and recovery rates, atomic to molecular Hydrogen conversion rate, and Hydrogen species diffusion in oxide layer. Section 4 shows the simulation results and discuss them. Finally Section 5 concludes the paper.

2 NBTI Model Under Technology Scaling

NBTI was recognized as a reliability concern since 1970s, and the well established Reaction Diffusion (RD) model was presented at that time [10]. The model interprets power law time dependence (t^n) of PMOS degradation due to NBTI, e.g. for threshold voltage increase, $\Delta V_{th} \sim t^n$ [4, 5]. The original RD model assumes

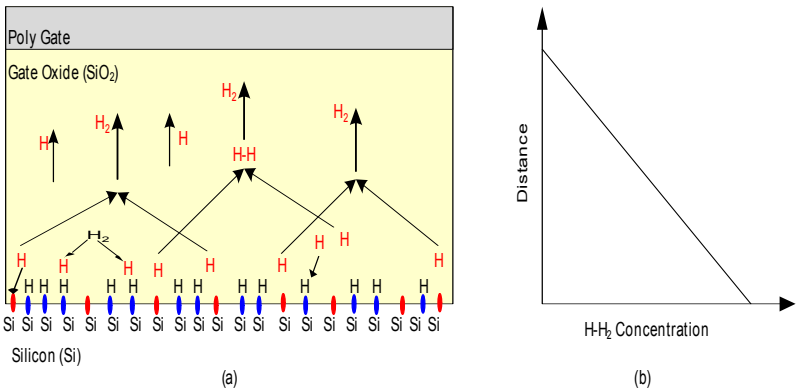


Fig. 2. (a) Schematic view of Si-H bond breaking, atomic and molecular Hydrogen diffusions and their interconversion at $Si/Si0_2$ interface and inside oxide dielectric. (b) Atomic and molecuar Hydrogen concentration in oxide layer.

a higher time exponent of n=1/4 [10]. Later refinements of the model possess a lower time exponent of n=1/6, especially for longer stress time [9]. A recently proposed model [9, 12], initially suggests a higher time exponent, and a lower exponent if stress is maintained for longer time. In the following subsections we first review the RD model [9] and thereafter give a brief discussion about impact of scaling on the model sub-processes.

2.1 Reaction Diffusion Model

RD model explains physics of NBTI degradation in term of different sub-processes. According to the model, NBTI degradation originates from Silicon Hydrogen bonds (≡Si-H) breaking at Silicon-Silicon dioxide (Si-SiO_2) interface during negative stress (V_{gs}=-V_{dd}), as shown in Fig. 2(a). The broken Silicon bonds (≡Si-) act as interface traps that are responsible for higher V_{th} and lower drain current. The number of interface traps (N_{IT}) depends on ≡Si-H bond breaking rate (k_f) and ≡Si- bond recovery rate (k_r). The N_{IT} generation rate can be written as [5]:

$$\frac{dN_{IT}}{dt} = k_f(N_o - N_{IT}) - k_r N_{IT} N_H^0, \tag{1}$$

where N_o and N_H^0 denote initial bond density and Hydrogen density at the Si-SiO_2 interface. The H atoms released from ≡Si-H bond breaking contribute to three sub-processes including: (a) diffusion towards the gate, (b) combination with other H atoms to produce H_2, or (c) recovery of the broken bonds. Similarly, H_2 participate in the diffusion towards poly gate or dissociation to produce H atoms. All these sub-processes are schematically shown in Fig. 2(a). The figure shows that N_{IT} is limited by these sub-processes. These sub-processes are formulated as [12]:

$$\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2} - k_H N_H^2 + k_{H_2} N_{H_2}, \tag{2}$$

$$\frac{dN_{H2}}{dt} = D_{H2} \frac{d^2 N_{H2}}{dx^2} + \frac{1}{2} k_H N_H^2 - k_{H2} N_{H2}, \tag{3}$$

where N_H and N_{H_2} are densities, D_H and D_{H_2} are diffusion rates, while k_H and k_{H_2} are interconversion rates of H and H_2 respectively. The model (Eq. 1-3) show that N_{IT} depends on rates of several sub-processes.

Based on Huldun and Alam's refinement of RD model [9], distinct triggering requirements of each sub-process results in four distinguished stages of N_{IT} generation. At very early stress time, N_{IT}=$N_H$$\sim$ 0, so the broken bond recovery, atomic and molecular Hydrogen interconversion as well as diffusions sub-processes are negligible. Under such conditions N_{IT} depends upon ≡Si-H bond breaking rate i.e. $N_{IT}(t) = k_f N_o t$.

During the second stage, the bond breaking domination continues to produce H atoms. The H atoms either participate in broken bonds recovery or interact with H atoms to produce H_2 molecules . However, due to lower H and H_2 densities, the diffusion sub-processes are negligible. Therefore, after re-arranging Eq.1 and Eq.2, the N_{IT} is given by [12]:

$$N_{IT}(t) = \left(\frac{k_f N_o}{k_r}\right)^{2/3} (k_H t)^{1/3}. \tag{4}$$

The third stage is very short. In this stage ≡Si-H bond breaking, H diffusion, and broken bond recovery sub-processes dominate the N_{IT} generation. The H_2 diffusion and dissociation sub-processes are still negligible [9] and N_{IT} is given by solving Eq. 1 and Eq.2, as following:

$$N_{IT}(t) = \left(\frac{k_f N_o}{k_r}\right)^{1/2} (D_H t)^{1/4}. \tag{5}$$

During the last stage, most of the H atoms are converted to H_2, so sub-processes related to H_2 become dominant. The H_2 diffuses in SiO_2 layer, and dissociates to produce H atoms inside oxide layer. Under such conditions the N_{IT} is obtained by solving Eq. 1 and Eq. 3 [12]:

$$N_{IT}(t) = \left(\frac{k_f N_o}{k_r}\right)^{2/3} \left(\frac{k_H}{k_{H_2}}\right)^{1/3} (6 D_{H2} t)^{1/6}. \tag{6}$$

The model solutions given in (Eq. 4-6) show that interface traps generation process and consequent degradation manifest itself from different sub-processes. These sub-processes have the distinct activation requirement, that causes time exponent variation ($n = 1, 1/3, 1/4, 1/6$) for shorter and longer stress time in the RD model.

2.2 Scaling Impact on NBTI

Scaling PMOS transistors escalate NBTI degradations due to two prevailing trends: (a) Voltage scaling can not keep up with the oxide layer scaling resulting in higher gate oxide field (E_{ox}) [5], and (b) Introduction of nitrogen to prevent boron diffusion, reduce leakage, and decrease hot carrier injection [5].

The higher oxide field does not affect NBTI sub-processes related to neutral hydrogen formation, diffusion and dissociation (see Eq. 4-6). However ≡Si-H bond breaking sub-process accelerates significantly with increase in oxide field. The breaking rate dependency on oxide field can be written as [15]:

$$k_f \propto p \times T \times e^{-(E_{Fo} - a \times E_{ox})/k_B T}. \tag{7}$$

The k_f acceleration is due to its three fold E_{ox} dependence: (a) The number of weaker ≡Si-H bonds p at the interface depends upon E_{ox} i.e. $p \propto E_{ox}$, (b) the inversion layer hole tunneling depth into the ≡Si-H bond depends on the transmission coefficient (T), that varies exponentially with E_{ox} i.e. $T \propto exp^{\gamma_T E_{ox}}$ [15], and (c) the barrier potential E_{Fo} required to generate interface traps decrease by factor ($a \times E_{ox}$) with E_{ox} (as shown in Eq.7).

The introduction of nitrogen accelerate NBTI degradation. Since it contributes to the following sub-processes:

- Nitrogen decreases activation energy of the ≡Si-H bond breaking sub-process and thus speed up the interface traps generation rate (see Eq.1).
- The nitrogen atoms piles up near the Si-SiO_2 interface and reduces diffusivity of H and H_2 towards Si-SiO_2 interface [16]. The reduced diffusivity implies that ≡Si- bond recovery sub-process slows down leading to high NBTI degradation.

3 NBTI Model with Temperature Variation

RD model assumes that NBTI degradation is temperature dependent, but does not give any physical basis for such dependency [12]. Similarly, the origin of temperature increment in scaled PMOS transistors and its impact on NBTI degradations have not been explored in the model. In this section, we describe the origin of temperature increment in scaled PMOS transistors and its impact on RD model sub-processes.

In order to meet the 30% delay reduction in each successive technology generation, the hole speed in PMOS inversion layer has to increase. The fast moving holes break ≡Si-H bonds at Si-SiO_2 interface. Analysis reveals that approximately 0.2-0.3eV energy is consumed to bring a hole close to ≡Si-H bond [19]. The interaction results in breaking of ≡Si-H bond, producing an interface trap and H atom with 1.3eV energy release. Therefore, the net energy gain due to a single interface trap production is 1.1eV [19]. The energy gain raises the temperature to T_{max} from a reference temperature T_{ref} (25°C). Some of the released energy is consumed by recovery of the broken ≡Si- bonds. Therefore, the temperature T(t) at any stress instant t can be modeled by a sinusoidal wave [14], as given by:

$$\begin{aligned} T(t) = &[(1/2)(T_{max} + T_{ref})] \\ &+ [(1/2)(T_{max} - T_{ref})sin(2\pi ft)], \end{aligned} \tag{8}$$

where f is the thermal frequency. Impacts of the temperature increment on rate co-efficients (D_H, D_{H_2}, k_H, k_{H_2}, k_f, and k_r) of RD model are described below.

Temperature dependence of diffusion rates

The diffusion sub-processes in oxide layer follows Fick's law e.g. D_H decreases linearly with decreasing H density from Si-SiO_2 interface. Alam used a simple approximation in the law, and suggested a triangular profile for D_H as shown in Fig. 2(b) [5]. Temperature variation strongly effects the diffusion rates D_H and D_{H_2}. The effect is based on Arrhenius relation [13], which can be written as:

$$D_H = D_{H_o} exp\left(-\frac{E_a}{kT}\right), \tag{9}$$

where D_{H_o} is the diffusion rate at T_{ref}, E_a is the activation energy, k is Bolzmann's constant, and T is temperature. The equation describes H diffusion, but the same applies to H_2 diffusion. The diffusion variation with temperature increment from T_{ref}, to $T(t)$ is given by diffusion ratio [14]:

$$D_H[T(t)] = \frac{D_{T(t)}}{D_{ref}} = exp\left[\frac{E_a}{k}\left(\frac{1}{T_{ref}} - \frac{1}{T(t)}\right)\right], \tag{10}$$

The equation shows that the temperature increment accelerate D_H. The D_H acceleration towards gate attenuate the ≡Si- broken bond recovery sub-process at Si-SiO_2 interface and hence increases the N_{IT}.

Temperature dependence of conversion rate

The PMOS negative gate stress breaks ≡Si-H bonds at Si-SiO2 interface resulting in ≡Si- broken bonds and H atoms by the following reaction:

$$\equiv Si - H \rightarrow H + \equiv Si -, \tag{11}$$

Most of the H atoms released convert to H_2 molecules. The H to H_2 conversion at Si-SiO2 interface and inside SiO_2 is a complex mechanism. We assume that the conversion takes place when a free H atom approaches a ≡Si-H bond within a distance of $r_H < 1.0$nm and break it by reaction [20]:

$$\equiv Si - H + H \xrightarrow{k_H} \equiv Si - + H_2, \tag{12}$$

where k_H is the rate constant of H to H_2 conversion. The temperature impact on conversion can be understood by inspecting the rate constant k_H [20], as:

$$k_H[T(t)] = 4 \times \pi . D_H[T(t)] . r_H . \xi_{1(x)}. \tag{13}$$

For atomic Hydrogen diffusion the parameter $\xi_1(x)$ is equal to $\sim 10^{-4}$. The temperature impact on k_H comes from two parts. First, since the conversion takes place when Hydrogen approaches at distance $r_H < 1.0nm$ to a ≡Si-H bond, the Hydrogen diffusion is involved, and [see Eq. 10] shows the temperature dependence of diffusion. Second, at higher temperature the ≡Si-H bonds vibrate that bring H atoms and ≡Si-H at $r_H < 1.0nm$, and hence accelerate k_H subprocess.

Temperature dependence of reaction rates

The RD model predicts that N_{IT} during stress phase mainly depends on ≡Si-H bond breaking and ≡Si- broken bond recovery sub-processes. The rates k_f and k_r depend on oxide layer temperature. The dependence can be expressed as [5]:

$$k_f T[(t)] \propto E_{ox} . exp(E_{ox}/E_o) . exp(E_a(k_f)/E_o)/kT(t),$$

$$k_r T[(t)] \propto exp(E_a(k_r)/E_o)/kT(t), \tag{14}$$

where E_{ox} is the oxide field and E_o is the field acceleration constant. While $E_a(k_f)$ and $E_a(k_r)$ are k_f and k_r activation energies respectively. The equation shows temperature increment increases e.g. k_f, that in turn increases N_{IT}. The increment is significant in first stage of Alam and Huldun model [9]. However, at intermediate and longer stress time, both k_f and k_r take place in parallel. Under these condition ratio between k_f and k_r is used, as given by [5]:

$$\frac{k_f}{k_r} \propto E_{ox} exp(E_{ox}/E_o) exp[-E_a(k_f) + E_a(k_r)]/kT. \tag{15}$$

Simulation results supported by industrial data reveal that quick recovery of ≡Si- bonds during recovery phase is due to the fact that $E_a(k_f) \approx E_a(k_r)$. If the E_a's were different, it would be impossible for H atoms to recover ≡Si- bonds during recovery phase [15]. Considering $E_a(k_f) \approx E_a(k_r)$, we obtained:

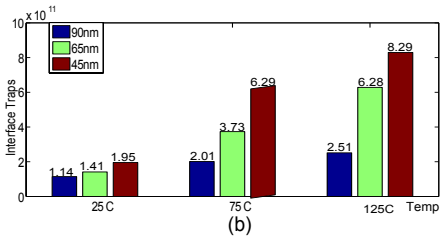
$$\frac{k_f}{k_r} \propto E_{ox} exp\left(\frac{E_{ox}}{E_o}\right), \tag{16}$$

The equation shows that when k_f and k_r take place in parallel, the reaction rates become temperature independent.

In conclusion, Eq. [10,13,14,16] present the temperature impact on NBTI subprocesses. By considering the impacts, N_{IT} during the four stages [see section 2] is given by:

MOS Tech.	90nm	65nm	45nm
V_{dd} (V)	1.2	1.1	1.0
T_{ox} (nm)	2.05	1.85	1.75
L_{eff} (nm)	35	24.5	17.5
V_{th}(V)	0.284	0.289	0.292

(a)



(b)

Fig. 3. (a)Equivalent parameters of PTM models (b) Number of Interface traps in different technologies at different temperatures.

$$N_{IT(T(t))} = (E_{ox}.exp(E_{ox}/E_o).exp(E_a(k_f)/E_o)/kT(t))).(N_o.t) \quad (17a)$$

$$N_{IT(T(t))} = (N_o.E_{ox}.exp(E_{ox}/E_o))^{2/3}.(t.k_H[T(t)])^{1/3} \quad (17b)$$

$$N_{IT(T(t))} = (E_{ox}.exp(E_{ox}/E_o.N_o))^{1/2}.(D_H[T(t)].t)^{1/4}.(t_{eq1})^{1/4} \quad (17c)$$

$$N_{IT(T(t))} = (E_{ox}.N_o.expE_a/E_o)^{2/3}.(k_H[T(t)]/k_{H2})^{1/2}.(D_{H2}[T(t)].t)^{1/6} \quad (17d)$$

We consider equivalent parameters for 90nm, 65nm, and 45nm PMOS transistor models as shown in fig.3(a) [21], and take three temperatures, 25°C, 75°C, and 125°C as an example. The numeric simulation results of the equations are given in the Fig 3(b). Analysis of figure shows that:

- For agiven technology and stress duration, the N_{IT} depends on the stress temperature. For example, for 65nm technology and 10^5sec stress duration N_{IT} are 1.41×10^{11} at 25°C, while the count approaches to 6.28×10^{11} at 125°C. The N_{IT} increment results from different sub-processes acceleration with rise in temperature.
- For a given range of temperature increment and stress duration, the increment in N_{IT} count is higher for smaller technologies. For example, after 10^5sec stress for 90nm and temperature increment from 25°C to 125°, the increment in N_{IT} is (2.51-1.14)$\times10^{11}$=1.37×10^{11}. If the same stress time and temperature increment are considered for 65nm and 45nm model parameters, the N_{IT} increment reach to 4.87×10^{11} and 6.34×10^{11} respectively. The N_{IT} growth under given conditions results from E_{ox} increment with technology scaling.

4 Simulation and Analysis

In this section, we present simulation results and key insights observed from the result analysis. We use Predictive Technology Model (PTM) 90nm, 65nm, and 45nm Bulk PMOS transistor models. NBTI impact on PMOS transistor is modeled using an external voltage source (V_{NBTI}) as shown in Fig.4(a). (V_{NBTI}) source opposes applied gate voltage in HSPICE net list. Behavior of the source is modeled using a Verilog-A module (V_{NBTI}) as shown in Fig. 4(b). Inputs to the module circuit are temperature $T(t)$, biasing voltage V_{dd}, and transistor physical parameter e.g., T_{ox}. The voltage across the module $V_m(+,-)$ represents the PMOS transistor threshold voltage degradation due to NBTI at any instant of time. Other degraded parameter is PMOS transistor drain current. Temperature impact on these parameters in different technologies are described below.

The most obvious impact of NBTI is the increase in threshold voltage of PMOS transistors. Fig. 5 validates this increment for different PMOS transistor

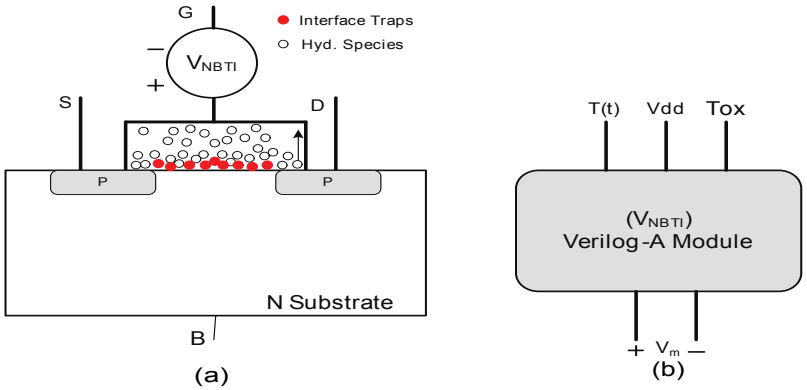


Fig. 4. (a) PMOS transistor transistor degradation due to NBTI. (b)The Verilog-A source representing NBTI degradation at different temperature.

models. The figure shows that after 10^5sec of stress application at 25°C, the threshold voltage shifts are 17.68mV, 18.22mV, and 20.68mV for 90nm, 65nm, and 45nm PMOS transistors respectively. When the temperature is raised to 125°C the voltages shift approach to 23.96mV, 25.74mV and 29.81mV in the respective PMOS transistors. By observing the additional shifts of 6.01mV for 90nm, 7.52mV for 65nm, and 9.31mV for 45nm MOS technology, we can conclude

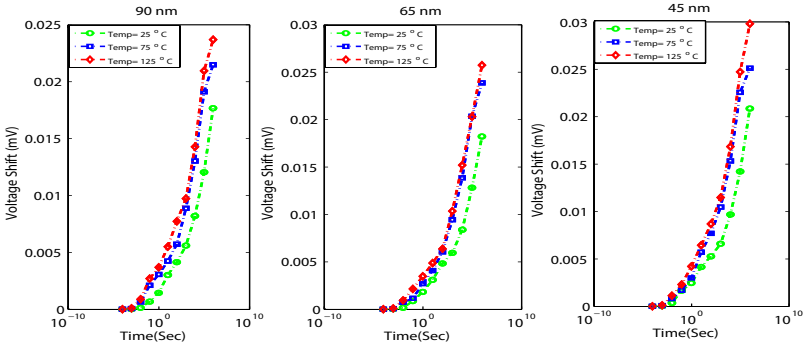


Fig. 5. Threshold voltage shift in 90nm, 65nm, and 45nm transistors due to NBTI degradation under temperature variation.

that

- The same range of temperature variation (25°C to 125°C) and stress time (10^5sec) causes higher voltage shift in 45nm technology (approx. 42%) as compared to 90nm technology (approx. 34%).
- The 45nm MOS technology chip operates at higher temperature than 90nm technology chip. Therefore, 45nm PMOS transistor will reach to the limit of voltage shift earlier than other technologies.

PMOS transistor drain current degradation is another important metric of NBTI degradation. We measure the drain currents at time $t = 0$sec for 90nm, 65nm, and 45nm PMOS transistors as reference. The drain current measured after 10^5sec stress for each technology at 25^{o}C, 75^{o}C, and 125^{o}C are shown in the Fig. 6. The figure shows that percent current degradations is higher for 45nm

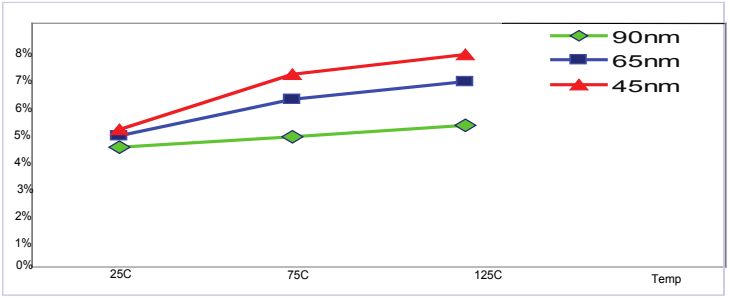


Fig. 6. Percent (%) drain current decrease after 10^{+5}sec stress.

PMOS transistors as compared to 90nm. The systematic current degradations for each stress time and temperature are tabulated in Table 1. From the table we can observe two obvious trends:

Tech. Node	90nm			65nm			45nm		
Temp °C	25 °C	75°C	125°C	25°C	75°C	125°C	25°C	75°C	125°C
$10^{-05}(sec)$	0.00	0.0	0.00	0.00	0.00	0.00	0.00	0.00	0.00
$10^{-03}(sec)$	0.02	0.10	0.14	0.10	0.15	0.17	0.13	0.21	0.17
$10^{-01}(sec)$	0.25	0.33	0.35	0.33	0.28	0.42	0.52	0.64	0.62
$10^{+01}(sec)$	0.70	0.98	1.09	0.97	1.048	1.30	1.20	2.23	1.45
$10^{+03}(sec)$	1.42	2.24	2.43	2.24	3.96	2.99	2.32	3.46	3.68
$10^{+05}(sec)$	3.42	4.82	5.22	4.83	6.20	6.86	5.03	7.50	7.85

Table 1. Transistor percent current degradation under various temperatures.

- For a given PMOS technology (90nm, 65nm, or 45nm) and temperature (25^oC, 75^oC, or 125^oC), the drain current degradation increases with increase in stress time. For example, after 10^{+1}sec the current degradation of 90nm PMOS transistor at 25^oC, is 0.7%. However if the stress is maintained for 10^{+5}sec, the current degradation approaches to 3.4%.
- For a given stress time and temperature the current degradation is very significant for smaller PMOS technology. For instance, after 10^5sec stress at 125°C temperature, the percent current degradation for 90nm, 65nm are 5.2%, 6.8% respectively, however for 45nm technology the degradation approaches to 7.8% under same conditions.

5 Conclusion

In this paper, we have analyzed temperature impact on sub-processes of NBTI. Our analysis are based on numerical solutions of the RD model which consider different sub-processes. We observed that majority of the NBTI sub-processes are temperature dependent and accelerate with technology scaling. We have implemented the temperature impact on NBTI sub-processes in HSPICE using Verilog-A, and conducted simulations for 90nm, 65nm, and 45nm PTM Bulk PMOS models. Our simulation results revealed that performance of scaled PMOS transistors are more effected at higher temperatures. For example, at 125°C and 10^{+5}sec stress time: a) the voltage shift increment of 90nm PMOS transistor was

34%, while it approached to 38% and 42% for 65nm and 45nm PMOS transistors respecively, and b) For 90nm MOS transistor the drain current decreased by 5%, while for 45nm the was 8%. Overall our analysis provide a solid basis to conclude that, temperature increment in scaling technologies exacerbate NBTI degradation.

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