Modeling and Mitigating NBTI in Nanoscale Circuits

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***Abstract*—As semiconductor manufacturing has entered into nanoscale era, performance degradation due to Negative Bias Temperature Instability (NBTI) became one of the major threats to circuits reliability. In this paper, we present an NBTI gate delay model and a technique to mitigate its impact on circuit delays. First, we model NBTI impact on a gate while considering both the degradation of its own transistors and that of transistors in the adjacent gates. Simulation of our model on some ISCAS-85 benchmark circuits reveal that NBTI can cause up to 19.00% additional delay to a gate due to its own transistors degradation and up to 4.80% delay due to transistors degradation in adjacent gates after 10 years operation, resulting in a total delay of 23.80%. Therefore, we propose a transistor sizing techniques that not only mitigates NBTI induced delay of the gate under consideration but also minimizes its impact on the adjacent gates. Preliminary results of the mitigation technique applied to ISACAS-85 benchmark circuits show that with an average of 12% area overhead, the circuit delay will not exceed 15% after 10 years operation (i.e.; the introduced sizing technique realizes a delay reduction of about 45% as compared to the original circuit).**

I. Introduction

With the relentless pursuit for smaller CMOS process technologies, failures due to aging mechanisms have become a limiting factor for transistor/circuit reliability [1]. Industrial data reveal that as oxide thickness reached 4nm, Negative Bias Temperature Instability (NBTI) has become one of the most significant aging mechanisms [2,3]. NBTI degrades the performance of PMOS transistors under negative gate stress including: (a) threshold voltage increment, (b) drain current reduction, and (c) delay increment [4,5]. These effects manifest themselves at the circuit level by increasing circuit delays, or in extreme cases causing the circuit timing/functional failures.

There is an escalation of interest to investigate NBTI mechanism at transistor level and model its delay at gate level. The analytical gate delay models proposed so far [6,8,9] only consider NBTI induced degradation due to transistors in the gate under consideration. These models ignore the impact of degraded transistors in connected adjacent gates. However, it has been shown that the degraded gates also impact the delays of their adjacent neighbors [10,11]. Therefore, an appropriate analytical NBTI gate delay model is needed for accurate gate and circuit delay assessment.

Apart from delay modeling, circuit designers have focused on NBTI induced delay mitigation by using transistor sizing [13–16]. This technique estimates the delay increment due to NBTI induced degradation in transistors of the gates under consideration and compute optimal sizes for transistors to mitigate the gate delay. However, they ignore the fact that changing sizes of transistors in gates will affect the performance of adjacent gates [11]. Therefore, an optimal sizing technique has to consider the impact on adjacent gates and the optimization should be global (i.e.; at the circuit level) and not only local (i.e.; at the gate level).

This paper addresses the two shortcomings mentioned previously; it presents a novel NBTI gate delay model that considers both the degradation due to its own transistors as well as the degradation of transistors of the adjacent gates. Moreover, the paper presents a two steps transistor sizing technique to mitigate NBTI induced delay. The two steps are as follows:

(a) **Unconstrained sizing:** Transistors sizes are increased without any constraint to keep NBTI gate delay values below a desired threshold values.

(b) **Size optimization:** Transistors sizes obtained in the previous step are optimized for minimum area under the constraint of the threshold delay values. The technique minimizes the area of transistors in all the gates and ensures that the delay values of the current and adjacent gates are below the targeted value.

Simulation results of our novel gate delay model show that after 10 years operation, NBTI can cause up to 19.00% additional gate delay due to its own transistors degradation and up to 4.80% due to transistors degradations in the adjacent gates. Moreover, the simulation results of applying our sizing technique to several ISCAS-85 benchmark circuits show that the unconstrained sizing technique has an area overhead similar to that of the conventional techniques [13,14]. Furthermore, sizing optimization reduces the area overhead by 50% as compared to the unconstrained sizing and still maintain the delay values below the targeted 15% for 10 years operation.

The rest of the paper is organized as follows. Section II describes NBTI mechanism and a conventional gate delay model. Section III proposes an NBTI induced gate delay model that considers NBTI induced degradation of its own transistors and degradation of transistors in adjacent gates. Section IV models NBTI as a transistor sizing problem and presents our approach to solve it. Section V presents a technique to size transistors in an unconstrained manner to mitigate NBTI. Section VI optimizes the unconstrained sizing for minimum

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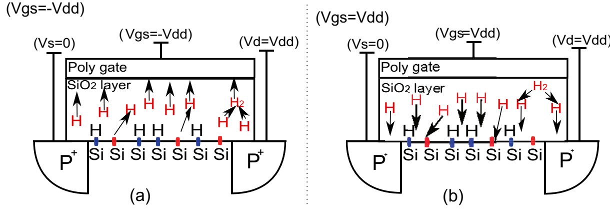

Fig. 1. Schematic view of (a) Si-H bond breaking, H and H_2 diffusions toward poly gate and their interconversion at Si/SiO_2 interface and inside oxide dielectric under negative gate stress (b) H and H_2 diffusions toward the Si-SiO_2 interface and ≡Si- bond recover under positive gate stress

area overhead. Finally, Section VII concludes the paper.

II. NBTI Mechanism and a Delay Model

This section shortly describes NBTI mechanism including NBTI induced threshold voltage increment; it also gives the well known conventional gate delay model.

A. NBTI Mechanism

NBTI degradation is characterized by the threshold voltage increment of PMOS transistor under negative gate stress. The degradation originates from Silicon Hydrogen bonds (≡Si-H) breaking at Silicon-Silicon dioxide (Si-SiO_2) interface as shown in Fig. 1(a). The broken Silicon bonds (≡Si-) act as Interface Traps near the Si-SiO_2 interface and the H atoms/molecules diffuse towards the poly gate. The *number of interface traps (N_{IT})* depend on ≡Si-H bond breaking rate (k_f) and ≡Si- bond recovery rate (k_r). A well known model for N_{IT} as a function of time t is presented in [6]:

$$N_{IT}(t) = \left(\frac{k_f N_o}{k_r}\right)^{2/3} \left(\frac{k_H}{k_{H_2}}\right)^{1/3} (6D_{H2}t)^{1/6} \qquad (1)$$

where N_o, k_H, k_{H2}, and D_{H2} represent initial bond density, H to H_2 conversion rate, H_2 to H conversion rate, and H_2 diffusion rate inside SiO_2 layer, respectively. The N_{IT} are assumed to be positive charges remaining at the Si-SiO_2 interface that oppose the applied gate stress resulting in threshold voltage increment (ΔV_{th}). The relation between N_{IT} and ΔV_{th} is [4]:

$$\Delta V_{th} = (1+m)qN_{IT}/C_{ox} \qquad (2)$$

where m, C_{ox}, and q are holes mobility degradation that contribute to V_{th} increment [5,12], oxide capacitance and electron charge, respectively. NBTI annealing takes place under positive gate stress; in this case, the H atoms anneal back towards the Si-SiO_2 interface as shown in Fig.1(b). The H atoms anneal the ≡Si- bonds at Si-SiO_2 interface resulting in less N_{IT} and consequently less ΔV_{th}.

B. Conventional Gate Delay Model

In a widely used model, the contribution of NBTI induced transistor degradation to gate delay is formulated as [6]:

$$\Delta D = K\frac{\alpha \Delta V_{th}}{(V_{gs} - V_{th})} D_o \qquad (3)$$

where K is a constant that represents technology dependent parameters, α is the velocity saturation index, and D_o is the delay without NBTI. Clearly, the model represents the degradation of PMOS transistors (due to ΔV_{th}) that manifest the gate itself; the model does not consider NBTI induced transistors degradation in adjacent gates that affect the gate delay [11].

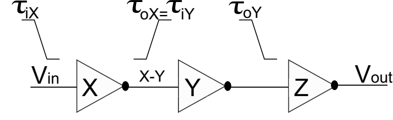

Fig. 2. An example to illustrate NBTI impact on a gate delay

III. Proposed Gate Delay Model

Traditionally, NBTI induced circuit delay is analytically modeled in two phases: (a) the delay is analytically modeled for each isolated gate, and (b) the isolated gate delays are added together to get the circuit model [6,8,9]. In reality, however, gates in a circuit are not isolated and so are their delays [10].

Fig. 2 will be used to illustrate how NBTI induced ΔV_{th} of PMOS transistor in an inverter affects the delay of the inverter itself and the delays of the adjacent inverters. NBTI causes threshold voltage increments ΔV_{th_X} and ΔV_{th_Y} to the PMOS transistors in inverters X and Y, respectively. The ΔV_{th_X} of inverter X increases input transition time of inverter Y (τ_{i_Y}). The increments in the ΔV_{th_Y} and τ_{i_Y} cause additional delays to inverter Y (ΔD_Y), as given by:

$$\Delta D_Y = \Delta D_{int_Y} + \Delta D_{fed_Y}, \qquad (4)$$

where ΔD_{int_Y} and ΔD_{fed_Y} are additional delays due to ΔV_{th_Y} and τ_{i_Y} increments respectively. Henceforth, we will refer to ΔD_{int_Y} as *Intrinsic delay* and ΔD_{fed_Y} as *Front-end delay* of inverter Y.

In the rest of the section, we develop an NBTI gate delay model; the model takes *both* intrinsic and the front-end delays into consideration.

Intrinsic Delay Model: Intrinsic delay of inverter Y (see Fig. 2) in the absence of NBTI depends on V_{th} of the transistors that make inverter Y. A simple yet accurate analytical formulation of this dependence is given by [11]:

$$D_{int_{o_Y}} = \frac{\gamma A}{(V_{gs_Y} - V_{th_Y})^{\alpha}}$$

where γ is the switching activity (i.e. the ratio of the input signal that stresses PMOS transistor to the total input cycle) and A is a technology dependent constant. Intrinsic delay due to NBTI is obtained by taking the differential of the above equation w.r.t. V_{th_Y} [6]; this results into:

$$\Delta D_{int_Y} = \alpha A \frac{\gamma \Delta V_{th_Y}}{(V_{gs_Y} - V_{th_Y})} D_{int_{o_Y}} \qquad (5)$$

the parameters of 45nm PMOS transistor model [18] are used to get ΔV_{th_Y} and ΔD_{int_Y} for 10 years operation. Throughout the simulation, the parameters used to estimate ΔV_{th} are taken from [4]: k_f= 8 $\times 10^{-4}s^{-1}$, k_r=3$\times 10^{-18}cm^3s^{-1}$, N_o= 5$\times 10^{16}cm^2$, D_{H2}=4$\times 10^{-21}cm^2s^{-1}$, T = 125$^oC$ etc. To

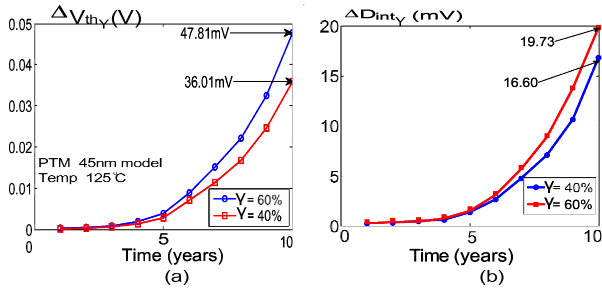

Fig. 3. (a) ΔV_{th} increment as a function of time under different γ values, (b) ΔD_{int_Y} of inverter Y with no degradation in the preceding inverter X

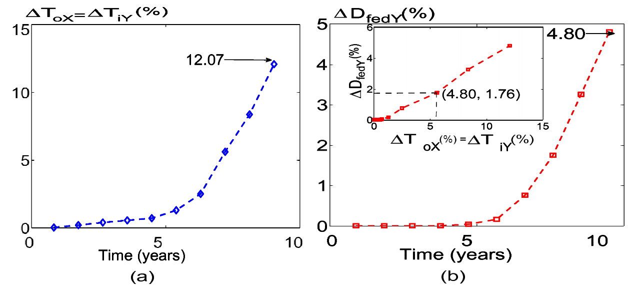

Fig. 4. (a) $\Delta\tau_{ox}$ due to NBTI induced V_{th_X} at γ=50% (b) ΔD_{fed_Y} variation with time at γ=50%

isolate the intrinsic delay from front-end delay, we assume that inverter X does not degrade due to NBTI resulting in ΔD_{fed_Y}=0 and the additional delay in inverter Y is only due to its PMOS transistor degradation. Fig. 3(a) shows ΔV_{th_Y} due to NBTI for various γ values. As expected, the curves follow the $t^{1/6}$ trends presented in Eq. 1 and increase with increasing γ values approaching 47.81mV for γ=60%. Additionally, the delay ΔD_{int_Y} caused by ΔV_{th_Y} is shown in Fig.3(b); it clearly follows the same trends as ΔV_{th_Y} and approaches 19.73% for γ=60%.

Front-end Delay Model: The output current of inverter X (see Fig. 2) is equivalent to the drain saturation current (I_{dsat}) of its active transistor, which is given by [11]:

$$I_{dsat_X} = \mu B(V_{gs_X} - V_{th_X})^{\alpha} \quad (6)$$

where μ is the hole mobility in the PMOS transistor and B is a technology dependent constant. It has been argued that I_{dsat_X} along with the inverter output load capacitance (C_L) and V_{dd} determine the output transition time of X (τ_{o_X}) as [17]:

$$\tau_{o_X} = \frac{C_L V_{dd}}{I_{dsat_X}} = \left(\frac{C_L V_{dd}}{\mu B}\right)\left(\frac{1}{(V_{gs_X} - V_{th_X})^{\alpha}}\right) \quad (7)$$

To get only the impact of τ_{o_X} on ΔD_Y (i.e., ΔD_{fed_Y}), we assume that the interconnect between X and Y (see Fig. 2) have zero delay and τ_{o_X} of a inverter X is equal to the input transition time of inverter Y; i.e., $\tau_{o_X} = \tau_{i_Y}$. For a given value of velocity saturation index α and voltage gain (ν_t) of the active transistor in inverter Y, we model the inverter delay (D_{fed_Y}) as a function of τ_{i_Y}=τ_{o_X} as follows [11]:

$$D_{fed_Y} = \left(\frac{\alpha + \nu_t}{1+\alpha}\right)\cdot\left(\frac{C_L V_{dd}}{\mu B}\right)\cdot\left(\frac{1}{(V_{gs_X} - V_{th_X})^{\alpha}}\right)$$
$$D_{fed_Y} = \frac{1}{(V_{gs_X} - V_{th_X})^{\alpha}}.C \quad (8)$$

where

$$C = \left(\frac{\alpha + \nu_t}{1+\alpha}\right)\cdot\left(\frac{C_L V_{dd}}{\mu B}\right)$$

The increment in τ_{o_X} due to NBTI induced PMOS transistor degradation in inverter X and its impact on ΔD_{fed_Y} is achieved by differentiating Eq. 8 w.r.t V_{th_X}. After expansion of the results using Taylor series and neglecting the higher order terms, the front-end delay is:

$$\Delta D_{fed_Y} = \left(\frac{\alpha \Delta V_{th_X}}{V_{gs_X} - V_{th_X}}\right).C \quad (9)$$

Consider again the circuit in Fig. 2. To isolate the front-end delay of inverter Y from intrinsic delay we assume that inverter X suffers only from intrinsic delay (due to NBTI) and inverter Y suffers only from ΔD_{fed_Y} due to τ_{i_Y} increment and D_{int_Y}=0. The delay measurement was taken from HSPICE simulation using 45nm PMOS transistor model [18]. The measurements include τ_{ox} and ΔD_{fed_Y}. Fig. 4(a) shows τ_{o_X} increment due to the degradation of PMOS transistor of inverter X. It follows the same trend as that of V_{th_X} increment; see Fig. 3(a). Fig. 4(b) shows the percentage ΔD_{fed_Y} increment and the inset shows the percentage ΔD_{fed_Y} increment against the percentage $\Delta\tau_{i_Y}$ increment. The figure shows that ΔD_{fed_Y} follows the same trend as ΔD_{int_Y}; see Fig. 3(b). However, increment of ΔD_{fed_Y} is less than that of ΔD_{int_Y}. This can be understood from Eq. 8 and Eq. 9. Since $\alpha > 1$ and $v_t < 1$ that causes smaller C and lower ΔD_{fed_Y}. The inset shows that ΔD_{fed_Y} increases linearly with $\Delta\tau_{i_Y}$. However, such an increment is smaller than that of ΔD_{int_Y} and 4.80% increment in τ_{i_Y} causes only 1.76% ΔD_{fed_Y}.

An appropriate model of NBTI has to take both intrinsic and front-end delays into consideration; combining equations 5 and 9 gives such a model. Substituting these two terms in Eq. 4 results in additional delay of inverter Y:

$$\Delta D_Y = \left(\frac{\alpha \Delta V_{th_Y}}{V_{gs_Y} - V_{th_Y}}\right).A + \left(\frac{\alpha \Delta V_{th_X}}{V_{gs_X} - V_{th_X}}\right).C \quad (10)$$

Since the model presented in the equation considers *both* impacts of NBTI induced transistor degradation in its own and the adjacent gates, it is more suitable for the circuit delay assessment.

Circuit Delay Model: The gate delay in Eq. 10 is used to model NBTI induced delay of circuit with n gates as follows:

$$\Delta D_{circ} = \sum_{i=1}^{n} \Delta D_{int(i)} + \sum_{i=2}^{n} \Delta D_{fed(i)} \quad (11)$$

where $\sum_{i=1}^{n} \Delta D_{int(i)}$ and $\sum_{i=2}^{n-1} \Delta D_{fed(i)}$ are the summation of intrinsic delays and front-end delays, respectively.

To demonstrate NBTI induced circuit delay, we consider the ISCAS-85 C17 benchmark circuit as shown in Fig. 5(a). The ΔV_{th} of Eq. 2 was integrated in the circuit to compute delays the gates. Delay increment measurements taken from HSPICE simulation using 45nm PMOS transistor model are given in Fig. 5(b). The key insight of the figure reveals that:

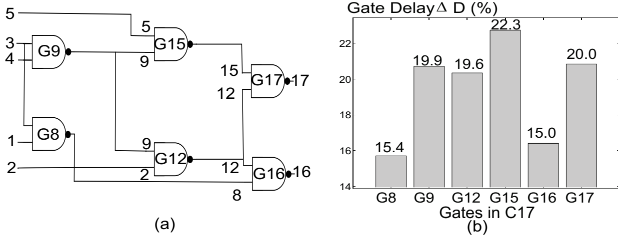

Fig. 5. (a) Schematics of C17 ISCAS-85 benchmark circuit,(b) $\Delta \mathrm{D_Y}$ of gates in the benchmark circuit at γ=50%

- At the same level in the circuit and at the same switching activity γ value, NBTI induced delay of a gate depends on the degradation of the succeeding gates. For example, G8 and G9 are primary gates, while G8 is succeeded only by G16 and suffers from 15.4% delay. On the other hand, G9 is followed by G12 and G16, which increases its delay to 19.9% approximately 1.3× more than G8.
- The delay of a gate is affected by the degradation of the preceding gates in the circuits. For example, the gates preceding G16 (i.e., G8, G12) are less degraded and results in only 15% delay increment for G16. However, the gates preceding G17 (i.e. G12, G15) have higher delay increments, as a result delay of G17 approaches 20%. It should be noted that both G16 and G17 have the same γ values and the difference in delay is only due to different levels of degradations in the adjacent gates.

Based on the above two observations, we propose a gate sizing technique to mitigate NBTI induced delay of a gate itself and delays of the adjacent gates.

IV. NBTI Mitigation by Transistor Sizing

In this section, we will mitigate NBTI impact on gate delay by using a well-known gate sizing approach [19]. The purpose of this approach is to resize the PMOS transistors such that delay increment will slow down and will not exceed a given limit. In our case, we will add another step to the approach: optimize the overall area overhead. In this section we formulate the problem and then briefly describe our approach to solve it.

A. Problem Formulation:

Let us consider C17 ISCAS-85 benchmark circuit of Fig. 5(a). Fig. 6 shows the directed acyclic graph (DAG) of the circuit, where each gate is represented by a node and each connection between any two gates by an edge. We associate the arrival time (t_i) attribute with each node i; t_i is the delay of the node itself (D_i) plus the largest arrival time t_j of a signal from node j at the fan-in (FI) of node i; i.e.; (t_i=D_i+t_j). We index the nodes such that the nodes at the fan-out (FO) of each node have higher indexes than the node itself. For example, nodes at FO of G12 are indexed as G16 and G17 [19]. DAG of a n gate circuit can represented by a $n \times n$ sparse matrix F.

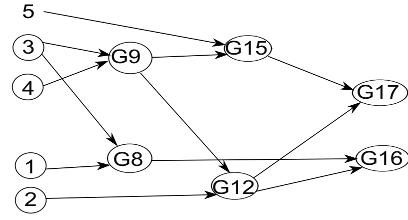

Fig. 6. Directed Acyclic Graph (DAG) of C17 ISCAS-85 benchmark circuit

For example, circuit of Fig. 5(a) can be represented as 6×6 sparse matrix as follows.

DAG	$G8$	$G9$	$G12$	$G15$	$G16$	$G17$
$G8$	0	0	0	0	1	0
$G9$	0	0	1	1	0	0
$G12$	0	0	0	0	1	1
$G15$	0	0	0	0	0	1
$G16$	0	0	0	0	0	0
$G17$	0	0	0	0	0	0

F_{ij} entry in the matrix shows adjacency of node i with node j. In addition, we relate the weighted area ($\mathrm{a}_i\mathrm{x}_i$) attribute to each node, where a_i represents the area of a gate with minimum sized transistors and $\mathrm{x}_i > 1$ is the scale factor with respect to the minimum size gate.

The gate delay depends on its own size (i.e., transistors sizes) and sizes of the adjacent gates. This dependency is [19]:

$$D_i = D_i^{min} + \frac{g_i + \sum_{j \epsilon FI(i)} F_{ij} x_j}{x_i}, i....n \quad (12)$$

where D_i^{min} is minimum delay of a gate excluding the impact of NBTI, g_i is the size gradient of gate i with respect to the adjacent gate j (i.e., size ratio between node i and j) and x_j is scale factor of the adjacent gate j. The first term in the equation represents the minimum gate delay when it is not affected by the adjacent gates and the second term shows the impact of adjacent gates sizes.

After modeling NBTI induced gate delay and relating gate delay in a circuit to transistors sizes in the gate itself and adjacent gates, we incorporate NBTI induced delay as a constraint in gate size optimization problem. Our objective is to find the minimum gate area $a_i x_i$ (i.e., to find the optimized scaling factors x_i) that ensures that delays $\Delta\mathrm{D}_i$ of all the gates are below some threshold value.

$$\begin{aligned} \text{Objective :} \quad & \text{Minimize} \sum_{i=1}^{n} a_i x_i; \\ \text{Subject to :} \quad & \Delta D_i \leq \left(\frac{g_i + \sum_{j \epsilon FI(i)} F_{ij}.x_j}{x_i} \right), \\ & \Delta D_i = t_i - t_j - D_i^{min}, j \epsilon FI(i), \\ & L_i \leq x_i \leq U_i \end{aligned}$$

where PO, t_i, t_j, L_i and U_i are primary output, arrival time attributed to gate i, arrival time attributed to gate j, lower and upper limits of gate scaling factors, respectively. Note that when gate i is a primary output, then $t_i \leq T$, where T is the critical path delay.

B. Our Approach

Our approach for mitigating NBTI induced delay using gate sizing consists of two steps as explained next.

Unconstrained sizing: In this step, we assume that the scaling factor (x_i) constraint in the above problem can be relaxed. This will transform the problem to an unconstrained optimization problem [21]. Sizes of the gates (i.e. transistors) are increased so that the worst case delay (22.3% in our example) is reduced to 15%.

Sizing optimization: Having achieved the objective of reducing gate delay below the targeted 15% even in the presence of NBTI induced degradation, we introduce the scaling factor constraint step-by-step in the gate size optimization problem. We optimize the area (i.e. transistors sizes) and still ensure that the delay is 15%.

The above approach is explained in the next sections.

V. UNCONSTRAINED SIZING

Now we havethe unconstrained optimization problem that only targets the delay requirements. This will transform the problem formulated in Section IV-A to the following:

$$\text{Objective}: \quad \text{calculate area} = \sum_{i=1}^{n} a_i x_i;$$

for a given ΔD_i

$$\text{Subject to}: \quad x_i \geq max\left(\left(\frac{g_i + \sum_{j \epsilon FI(i)} F_{ij}.x_j}{\Delta D_i}\right), 1\right)$$

$$\Delta D_i = \min_{j \epsilon FI(i)} (t_i - t_j - D_i^{min}), i = 1..n$$

To solve the above problem, initially, additional delay (ΔD_i) of each gate i ($1 \leq i \leq n$) is computed and used to determine its scaling factor x_i. The scaling factors x_i's are determined in a recursion manner that starts from the primary outputs and move towards the primary inputs. The resulting value of the objective is denoted by $\psi(t)$ and is given by:

$$area = \psi(t) = \sum_{i=1}^{n} a_i x_i \qquad (13)$$

The above procedure has been implemented in MATLAB and the scaling factors are calculated for the delay values given in Section III. Fig. 7(a) shows the scaling factors x_is required to ensure lower delays than the targeted 15% even in presence of NBTI. An important observation is that although G15 suffers from the highest delay (see Fig. 5), it does not have the highest scaling factor; the gate with the highest scaling factor is G9

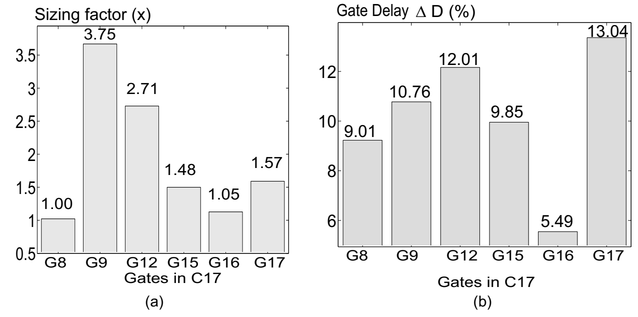

Fig. 7. (a)Scaling factors for unconstrained sizing of the C17 ISCAS-85 benchmark circuit (b) percentage delay increment of gates in C17 ISCAS-85 benchmark circuit after transistor unconstrained sizing

instead. This can be justified by the fact that higher scaling factor of G9 reduces both its own intrinsic delay as well as the front-end delay of G15. Additionally, Fig. 5(b) shows that G8 and G16 have lower delays and have minimum impact on the gates in the critical path (G9-G15-G17). Therefore, their scaling factors are smaller than the other gates. Transistors sizes in the gates are updated according to their scaling factors and the NBTI induced delays of the newly sized gates are measured from HSPICE simulation and the results are shown in Fig. 7(b). All the newly sized gates have additional delays smaller than the targeted 15%.

VI. SIZING OPTIMIZATION

In this section, the scaling factors are optimized step-by-step while ensuring that the delay is below 15% target value. The optimization is carried out using the Large Scale Gate Sizing (LSGS) technique proposd in [19,20]. Main steps are:

- Start from an *initial point*, i.e., approximate a smaller scaling factor of a gate and compute its additional delay.
- Repeat
  1) Compute *delay gradients*; i.e., delay variation of the adjacent gates.
  2) Perform the *maximum impact search;* i.e., search the maximum delay variation in the adjacent gates.
  3) Perform *line search*; i.e., calculate delay variation in all paths.
  4) Check feasibility of the scaling factor i.e., to ensure that delay of any path is less than the critical path.
- Update the objective function of the optimization problem.

Details of the above steps has been explained in [19]. For our case study, we use the same benchmark as that we used for "unconstrained sizing". NBTI induced delays from HSPICE simulation of Section III, critcal path delay and scaling factors of Section V are used as input for optimization using LSGS. Fig. 8 (a) shows that optimized scaling factors for gates are smaller than the factors presented in Fig. 7(a). Gates in the benchmark circuit are sized according to the optimized scaling factors and simulated for 10 years using HSPICE to see the impact of NBTI on the modified gates.

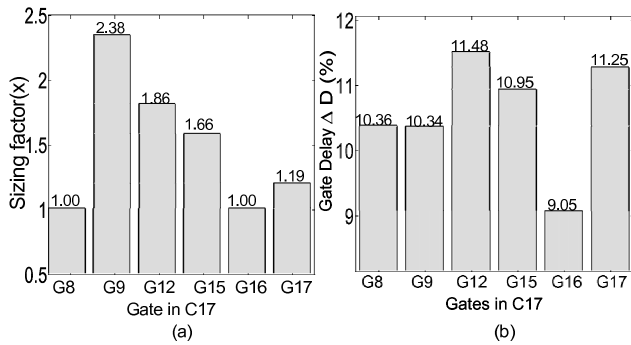

Fig. 8. (a)Scaling factors for constrained sizing of the C17 ISCAS-85 benchmark circuit (b) percentage delay increment of gates in C17 ISCAS-85 benchmark circuit after transistor optimal sizing

Fig. 8(b) shows additional delays of the modified gates. The figure reveals that ΔD's are now nearly uniformly distributed among all the gates and none of them violate the targeted 15% delay values of Section V.

Table I shows the original and modified areas by using unconstrained and optimized sizings to ensure reliability for 10 years operation. The table shows that unconstrained sizing

TABLE I
AREA ANAMYSIS OF THE PROPOSED TECHNIQUES FOR C17 ISCAS-85 BENCHMARK CIRCUIT

Gate	G8	G9	G12	G15	G16	G17	Avg.
Orig. area(μm^2)	0.6	0.60	0.60	0.60	0.60	0.60	0.60
Uncons. area(μm^2)	0.6	1.09	0.90	0.68	0.62	0.80	0.78
Uncons. Overhead(%)	0.0	81.66	50.00	13.33	3.16	33.05	29.06
Opt. area(μm^2)	0.6	0.85	0.74	0.70	0.60	0.64	0.68
Opt. Overhead(%)	0.0	41.5	24.23	18.30	0.00	5.77	13.23

Uncons.= Unconstrained, Orig.=Original, Avg.= Average, Opt.= Optimal

has an average of 29% area overhead which is similiar to the results presented in [13]. However, optimized sizing requires only 13% area overhead, resulting in 54% area saving as compared to the existing work [13].

Table II shows the area overhead results of the technique

TABLE II
AREA ANALYSIS OF THE PROPOSED TECHNIQUES FOR SOME ISCAS-85 BENCHMARK CIRCUIT

Benchmark	No of gates	Orig. area	Area-overhead(%)		
			X	Y	Area saving (%)
C432	142	295.05	24.53	11.28	55.00
C499	516	797.58	26.15	16.14	38.25
C1908	254	431.85	26.21	12.34	52.92

X=Unconstrained sizing, Y= Optimized sizing

for other ISCAS-85 benchmark circuits. The circuits were simulated for 10 years to get NBTI induced delays. The circuits were initially sized in an unconstrained manner and then by using LSGS optimization method. The resulting area overheads are shown in columns 4 and 5 of the table. The table clearly shows that an area saving of about 50% can be achieved while still ensuring that the delay satisfies the requirement of being below 15%

VII. CONCLUSION

In this paper, we modeled NBTI induced gate delay in a nanoscaled circuit. The model considers NBTI impact on transistors in the gate itself and the impact of degraded transistors in the adjacent gates. From the model simulation, we found that depending on the switching activity γ values, NBTI can cause up to 19.00% delay increment due to its own transistors degradation and up to 4.80% additional delay due to transistors degradation in the adjacent gates. Finally, we used LSGS technique to mitigate NBTI induced delay. The technique selects the degraded gates and increase their transistor sizes to keep circuit delay below a threshold value of 15%. It ensures lifetime reliable operation at the cost of 12% area overhead.

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