Worst-Case Bit Line Coupling Backgrounds for Open Defects in SRAM Cells

Sandra Irobi Zaid Al-Ars
{i.s.irobi, z.al-ars}@tudelft.nl
Computer Engineering Laboratory
Faculty of Electrical Engineering, Mathematics, and Computer Science
Delft University of Technology
2628 CD Delft, Netherlands
Phone: +31 15 278 1832

I. Abstract

In this paper, we present an evaluation of the impact of bit line (BL) coupling on the faulty behavior of an SRAM cell in the presence of specific data in the neighborhood cells. In a nutshell, we tackle the following problem: given a defective SRAM cell with parasitic coupling effects, where the parasitic effect is capacitive, determine specifically the influential open defects, the impact of neighborhood coupling data on the faulty cell, all stressful coupling background data and thus, quantify the magnitude of the worst-case coupling background (WCB) against other stressful coupling background (CB) for each defect. Our results show that for a read 0 operation, CB 00 is the most stressful, while for a read 1 operation, the CB 11 is the most stressful. The exact amount of stress depends both on the location of the defect and the amount of BL coupling.

Keywords: Open defects, SRAM cells, bit line coupling, worst-case coupling background.

II. Introduction

Research on parasitic coupling effects in ICs is becoming indispensable due to the ever decreasing sizes of currently manufactured memory devices. As a result of the regular structure of memory devices, the optimization of the cell area is highly beneficial in the sense that the dimensions of transistors, and distances between wires can be adjusted to achieve miniaturization. Unfortunately, one of the disadvantages of this trend is high sensitivity to defects such as opens, both within and at the peripherals of the memory cell array.

Signals in memory devices are carried by lines wired across the memory area such as the BLs. A common attribute due to such connections is a high load and capacitance, as well as capacitive coupling with other signals, power, BL and ground lines.

BL capacitive coupling causes small coupling voltages on adjacent BLs, which influences proper sense amplifier operation. The resultant cross talk noise has long been considered as a limiting factor to designing high speed SRAM devices [2]. Capacitive coupling was identified as the cause of 67% field returns in 2002 in Intel microprocessors [9], which buttresses the increasing importance of this problem.

A number of solutions, such as BL twisting, have been proposed to reduce cross talk noise and increase the *signal-to-noise ratio* [4], [5]. However, such solutions focus mainly on overcoming BL coupling from a design perspective, in order to prevent data destruction during a write operation [6], or in order to reduce the BL delay time during the precharge cycle, thereby increasing overall memory performance [3]. Despite these efforts, no work has focused on determining all other stressful CBs nor in addition, quantified the magnitude of other stressful backgrounds against WCB.

Therefore, in this paper, we determine all influential open defect positions in the SRAM cell as well as the impact of coupling CB on the faulty cell. We present, in addition to WCB, other stressful coupling CBs for each open defect, and then quantify the magnitude of these stressful CBs against their corresponding WCB.

The rest of this paper is organized as follows. Section III discusses BL coupling, while Section IV presents an evaluation of open defect positions in an SRAM cell. In Section V, we describe the influence of neighborhood data. We present simulations results and analysis in Section VI. In Section VII we evaluate the worst-case deviation of each CB against WCB for each open defect. Section VIII gives the conclusions.

III. Explaining BL Coupling

An electrical Spice SRAM model, is presented in Figure 1, which is used in the evaluation of BL coupling effects

in this paper. The model transistor parameters are based on the 65nm BSIM4 model card as described by the Predictive Technology Model [10]. The memory has a 3x3 cell array to enable simulation of all neighboring coupling effects. These cells are connected to three BL pairs: left BL (BLl), which has the *left true (BTl)* and *left complementary (BCl)* BLs, *middle BL (BLm)*, which has the *middle true (BTm)* and *complementary (BCm)* BLs, and the *right BL (BLr)*, which has BTr and BCr BLs.

Each *word line (WL)* or cell array row in the model has 3 cells: left (l), middle (m) and right (r); while each BL or cell array column has 3 cells numbered as 0, 1 and 2. The cell in the center of the array (i.e., memory cell Mm1) is the faulty cell under analysis. Each BL is also connected to precharge devices to ensure proper initial BL voltages. Read/write access to different BLs is controlled by the column access devices, which ensure that only one BT gets connected to the *true data line (DT)* and only one BC gets connected to the *complementary data line (DC)* during each memory operation. The model also contains a *sense amplifier (SA)* to inspect the read output (data out), as well as a write driver to drive input data (data in).

The total BL capacitance (C_{t}) is divided into three components: internal coupling to complementary BL (C_{bi}), external coupling to a neighboring BL (C_{bx}) and an inherent BL capacitance to ground (C_{g}) composed of coupling to all other parts of the memory (cells, WLs, substrate, etc). This is expressed as:

$$C_{\mathrm{t}} = C_{\mathrm{bi}} + C_{\mathrm{bx}} + C_{\mathrm{g}} \tag{1}$$

The exact values of these capacitance depend on the layout of the memory and its manufacturing technology. In general, the value of C_{g} accounts for a large portion of C_{t}. In literature, reported $C_{\mathrm{g}}/C_{\mathrm{t}}$ ratios range from 40% to over 90% [6]. On the other hand, due to the symmetry of the layout implementation of the BLs, the values of C_{bi} and C_{bx} are rather close to each other, and therefore we consider them to be equal ($C_{\mathrm{bi}} = C_{\mathrm{bx}} = C_{\mathrm{b}}$) such that:

$$C_{\mathrm{t}} \approx 2C_{\mathrm{b}} + C_{\mathrm{g}} \tag{2}$$

and the capacitive ratio range is [6]:

$$1 \leq C_{\mathrm{g}}/C_{\mathrm{b}} \leq 20 \tag{3}$$

IV. Evaluation of open defect positions

In this section, we present all *open defect positions (ODs)* in an SRAM cell. Figure 2 depicts all 18 possible ODs, $\mathrm{R1_t}$, $\mathrm{R2_t}$,..., $\mathrm{R1_c}$, $\mathrm{R2_c}$,...in an SRAM cell. Open defects are usually caused by broken lines or particle contamination that results in increasing line resistivity at the open position. When within the cell, opens partially disconnect the nodes of the cell, thus limiting the ability of

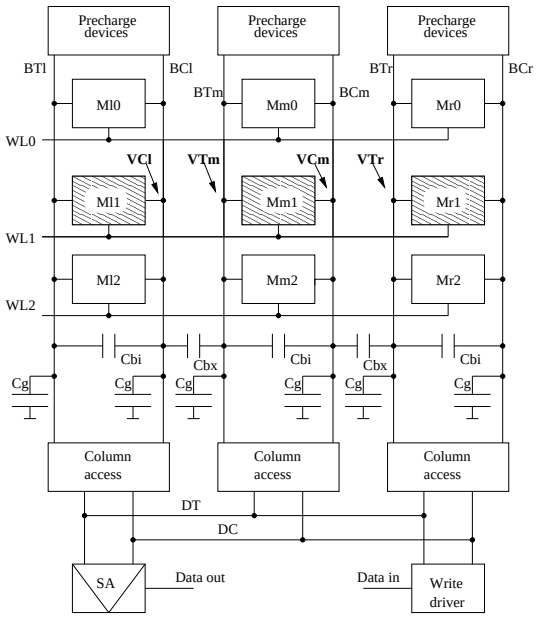

Fig. 1. SRAM electrical Spice model

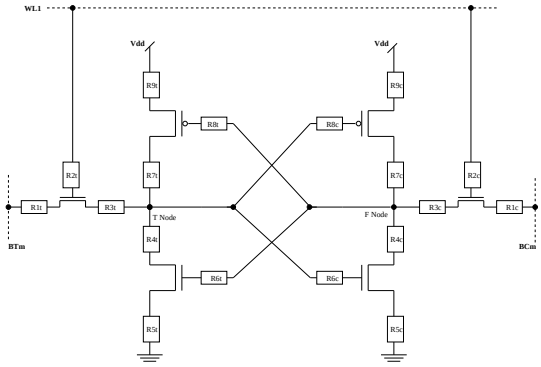

Fig. 2. Read 0 and read 1 in SRAM cells

the memory to control and observe the voltage within the cell. As shown in Figure 2, an open resistor R is injected on the defective signal line denoted in the figure as $\mathrm{R1_t}$, $\mathrm{R2_t}$,..., $\mathrm{R1_c}$, $\mathrm{R2_c}$,..., where *t* and *c* represent the T-Node and F-Node sides of the cell. R can vary from 0Ω to $\infty\Omega$. Table I lists and describes all ODs at the T-Node side, while Table II lists all ODs at the F-Node side of the cell with a description of the defect as well.

V. Influence of neighborhood data

As shown in our model in Figure 1, when a specific victim cell is accessed, the only neighboring cells also being accessed at the same time are those that belong to the same row as the victim, that is, those cells connected to the same WL as the victim cell. In our model, when the middle memory cell (Mm1) is accessed, the only other influential cells are the left memory cell (Ml1) and the

TABLE I. Description of open defects on the T-Node side

OD	Description
$R1_t$	Pass transistor connection to BL broken (drain)
$R2_t$	Pass transistor connection to WL broken (gate)
$R3_t$	Pass transistor connection to T-Node broken (source)
$R4_t$	NMOS down transistor connection to T-Node broken (drain)
$R5_t$	NMOS down transistor connection to ground broken (source)
$R6_t$	NMOS down transistor connection to F-Node broken (gate)
$R7_t$	PMOS up transistor connection to T-Node broken (drain)
$R8_t$	PMOS up transistor connection to F-Node broken (gate)
$R9_t$	PMOS up transistor connection to Vdd broken (source)

TABLE II. Description of open defects on the F-Node side

OD	Description
$R1_c$	Pass transistor connection to BL broken (drain)
$R2_c$	Pass transistor connection to WL broken (gate)
$R3_c$	Pass transistor connection to F-Node broken (source)
$R4_c$	NMOS down transistor connection to F-Node broken (drain)
$R5_c$	NMOS down transistor connection to ground broken (source)
$R6_c$	NMOS down transistor connection to T-Node broken (gate)
$R7_c$	PMOS up transistor connection to F-Node broken (drain)
$R8_c$	PMOS up transistor connection to T-Node broken (gate)
$R9_c$	PMOS up transistor connection to Vdd broken (source)

right memory cell (Mr1) connected to the same WL1 as Mm1.

During a read operation, the WL accesses the cell and connects it to the precharged BLs. Based on the value stored in the cell, a voltage differential develops on the BLs that the sense amplifier subsequently attempts to detect. The presence of BL coupling capacitance C_b, causes neighboring BLs to influence the voltage development during a read.

Now, we present a brief explanation of the impact of neighboring cells CBs, in this case Ml1 and Mr1 on the sensing of Mm1 when both Ml1 and Mr1 contain a logic 1. When WL1 is activated, cell Ml1 is accessed, which pulls BCl down by a voltage V_{Cl}. This, in turn, pulls the voltage on BTm down by V_{Tm}. Thus, this makes the detection of logic 1 in Mm1 more difficult while it makes the detection of logic 0 in Mm1 a lot easier. On the other hand, having a logic 1 in cell Mr1 does not modify the voltage on BTr, which in turn does not modify the voltage on BCm. In short,

- In order to stress logic 1 in Mm1, for example, $R1_t$, Ml1 must contain logic 1.
- Consequently, in order to stress logic 1 in Mm1 for the complementary defect, in this case, $R1_c$, Mr1 must contain logic 1 as well.

Simulated proofs of these statements will be shown in further analysis of our results. Furthermore, we consider the impact of CBs of Ml1 and Mr1 on the sensing of Mm1

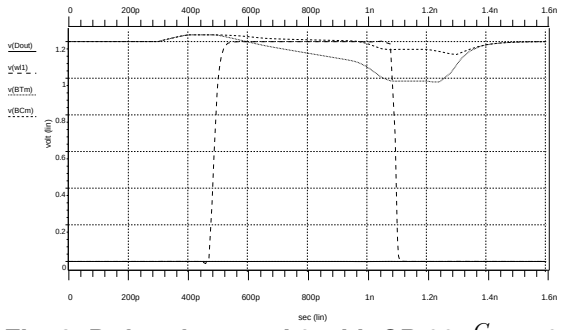

Fig. 3. Defect-free read 0 with CB 00, $\frac{C_g}{C_b}$ = 10.

when both Ml1 and Mr1 contain logic 0. When WL1 is activated, cell Mr1 is accessed, which pulls BTr down by a voltage V_{Tr}. This in turn pulls the voltage on BCm down by V_{Cm}, thereby making the detection of logic 0 in cell Mm1 more difficult, while making the detection of logic 1 in Mm1 easier. On the other hand, having logic 0 in cell Ml1 does not modify the voltage on BCl, which in turn does not modify the voltage on BTm. Simply put,

- In order to stress logic 0 in Mm1, Mr1 must contain logic 0.
- Consequently, in order to stress logic 0 in Mm1 for the complementary defect, in this case, $R1_c$, Ml1 must contain logic 0 as well.

Therefore, the most stressful CBs to detect parasitic BL coupling for an SRAM cell containing logic 1 is 11 in the neighboring cells connected to the same WL as the victim cell, while the most stressful CBs to detect logic 0 is 00 in the neighboring cells connected to the same WL as the victim cell.

VI. Simulation analysis of ODs

In our analysis we use an electrical Spice simulation model of the SRAM, consisting of a 3x3 cell array, sense amplifiers and a read/write circuitry. The model transistor parameters used for our simulations are based on the 65nm BSIM4 model card as described by the Predictive Technology Model [10].

For each OD evaluated, all scenarios are considered namely, read 0 and read 1 performed for each CB for all $\frac{C_g}{C_b}$ values. The value of C_g is considered to be a typical 500fF [7], while $\frac{C_g}{C_b}$ values are modified for each simulation in the range $1 \leq C_g/C_b \leq 20$ [1], with used C_b values as 500fF, 100fF, 50fF, 30fF and 25fF.

In general, both the value of R_{def} as well as the amount of the coupling capacitance influence the BL voltage differential and therefore decide the eventual output logic value at the sense amplifier. This creates a space of possible ($\frac{C_g}{C_b}$, R_{def}) values, where the defective cell can either function properly or fail. The specific resistive value in the R_{def} range, beyond which a fail occurs is the *critical resistance*

TABLE III. Simulation results of the 18 ODs

Defects (Read 0)	WCB	Stressful CBs			Defects (Read 1)	WCB	Stressful CBs		
		01	10	11			01	10	00
OD-R1$_t$	00	−	−	−	OD-R1$_c$	11	−	+	+
OD-R2$_t$	00	−	+	−	OD-R2$_c$	11	−	+	+
OD-R3$_t$	00	−	+	−	OD-R3$_c$	11	−	+	+
OD-R4$_t$	00	+	+	+	OD-R4$_c$	11	+	+	+
OD-R5$_t$	00	+	+	+	OD-R5$_c$	11	+	+	+
OD-R6$_t$	00	+	+	+	OD-R6$_c$	11	+	+	+
OD-R7$_t$	−	−	−	−	OD-R7$_c$	−	−	−	−
OD-R8$_t$	−	−	−	−	OD-R8$_c$	−	−	−	−
OD-R9$_t$	−	−	−	−	OD-R9$_c$	−	−	−	−

(R_{cr}). Our analysis is based on detecting the differences in behavior between a properly functional circuit and its behavior after an OD has been injected.

A. Analysis and results for OD-R1$_t$ and OD-R1$_c$

In this section, we analyze the simulated results for each read operation for OD-R1$_t$ and OD-R1$_c$ using all CBs.

Read at Mm1 with OD-R1$_t$. OD-R1$_t$ is injected between the access transistor and BTm, which limits the ability of the cell to discharge BTm, thereby reducing the voltage differential between BTm and BCm, and making the sense amplifier more prone to crosstalk errors.

Figure 3 shows the simulation result of a defect-free read 0 in cell Mm1, with $\frac{C_g}{C_b}$ = 10 and CB 00. Once WL1 is accessed, a differential voltage starts to develop between BTm and BCm, which is then detected by the sense amplifier and amplified as a full 0, thereby leaving the data out (Dout) line at 0.

Figure 4 shows the defective simulation results of a read 0 performed on Mm1, with R_{def} = 110KΩ and $\frac{C_g}{C_b}$ = 10 using CB 00. Comparing these with the defect-free simulation results in Figure 3, we identify a number of differences. First, the differential voltage developing on BLs is significantly reduced in the defective case between $t = 0.4$ ns and $t = 1.4$ ns, making it extremely difficult for the sense amplifier to identify the correct stored value in the cell. Adding to that, the BL coupling voltage from neighboring cells causes the sense amplifier to detect an incorrect logic 1 in the cell rather than a logic 0, as indicated by the Dout signal in the figure. For all simulated $\frac{C_g}{C_b}$, values of R$_{cr}$ for OD-R1$_t$ are plotted and is depicted as curve CB000t of Figure 6. In the plot, the $x-$axis denotes $\frac{C_g}{C_b}$, while the $y-$axis represents R_{def} values. Each curve in the figure divides the ($\frac{C_g}{C_b}$, R_{def}) plane into two regions. The region above the curve is the *fail* region while the region below is the *pass* region. Note that only CBs for which fails have been observed are included in the plot.

As curve CB000t in Figure 6 indicates, the fail region expands gradually as the amount of coupling capacitance increases (i.e., decreasing $\frac{C_g}{C_b}$ values). This emphasizes

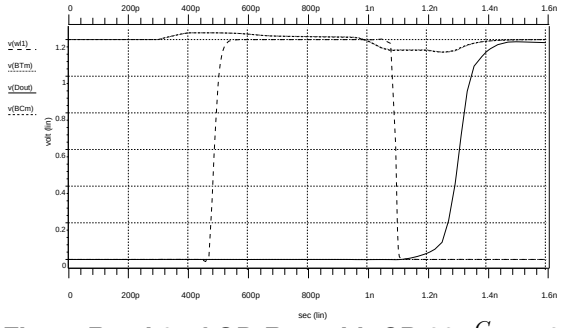

Fig. 4. Read 0 of OD-R1$_t$, with CB 00, $\frac{C_g}{C_b}$ = 10, R$_{def}$ = 110KΩ.

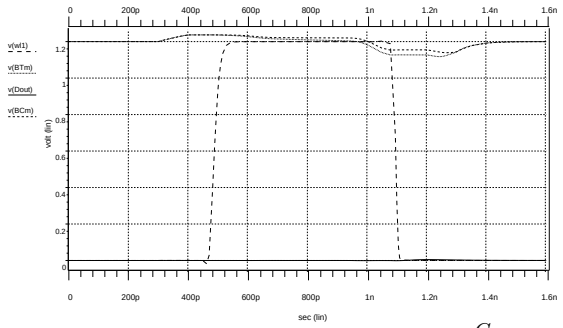

Fig. 5. Read 0 of OD-R1$_t$, with CB 11, $\frac{C_g}{C_b}$ = 10, R$_{def}$ = 110KΩ.

the importance of keeping the amount of BL coupling capacitance small relative to the total capacitance of BL. It also indicates that with continued technology scaling, the importance of testing for coupling effects will increase.

Result of a read 0 using CB 11 is as shown in Figure 5. Again, due to the defect in the memory cell, the differential voltage on BLs is very limited. However, as a result of the CB pattern in the neighboring cells and BL coupling effects, the differential voltage is biased towards detecting a logic 0 in the cell. This bias corrects the faulty behavior and prevents detecting a fail. In the same way, using other CBs (10 and 01) corrects the faulty behavior and prevents any fault from being detected.

A read 1 in the presence of OD-R1$_t$ will produce a correct logic 1 at the output irrespective of CBs used. The reason is that for a read operation, BL voltages are influenced by the cell node voltages. Since BLs are precharged to V$_{dd}$, only one BL is discharged during the operation, in this case BCm. Since BTm is not discharged, a read 1 operation will yield a correct logic 1 output.

Read at Mm1 with OD-R1$_c$. OD-R1$_c$ lies between BCm and the pass transistor at the F-Node side (symmetric counterpart of OD-R1$_t$) of the cell.

For a read 1 using CB 11, the differential voltage developing on BLs is significantly reduced in the defective case between $t = 0.4$ns and $t = 1.4$ns. An increase in

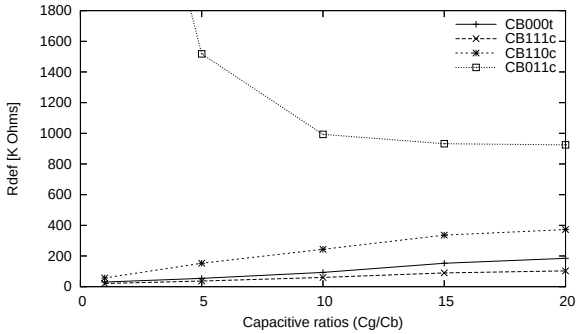

Fig. 6. Pass and fail regions for OD-R1$_t$ and OD-R1$_c$

coupling capacitance results in making the faulty behavior more dominant causing the sense amplifier to record an incorrect logic 0 instead of a logic 1. Plots of R_{cr} at varying $\frac{C_g}{C_b}$ for OD-R1$_c$ for CB 11 is shown in Figure 6 depicted by curve CB111c. Coupling due to both CBs 01 and 10 also yielded incorrect read outputs as depicted by curves CB011c and CB110c.

B. Analysis and results for other ODs

In this section, we present a behavioral summary for the rest of the open defects in the cell. The simulation results and analysis for OD-R2$_t$ ... OD-R9$_t$ (all on the T-Node side) are listed in the left-hand side of Table III, while those for OD-R2$_c$ ... OD-R9$_c$ (all on the F-Node side) are listed in the right-hand side of Table III. The first column of Table III lists the ODs, while the second column lists the corresponding worst case CB. The third column lists whether other CBs are also stressful (+) or not (−) for each given OD.

As listed in Table III, for OD-R4$_t$ and OD-R5$_t$ very low R_{cr} values were recorded. This underscores the high sensitivity to a resistive open on the pull-down transistor, which is on the current path for a read 0. This is also the case for OD-R4$_c$ and OD-R5$_c$ at the F-Node side of the cell while performing a read 1 where BCm is discharged. In the presence of OD-R7$_t$ ... OD-R9$_t$ the cell exhibits a fault-free behavior irrespective of the CB used. These 3 ODs represent broken connections on the source, gate and drain of the pull-up transistor. For a read 0 in SRAM, when WL1 is activated, current flows through the NMOS pass transistor on the BT side, through the pull-down NMOS transistor to ground. Since this necessary current path for a read 0 does not pass through the connections represented by OD-R7$_t$ ... OD-R9$_t$, the cell exhibits a fault-free behavior such that the sense amplifier gives a correct logic 1 output for all performed simulations. Here, a delay fault occurs, which takes place a while after the operation is performed. Special tests are used to detect these faults [8]. In the same way, OD-R7$_c$ ... OD-R9$_c$ on the F-Node side exhibit a complementary behavior for a read 1 operation.

VII. Worst-case deviation

In order to show how each CB performs against the simulated worst case value, we quantify the magnitude of deviation for all capacitive ratios for every OD considered in the SRAM cell. Let τ represent the worst case deviation ratio, such that:

$$\tau = \frac{Rcr_{\mathrm{CB}}}{Rcr_{\mathrm{WCB}}} \tag{4}$$

where Rcr_{WCB} is the value of R_{cr} for the worst case CB, and Rcr_{CB} is the R_{cr} of another stressful CB for the considered OD. The ratio, τ for a given defect indicates the magnitude to which WCB is more stressful compared to a given CB.

Table IV lists all ODs in the cell and their corresponding τ values. The left-hand side of Table IV lists the minimum to maximum τ values for all $\frac{C_g}{C_b}$ ratios (i.e, $1 \leq C_g/C_b \leq 20$) for each given ODs on the T-Node side of the cell. In the same way, the right-hand side of Table IV lists the minimum to maximum τ values for all $\frac{C_g}{C_b}$ ratios (i.e, $1 \leq C_g/C_b \leq 20$) for each given OD on the F-Node side of the cell. The first column on each side of Table IV lists OD positions, while the second column gives the corresponding worst case CB for the considered OD. The third column lists the minimum to maximum values of τ for each CB. $\tau = \infty$ indicates that R_{cr} for the considered CB (in all or for a given value of $\frac{C_g}{C_b}$) does not cause a fail. " − " indicates the absence of WCB, where no fail occurs and in which case the value of τ is not computed.

As shown in Table IV, for OD-R1$_t$, $\tau = \infty$ for all CBs, while for OD-R1$_c$ τ ranges from 8.9 to ∞ for CB 01, 2.63 to 4.02 times for CB 10 and ∞ for CB 00. It shows that for a read 1 (i.e., in the presence of OD-R1$_c$), WCB 11 is at least 8.9 times more stressful than CB 01 and 2.63 times more stressful than CB 10 and so on.

For OD-R2$_t$ and OD-R3$_t$, τ values for both CBs 01 and 11 for read 0 are ∞ signifying a fault-free behavior for these CBs, while in the presence of OD-R2$_t$, WCB 00 is at least 2.53 times more stressful than CB 10, and at least 12 times more stressful than CB 10 in the presence of OD-R3$_t$. It also lists that for a read 1 (i.e., in the presence of OD-R3$_c$), CB 11 is at least 3 to 5 times more stressful than CB 01 and 9 to 49 times more stressful than CB 10

For OD-R4$_t$, ..., OD-R6$_t$ and also for OD-R4$_c$, ..., OD-R6$_c$ the table shows very low τ values all in the range of 1 to 3.68, which emphasizes the equally low R_{cr} values recorded for these ODs beyond which a fail occurs. For example, for a read 0 in the presence of OD-R4$_t$, WCB 00 is between 1 and up to 1.08 times more stressful than CB 01. Likewise for a read 1, WCB 11 is between 1.125 times and up to 1.3 times more stressful than CB 01 and so on.

TABLE IV. min to max τ values for all ODs

Defects (Read 0)	WCB	min to max τ values for CBs			Defects (Read 1)	WCB	min to max τ values for CBs		
		01	10	11			01	10	00
OD-R1$_t$	00	∞	∞	∞	OD-R1$_c$	11	8.9 to ∞	2.63 to 4.02	∞
OD-R2$_t$	00	∞	2.53 to ∞	∞	OD-R2$_c$	11	1.49 to 1.79	1.87 to ∞	∞
OD-R3$_t$	00	∞	12 to ∞	∞	OD-R3$_c$	11	3 to 5	9 to 49	∞
OD-R4$_t$	00	1 to 1.08	1 to 1.01	1 to 1.01	OD-R4$_c$	11	1.125 to 1.3	1.125 to 1.5	1.25 to 2
OD-R5$_t$	00	1 to 1.02	1 to 1.05	1 to 1.03	OD-R5$_c$	11	1 to 1.3	1 to 1.04	1 to 1.01
OD-R6$_t$	00	1.1 to 1.8	1.08 to 1.4	1.2 to 2.5	OD-R6$_c$	11	1.12 to 1.58	1.16 to 2.25	1.3 to 3.68
OD-R7$_t$	–	–	–	–	OD-R7$_c$	–	–	–	–
OD-R8$_t$	–	–	–	–	OD-R8$_c$	–	–	–	–
OD-R9$_t$	–	–	–	–	OD-R9$_c$	–	–	–	–

TABLE V. τ values for read 0 & read 1 for OD-R6$_t$ & OD-R6$_c$

CBs	τ values for OD-R6$_t$					τ values for OD-R6$_c$				
	1	5	10	15	20	1	5	10	15	20
001	1.8	1.4	1.21	1.13	1.11	–	–	–	–	–
100	1.4	1.3	1.2	1.1	1.08	–	–	–	–	–
101	2.5	1.7	1.4	1.24	1.2	–	–	–	–	–
010	–	–	–	–	–	3.68	2.12	1.60	1.4	1.30
011	–	–	–	–	–	1.58	1.38	1.23	1.15	1.12
110	–	–	–	–	–	2.25	1.53	1.30	1.18	1.16

Listings for OD-R7$_t$, ..., OD-R9$_t$, and for OD-R7$_c$, ..., OD-R9$_c$ show that no τ values are computed since the read operations yielded correct outputs in the presence of these ODs.

As an example, Table V shows all τ values for OD-R6$_t$ and OD-R6$_c$ for each simulated capacitive ratios $\frac{C_g}{C_b}$. It lists the exact magnitude of τ for this OD, which was summarily provided in Table IV.

VIII. Conclusion

This paper discussed BL coupling and the way it impacts the faulty behavior of SRAM devices. The paper derived a model for BL coupling and estimated the amount of BL coupling voltage expected. The effects of coupling were analyzed analytically and using a Spice memory simulation model. The results show that the coupling mechanisms require the coupling backgrounds xxx in neighboring cells to ensure the worst case coupling conditions. It has been shown that in the presence of certain defects, some CBs are stressful, while others are not. Finally, this paper presented an evaluation of the magnitude of deviation (stressfulness), τ, of the coupling data background compared to the worst case CB for each open defect position. The analysis of simulation results shows that the exact amount of stress depends both on the location of the defect and the amount of BL coupling.

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