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According to these structural properties and characteristics, the membrane can be used for fuel cells systems manufacture, material for microcapacitors, membranes for electronic used solvents nanofiltration and purification.

4. CONCLUSIONS

A new method was presented for polysulfone-polypyrrole composite membranes synthesis consisting in phase inversion with chemical reaction. The membranes were synthesised from polysulfone/ pyrrole-N,N'-dimethylformamide/ methanol system by phase inversion followed by remaining pyrrole in membrane pores polymerization in the presence of iron chloride The polypyrrole from obtained membranes can be reversible activated with $FeCl_3$ during synthesis in order to increase the ionic conductivity and to improve the electrochemical characteristics for new synthesized material. At a thickness of 165 μm the measured capacitance was $C = 6.166$ nF/cm^2 and the ionic conductivity was $\sigma = 1.72 \cdot 10^{-4}$ S/cm^{-1}.

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SUSPENDED GATE FIELD EFFECT TRANSISTOR BASED POWER MANAGEMENT - A 32-BIT ADDER CASE STUDY

M. Enachescu, A. Van Genderen, and S. Cotofana

Delft University of Technology, Delft, The Netherlands
E-mail: {M.Enachescu, A.J.vanGenderen, S.D.Cotofana}@tudelft.nl

Abstract–*Recent investigations suggest that the Suspended Gate Field Effect Transistor (SG-FET) appears to have the potential to replace traditional high-Vt FETs, utilized as sleep transistors in power management circuits, due to its abrupt switching enabled by electromechanical instability at a certain threshold voltage and its ultra low "off" current (Ioff). This paper presents a preliminary assessment of the SG-FET potential if utilized as sleep transistor in circuits featuring cell based power gating. We first evaluate various SG-FET instances in terms of switching delay, current capability, and leakage. Subsequently, we compare these figures with the once offered by traditional switch transistors utilized in CMOS technologies. Finally, we evaluate the potential implications of the utilization of SG-FETs as sleep transistors in a 90nm CMOS 32-bit Adder. Our simulations indicate that Ioff is reducing by 10 orders of magnitude, while the active area of the sleep transistor is increasing with 130%.* ***Keywords:*** *SG-FET, sleep circuit.*

1. INTRODUCTION

According to International Technology Roadmap for Semiconductors (ITRS) [1], leakage in nanometer CMOS technologies can exceed active power consumption for VLSI circuits. The Suspended Gate Field Effect Transistor (SG-FET) appears to have the potential to replace traditional FETs in sleep mode circuits, due to: (1) its *abrupt switching* enabled by electromechanical instability at a certain threshold voltage that can lower the dynamic leakage and (2) its ultra low "off" current (I_{off}) that can lower the static leakage [9]. The purpose of this paper is twofold: (i) asses the SG-FET potential when utilized as sleep transistor in circuits featuring cell based power gating, and (ii) find out if SG-FETs constitute a viable alternative to high-V_t FETs in sleep mode circuits. In this line of reasoning we need to evaluate the SG-FET performance in terms of switching delay, current capability, and leakage and compare those with the ones offered by traditional switch transistors utilized in up to date CMOS technologies.

To achieve our goal we go through the following steps. We first focus on SG-FET background and its advantages. Subsequently, we perform a design space exploration in order to identify the most promising SG-FET geometries and to evaluate their potential performance. Finally, we compare the performance of an N-channel SG-FET with the one of an N-channel high-V_t FET in 90nm CMOS technology having the same active area. This paper is organized as follows: in Section 2 a brief introduction is provided on SG-FET including its basic operation and modeling. Section 3 describes the SG-FET design space exploration process. In Section 4 we evaluate the potential implications of the utilization of SG-FETs as sleep transistors in a 90nm CMOS 32-bit Adder [2] and finally concluding remarks are made in Section 5.

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2. SG-FET BACKGROUND

The SG-FET described in [3] and [4] is a rather complex device with a 3D geometry as presented in Fig. 1, where: (i) t_{ox} - the thickness of the gate oxide, (ii) h - the thickness of the suspended gate, (iii) W_{beam} - the width of the beam, (iv) L_{beam} - the length of the beam, (v) t_{gap0} - the gap between the oxide and the suspended gate, (vi) k_{beam} - the lumped linear spring constant of the beam. Fig. 2 presents the typical I_D-V_G characteristics of SG-FET. As V_G starts increasing, the beam starts moving down due to electrostatic attraction and I_D increases. During this phase, the gate-oxide capacitance is in series with the air-gap capacitance resulting in low electrostatic coupling of the gate to the channel and I_D is very small (Fig. 3). At a specific gate bias, the electrostatic force cannot be compensated by the mechanical restoring force anymore, and the beam collapses on the oxide. This is called **pull-in effect** (see Fig. 2). After pull-in, the I_D increase with V_G is similar to the one of a standard MOSFET. If V_G is decreased from some high value, then I_D starts decreasing. At a certain V_G value the system becomes unstable due to combined electro-mechanical

force and beam is pulled-out. This causes sudden I_D decrease due to large decrease in capacitance. This is called **pull-out effect** and it is depicted in Fig. 2.

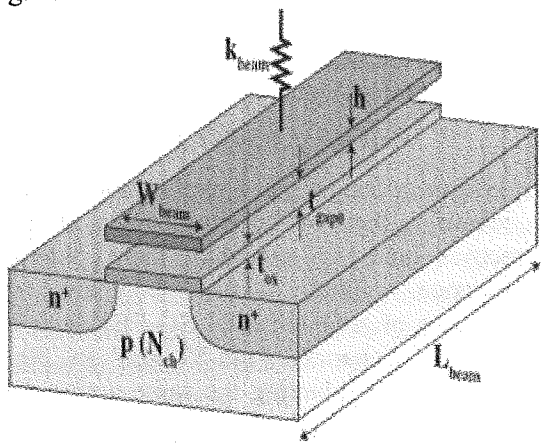

Fig. 1. Basic 3D SG-FET Geometry.

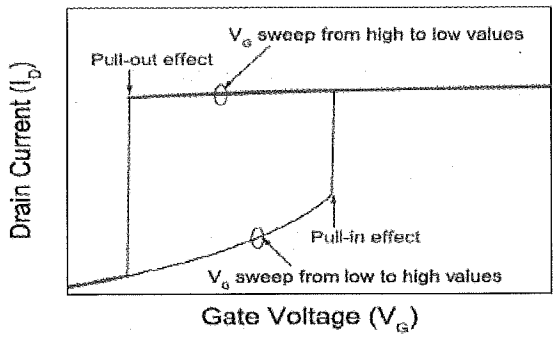

Fig. 2. ID-VG characteristic.

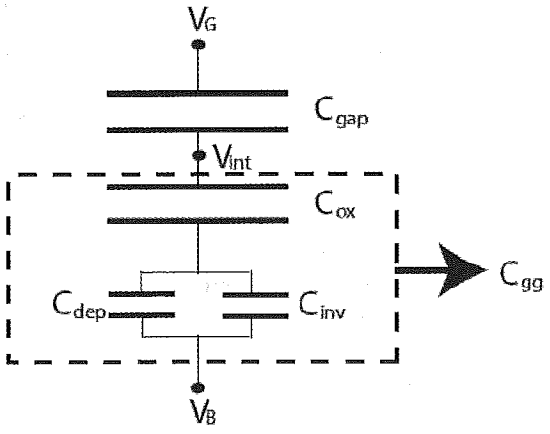

Fig. 3. SG-FET equivalent capacitive divider. Cgap, Cox, Cdep, Cinv, and Cgg represent gap, oxide, depletion, inversion, and gate-to-gate capacitances, respectively.

The SG-FET features a dynamic threshold voltage: *high* in the up-state and *low* in the down-state. This property is not always beneficial, especially in (micro)processors domain, where the supply voltage should be as low as possible.

3. SG-FET GEOMETRY ANALYSIS

To carry on a thorough analysis of the SG-FET potential capabilities as potential sleep transistor, we need to generate a large set of feasible SG-FET geometries and to evaluate them by means of simulations. To characterize the various SG-FET device instances we utilize the SG-FET Verilog-A model introduced in [5] in combination with Cadence software [6]. Given the complexity of the design space we have to restrict the dynamic range for the device parameters for the case of interest, i.e., (micro)processors. The supply voltage for processor applications in 90nm technology is 1.1 V, according to the 2007 ITRS roadmap [1]. This low supply voltage however, assuming the current lithography constraints (minimum W_{beam} = 350 nm, minimum t_{ox} = 3 nm, minimum t_{gap0} = 20 nm) is not sufficient for such an SG-FET device to properly function. In view of that, we focused the current investigation on finding SG-FET geometries with a pull-in voltage of 3 V, which can be of interest for applications with two supply voltages (3.3 V and 1.1 V). To find the device that is best suited for the considered application, we investigate a wide range of geometrical shapes as follows: (i) we vary h from 70nm to 100nm with a 10nm increment step, and (ii) we vary t_{gap0} from 10nm to 25nm, with a 5nm increment step. Other parameters that influence the performance of SG-FET are the gate work-function (WF) and the quality factor (Q). Every vibrating structure is subject to some energy loss, which translates in a reduction of vibration amplitude over time. The long settling times associated with those large Qs are however detrimental for rapidly switching devices such as the SG-FET [5]. We note here that in our preliminary study we only simulate one switching cycle (pulse), due to large amount of simulation data (many samples), thus the effect of the quality factor is not fully exposed. The gate work function (WF) mainly influences transistors characteristics by shifting them with respect to the applied gate bias [6]. In our experiments we assumed the following values: (i) WF of 4.4 eV, 4.6 eV, 4.8 eV, and 5 eV, and (ii) we varied Q from 10 to 100, with a step increment of 10.

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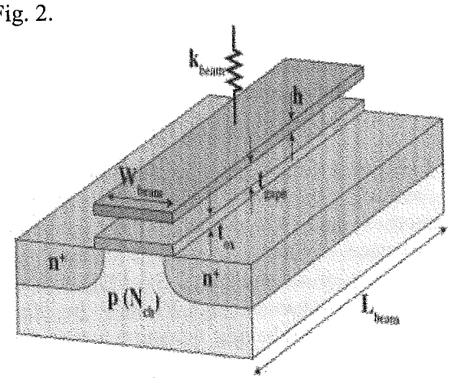

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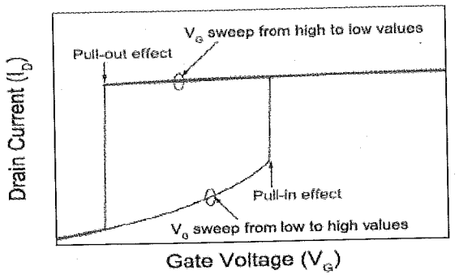

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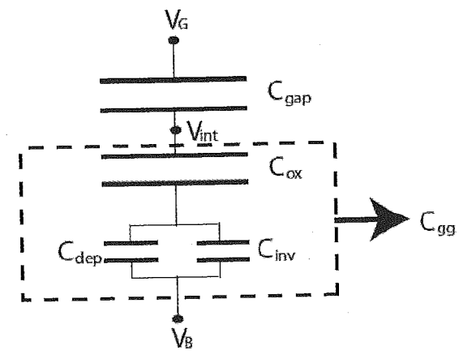

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The parameters of interest are determined as follows: (i) *Ion* is 90% of the maximum drain current produced as result of an input step signal, (ii) *Ioff* is the drain current after the pull-out event, and (iii) The switching delay is the time required for the device to reach 50% of its maximum drain current, when the gate voltage is larger than the pull-in voltage (V_{PI}). Examples of the *Ion*, *Ioff*, and switching delay we deduced via SPICE simulations are depicted in Fig. 4. The results of our simulations suggest the following: (i) *switching delay* ~ t_{gap0}, h, 1/LBEAM (area), WF, (ii) *Ion* ~ LBEAM, 1/WF, 1/h, 1/t_{gap0}, (iii) *Ioff* ~ LBEAM.

Table 1 presents three SG-FET configurations that we deduced from our extensive simulations results. The first set of parameters was selected as optimal for low *switching time* and high *Ion*, with respect to pull-in and pull-out effects, when WF=5 eV, tgap0 =20, 25 nm, and h=70, 80, 90, 100 nm. The second set of parameters was selected as optimal for low *switching time* and high *Ion*, with respect to pull-in and pull-out effects, when WF=4.4, 4.6, 4.8, 5 eV, selected as optimal for low *switching time* and high *Ion*, with respect to pull-in and pull-out effects, when WF=4.4, 4.6, 4.8, 5 eV, tgap0 =10, 15, 20, 25 nm, and h=70, 80, 90, 100 nm.

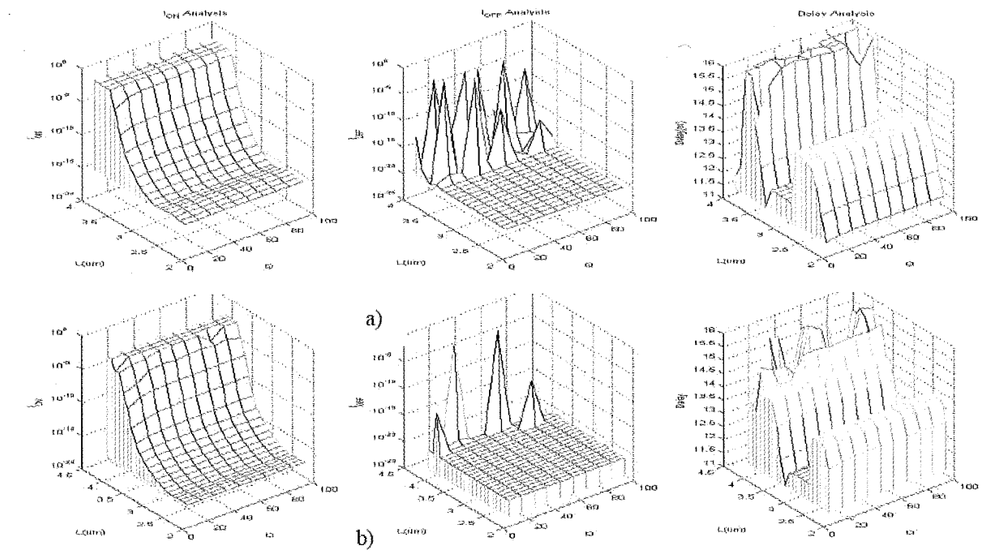

Fig. 4.

Table 1. Optimized SG-FET instances for low switching times and high Ion.

	h (nm)	$t_{gap}0$ (nm)	WF (eV)	L (µm)	W (nm)	Q	I_{on} (mA)	Ioff (Leakage floor) (fA)	Delay (ns)
I	100	20	5	4.2	350	100	2.2	5e-7(12)	8.67
II	100	20	4.4	4	350	100	3	2e-4(4.5e3)	7.41
II	100	10	5	4.5	350	100	1e-6	5e-7(5e-4)	3.03

4. 90nm CMOS 32bit ADDER ANALYSIS

To evaluate the potential implications of the utilization of SG-FETs as sleep transistors in a real application we consider a 32-bit adder equipped with a sleep mode circuit. The main purpose of this analysis is to demonstrate that SG-FET can be a better candidate for sleep transistor than FET for this kind of applications. Before doing that, we would like to mention that when properly designing a sleep transistor in a real digital circuit, one must take in consideration the followings parameters: (i) leakage current, (ii) ON current, (iii) area, and (iv) delay. Furthermore, the tolerance accepted for the

degradation of the gate performance is in the order of at most 5%.

We carry on our analysis over the 2.5 GHz CMOS 32-bit adder presented in [2]. For this circuit, in 90 nm technology, with high-V_t devices, T_{ox}=2.2nm, the sleep circuit (sleep transistor together whit the sleep circuit that triggers it) has the following characteristics: (i) the total leakage is 13 nA, (ii) the I_{ON} is 10 mA, (iii) the active area of the sleep transistor is 31.5μm^2, and (iv) the switching delay of the sleep circuit is 10us. If we want to replace the FET sleep transistor in this design with an SG-FET we have to be sure that this one can drive the same active current of 10 mA. To achieve this we need to use twenty-five SG-FET devices in parallel having the following parameters: W=350 nm, L=4.20 μm, h=90 nm, gap=20 nm, N_A=5×10^{17}, WF=5 eV, Q=100. These parameters were selected from Table 1 as being the best suited for this application. Such an SG-FET structure has the following characteristics: (i) I_{off} =50*0.4*10^{-21} =0.02 aA (sub-threshold drain current), (ii) I_{ON}=50*0.2*10^{-3}=10 mA, (iii) active area=73.5μm^2, and (iv) delay=10 ns. One can observe that this replacement is very much reducing (makes it negligible) the sleep transistor off current since I_{off} of SG-FET is much smaller (10 orders of magnitude) than I_{off} of "normal" FET. This suggests that the leakage savings due to the simple replacement of the FET with an SG-FET are very significant. Further research is required however in order to evaluate all the leakage components and to take full advantage of the SG-FET technology by designing special SG-FET tailored sleep circuits. The price that we have to pay for the sub-thresholds reduction is the increase of the active area of the sleep transistor by 130%, which can be quite significant in some circumstances.

It is hard to put into the right prospective the delay aspect. This is twofold: (i) The delay for the original design is covering the entire "go to sleep"/"weak up" process thus we do not have information about the actual delay of the FET sleep transistor, and (ii) In this evaluation we assumed that we just replace the FET sleep transistor with an SG-FET without changing anything in the rest of the sleep circuit. As suggested before this may not be the case in practice as this replacement may requires changes in the sleep circuit as well.

5. CONCLUSINS

SG-FET based sleep mode circuits are potentially interesting as they clearly enable substantial leakage reductions due to their extremely low OFF currents (10 orders of magnitude lower than FET). This holds true for the adder we considered and by implication for computing dominated applications. There is a clear area overhead associated with the utilization of SG-FET sleep transistors. We note here that our area estimates are not very accurate as they just include the active area of the SG-FET transistors and do not take into consideration extra area overhead that may result from potential changes in the rest of the sleep mode circuit and SG-FET specifics layout design rules. However, given that in nanotechnology context area is not the main issue any longer, as it was replaced by energy consumption and reliability, area overhead may not be perceived as a severe drawback.

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