Can SG-FET Replace FET In Sleep Mode Circuits?

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Abstract. The Suspended Gate Field Effect Transistor (SG-FET) appears to have the potential to replace traditional FETs in sleep mode circuits, due to its abrupt switching enabled by electromechanical instability at a certain threshold voltage and its ultra low "off" current (I_{off}). This paper presents a preliminary assessment of the SG-FET potential if utilized as sleep transistor in real applications, e.g., microprocessors. We first evaluate various SG-FET instances in terms of switching delay, current capability, and leakage. Subsequently, we compare these figures with the ones offered by traditional switch transistors utilized in CMOS technologies. Our simulation results indicate that SG-FET based sleep mode circuits are potentially interesting as they clearly enable substantial leakage reductions due to their extremely low "off" currents (4 orders of magnitude lower than FET) at the expense of a *4*x larger active area for the same capability to drive current.

Keywords: SG-FET, power gating, sleep transistor.

1 Introduction

The Suspended Gate Field Effect Transistor (SG-FET) appears to have the potential to replace traditional FETs in sleep mode circuits, due to its *abrupt switching* enabled by electromechanical instability at a certain threshold voltage and its ultra low "off" current (I_{off}).

The purpose of this paper is to asses the SG-FET potential if utilized as sleep transistor in real applications, e.g., micro (processors), and to find out if SG-FET constitutes a promising alternative to normal FET in sleep mode circuits. In this line of reasoning we need to evaluate the SG-FET performance in terms of switching delay, current capability, and leakage and compare those with the ones offered by traditional switch transistors utilized in up to date CMOS technologies. To achieve our goal we go through the following steps. We first perform a design space exploration in order to identify the most promising SG-FET geometries and to evaluate their potential performance. Subsequently, we compare the performance of an N-channel SG-FET with the one of an N-channel "normal" FET, having the same

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active area, in 90nm CMOS technology.

This paper is organized as follows: in Section 2 a brief introduction is provided on SG-FET including its basic operation and modeling. Section 3 describes the design space exploration for SG-FET model parameters. In Section 4 we compare nSG-FET with nFET by means of I_{on}, I_{off}, and switching *delay* and finally concluding remarks are made in Section 5.

2 SG-FET Background

The SG-FET described in [1] and [9] is a rather complex device with a 3D geometry as presented in Fig. 1, where: (i) t_{ox} - the thickness of the gate oxide, (ii) h - the thickness of the suspended gate, (iii) W_{beam} - the width of the beam, (iv) L_{beam} - the length of the beam, (v) t_{gap0} - the gap between the oxide and the suspended gate, (vi) k_{beam} - the lumped linear spring constant of the beam.

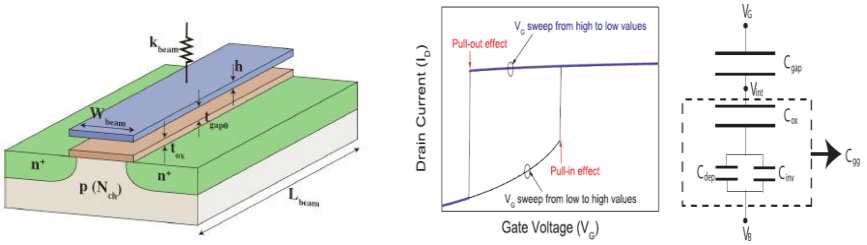

Fig. 1. SG-FET geometry, I_D-V_G characteristic, and the equivalent capacitance divider.

Fig. 1 presents the typical I_D-V_G characteristics of SG-FET. As V_G starts increasing, the beam starts moving down due to electrostatic attraction and I_D increases. During this phase, the gate-oxide capacitance is in series with the air-gap capacitance resulting in low electrostatic coupling of the gate to the channel and I_D is very small. At a specific gate bias, the electrostatic force cannot be compensated by the mechanical restoring force anymore, and the beam collapses on the oxide. This is called **pull-in effect** as depicted in Fig. 1. After pull-in, increase in I_D with V_G is similar to the standard MOSFET. If V_G is decreased from some high value, then I_D starts decreasing. At certain value of V_G, the system becomes unstable due to combined electro-mechanical force and beam is pulled-out. This causes sudden decrease in I_D due to large decrease in capacitance. This effect is called **pull-out effect** as indicated in Fig. 1. SG-MOSFET features a dynamic threshold voltage: *high* in the up-state and *low* in the down-state. This property is not always beneficial, especially in (micro)processors domain, where the supply voltage should be as low as possible.

3 Design Space Exploration

To carry on a thorough analysis of the SG-FET potential capabilities we need to generate a large set of feasible SG-FET geometries and to evaluate them by means of simulations. To characterize the various SG-FET device instances we utilize the SG-FET Verilog-A model introduced in [2] in combination with Cadence software [3].

Given the complexity of the design space we have to restrict the dynamic range for the device parameters for (micro)processors. The supply voltage for processor applications in 90nm technology is 1.1 V, according to the 2007 ITRS roadmap [4]. This low supply voltage, assuming the lithography constraints (minimum W_{beam} = 350 nm, minimum t_{ox} = 3 nm, minimum t_{gap0} = 20 nm) is not sufficient for such an SG-FET device to properly function. In view of that, we focused the current investigation on finding SG-FET geometries with a pull-in voltage of 3 V, which can be of interest for applications with two supply voltages (3.3 V and 1.1 V). To find the device that is best suited for the considered application, we investigate a wide range of geometrical shapes as follows: (i) we vary h from 70nm to 100nm with a step increment of 10nm, and (ii) we vary t_{gap0} from 10nm to 25nm, with a step increment of 5nm. Other parameters that influence the performance of SG-FET are the gate work-function (WF) and the quality factor (Q). Every vibrating structure is subject to some energy loss, which translates in a reduction of vibration amplitude over time. The long settling times associated with those large Qs are however detrimental for rapidly switching devices such as the SG-FET [5]. We note here that in our preliminary study we only simulate one switching cycle (pulse), due to large amount of simulation data (many samples), thus the effect of the quality factor is not fully exposed. The gate work function (WF) mainly influences transistors characteristics by shifting them with respect to the applied gate bias [6]. In our experiments we assumed the following values: (i) WF of 4.4 eV, 4.6 eV, 4.8 eV, and 5 eV, and (ii) we varied Q from 10 to 100, with a step increment of 10.

The parameters of interest are determined as follows: (i) I_{on} is 90% of the maximum drain current produced as result of an input step signal, (ii) I_{off} is the drain current after the pull-out event, and (iii) The switching delay is the time required for the device to reach 50% of its maximum drain current, when the gate voltage is larger than the pull-in voltage (V_{PI}). Examples of the I_{on}, I_{off}, and switching delay we deduced via SPICE simulations are depicted in Fig. 2 and Fig. 3.

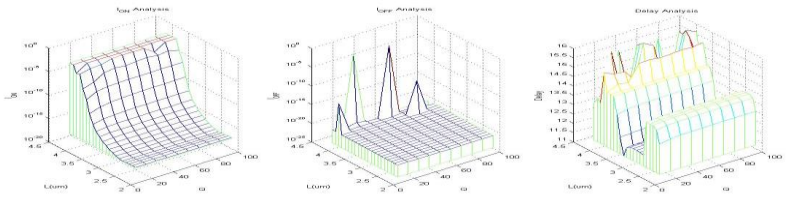

Fig. 2. I_{on}, I_{off}, Delay Analysis for WF = 5 eV, h = 100, t_{gap0} = 20nm.

The results of our simulations suggest the following: (i) *switching delay* ~ t_{gap0}, h, $1/L_{BEAM}$ (area), WF, (ii) I_{on} ~ L_{BEAM}, 1/WF, 1/h, $1/t_{gap0}$, (iii) I_{off} ~ L_{BEAM}. Moreover we observe that while there are clear relations between the various device parameters and the SG-FET performance there is no absolute "best in breed" geometry and various tradeoffs are possible.

Table 1 presents three SG-FET configurations that we deduced from our extensive simulations results. The first set of parameters was selected as optimal for low *switching time* and high I_{on}, with respect to pull-in and pull-out effects, when WF=5

eV, t_{gap0} =20, 25 nm, and h=70, 80, 90, 100 nm. The second set of parameters was selected as optimal for low *switching time* and high I_{on}, with respect to pull-in and pull-out effects, when WF=4.4, 4.6, 4.8, 5 eV, selected as optimal for low *switching*

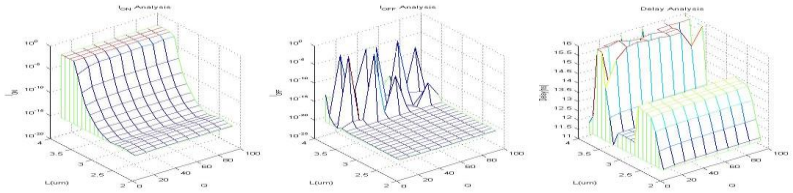

Fig. 3. I_{on}, I_{off}, Delay Analysis for WF = 4.4 eV, h = 100, t_{gap0} = 20nm.

time and high I_{on}, with respect to pull-in and pull-out effects, when WF=4.4, 4.6, 4.8, 5 eV, t_{gap0} =10, 15, 20, 25 nm, and h=70, 80, 90, 100 nm.

Table 1. Optimized SG-FET instances for low switching times and high I_{on}.

	h (nm)	t_{gap0} (nm)	WF (eV)	L (um)	W (nm)	Q	I_{on} *(mA)*	I_{off} *(Leakage floor)(fA)*	*Delay (ns)*
I	100	20	5	4.2	350	100	**2.2**	**5e-7(12)**	**8.67**
II	100	20	4.4	4	350	100	**3**	**2e-4(4.5e3)**	**7.41**
III	100	10	5	4.5	350	100	**1e-6**	**5e-7(5e-4)**	**3.03**

Table 1 indicates that the best compromise between high I_{on} and low *delay*, with respect to **pull-in** and **pull-out** effects, for t_{gap0}= 20, 25 nm and WF = 5 eV, can be reached for the set of SG-FET parameters (I).

4 SG-FET vs FET

In this section we compare the performance of an N-channel SG-FET with the one of an N-channel FET in 90nm CMOS technology, assuming the same active area.

To do that we utilize the best performance SG-FET instance still lithographically feasible having the parameters in Table 1 (I): W_{beam}=350 nm, L_{beam}= 4.2 um, h= 100 nm, t_{gap0}=20 nm, WF=5 eV, t_{ox}= 3 nm, N_A=5 x 10^{17} cm^{-3}.

For a fair comparison we assume as counterpart an N-FET with the width equal to L_{beam} of the SG-FET and the length equal to W_{beam}, in order to have the same active area for both transistors. The results of our simulations are presented in Table 2, which includes the key performance data for the "normal" nFET transistors and the nSG-FET devices for V_D=1.2 V and V_G=3V.

It is clear from Table 2 that the main SG-FET advantage is its extremely small I_{off}, and leakage floor, which are 10 and 4, orders of magnitude smaller, respectively, while I_{on} even though smaller it is comparable with the I_{on} of "normal" FET. The SG-FET however is about 100x slower then the normal FET and the active area is 4x larger for the same capability to drive current.

Table 2. Optimized SG-FET instances.

	I_{on}(mA/um)	I_{off} (pA/um)	Leakage Floor (pA/um)	Delay(ps)
nFET	0.8	13	200	20
nSG-FET	**0.52**	**$2.5*10^{-10}$**	**12e-3**	**8670**

To conclude, Table 2 suggests that SG-FET is a viable alternative to FET as sleep transistor due to its extremely low I_{off} and leakage floor. However, due to its relatively large *switching delay*, this device appears not to be suited for applications where the switching between active mode and sleep mode occurs too often. Fortunately, for processors, this is not the case in practice. For example, as indicated in [8], the wake-up time for a mobile application is about 2us.

5 Conclusions

In this paper we presented the results of the preliminary evaluation we carried on to estimate the SG-FET potential if utilized as sleep transistor in (micro)processors, to find out if SG-FET constitutes a promising alternative to normal FET. For this we evaluated various SG-FET geometries in terms of switching delay, current capability, and leakage and compared those with the ones offered by traditional switch transistors utilized in up to date CMOS technology. Our results indicate that SG-FETs can be potentially used as sleep transistors, due to their very low leakage floor and I_{off}, which are with 4 and 10 orders of magnitude smaller than the one of the normal FETs, respectively. However, for the current fabrication technology limitations, we could not obtain pull-in effects for gate voltages smaller than 3V and this implies some design overhead due to the utilization of an additional power supply. Moreover, due to lithographical requirements, the SG-FET requires a larger area when compared with a "normal" FET for the same capability to drive current.

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