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Emerging Non-CMOS Nanoelectronic Devices - What Are They?

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Abstract — **Complementary metal oxide semiconductor (CMOS) transistors have reached the nanometer geometry scale (1–100 nm) where they are difficult to be scaled anymore due to essentially quantum mechanical properties effects. This paper discusses emerging non-CMOS nanoelectronic devices (nanodevices) that could potentially be able to circumvent the CMOS scaling problem. First we propose a taxonomy, which classifies the nanodevices according to the physical phenomena driving their operations into electrical, magnetic, and mechanical nanodevices. Thereafter, a detailed analysis and comparison of the difference nanodevice classes are presented, including structures, advantages, disadvantages, and potential applications. Based on the comparison, we conclude that the electrical-dependent nanodevices are the leading nanodevices to be the complement or the replacement CMOS devices in future circuits.**

Keywords* — *CMOS, Nanodevices, CNTFETs, SETJs, spinFETs, moleculars.

I. INTRODUCTION

The ability of semiconductor industry to downscale complementary metal oxide semiconductor (CMOS) transistors has produced denser, cheaper, faster, smaller, and functionality richer electronic devices. Nevertheless, further scaling becomes more challenging with any new technological node as CMOS physical gate length has reached the nanometer geometry scale (1–100 nm). Nanoscale CMOS devices start to be influenced by quantum mechanical properties effects [1]. Furthermore, manufacturing difficulties in patterning small size transistor, rising cost in producing the chip and increasing in power density dissipation are some other problems faced by semiconductor industry [2], [3]. These are the reasons that CMOS devices are predicted to end their services at the end of next decade [1].

In order to solve these problems, researchers started to explore novel devices as a complement or even replacement to CMOS devices. Nanoelectronic devices (hereafter referred as *nanodevices*) offer opportunities for greater level of miniaturization, more economical fabrication costs, exceptional high density and high performance [1], [3].

The objective of this paper is to discuss various emerging non-CMOS nanodevices and their possibilities to replace CMOS devices as the core technology inside every integrated circuit chips in the future. The rest of this paper is organized as follows. Section II classifies the nanodevices based on the physical phenomena driving their operations, into three classes: electrical, magnetical, and mechanical nanodevices. Section III, Section IV and Section V analyzes the electrical, magnetic, and mechanical nanodevices, respectively. Section VI summarizes and compares the addressed nanodevices. Finally, Section VII concludes this paper.

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II. CLASSIFICATION OF NANODEVICES

Nanodevices can be classified, based on the phenomena driving their operation into three classes namely *electrical-dependent*, *magnetic-dependent*, and *mechanical-dependent*; they are defined next.

1) Electrical-dependent nanodevices

They are based either on *ballistic transport*, *tunneling* or, on *electrostatic* phenomenon. In the case of ballistic transport the electrons travel without resistivity in a medium (material) [4]. In the case of tunneling, the electrons can pass through a potential energy barrier at some level of energy as results of a quantum-mechanical process [5]. In the case of electrostatic, the interaction of electrons happens with the presence of electric field [6].

2) Magnetic-dependent nanodevices

Magnetostatic and *spin transport* are the driving phenomena for the operation of the devices in this class. In the case of magnetostatic, the magnetic dipole interactions are manipulated to carry the information [7]. In the case of spin transport, the spin polarized electrons movement can be maintained by the magnetic field [8].

3) Mechanical-dependent nanodevices

Restructuring of conductive polymers is the phenomenon for this category. The structure of the polymer moves or changes when activated by input sources [9].

Generally, these nanodevices have some advantages compared to CMOS transistors, for instance, higher mobility electrons, smaller size, and lower power consumption. On the other hand, there are some disadvantages, for example, low temperature requirement, immature fabrication techniques, and vulnerable to noise due to low power operation. In the following subsections, we explain the basic concept of operation, advantages, disadvantages, and review the current development for each of the nanodevices considered in this paper.

III. ELECTRICAL-DEPENDENT NANODEVICES

There are three rudiment categories of electrical-dependent nanodevices; ballistic transport-based nanodevices, tunneling-based nanodevices, and electrostatic-based nanodevices. These nanodevices have a common characteristic, which is the fact that their operations are determined by the movement of electrons inside each of them.

A. Ballistic transport-based nanodevices

As aforeentioned, ballistic transport is basically the smooth

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traverse of electrons in a medium without encounter a scattering event [4]. The resistivity originates from either, the scattering of impurity atoms, lattice vibration of atoms (which are called acoustic and optical phonons), crystal defects in the medium, or interfaces [10]. These scattering sources tend to slow down the velocity of the traverse electrons. In the ultra-small size medium, where the number of scattering is low ballistic transport is become dominant. Ballistic transport is ideally observed when the medium length is smaller than the mean free path of the scattering length [4], [10].

Two essential nanodevices that operate based on ballistic transport are carbon nanotube field-effect transistors (CNT-FETs) and nanowire transistors (NW-FETs). As an analogous to CMOS, CNT and NW used in the nanodevices act as channel in the bulk substrate.

1) *Carbon Nanotube Field-effect Transistors (CNT-FETs)*: Figure 1 shows a schematic structure of a CNTFET which is closely similar to MOSFETs in terms of construction and operation [10]. The only difference is that the channel is formed using CNT wire instead of the bulk substrate (the induced inversion layer).

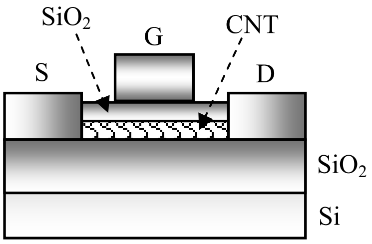

Figure 1. Schematic structure a CNTFET.

When compared with CMOS, CNTFETs have an extraordinary mechanical strength, low power consumption, better thermal stability, ballistic electron transit, capable to carry high current density, and higher resistance to electromigration [12]-[17]. However, the difficulty to control *chirality* formation to produce either semiconductor or metal and hardship in determining the placement and size of the tube are the drawbacks of these nanodevices [17].

Bachtold et al. [18] have demonstrated logic circuits built from CNTFETs such as an inverter, a logic NOR, an SRAM cell, and an ac-ring oscillator using these devices. A multistage complementary NOR, OR, NAND, and AND logic gates and ring oscillators have been fabricated based on arrays of p- and n-type CNTFETs by Javey et al. [10]. More recent work by Liu et al. [19] has utilized double-gate CNTFETs to build dynamically reconfigurable eight-function logic gate.

2) *Nanowire Field-effect Transistors (NW-FETs)*: A NW-FET has a similar structure to a CNT-FET but the channel is formed using semiconductor nanowire in place of carbon nanotubes [20]. More creative feature of a vertical wrap-gated field-effect transistor based on InAs nanowires has been demonstrated by Bryllert et al. [21].

The advantages of NW-FETs over CMOS are similar to CNT-FETs [22] plus the ability to operate at high speed, produces saturated current at low bias voltage [21] and the potential to behave as either active and passive devices (by synthesizing a single nanowire [17]). However, current fabrication techniques are still lacking the capability to control the size of a nanowire and accuracy to position it on the substrate [17].

Xiang et al. [23] have demonstrated top-gated Ge/Si NWFET heterostructures with high-k dielectrics. The NWFETs can perform three to four times greater than those for state-of-the-art MOSFETs. The ability of synthesizing NWs to be p- and n-type obviously leads to the realization of logic gates. Huang et al. [24] have fabricated AND and OR gates using p-doped Si and n-doped GaN. More recent work by Jalabert et al. [25] using NWs as transistor channel has resulted in non-volatile memory elements.

B. Tunneling-based nanodevices

The fundamental operation of tunneling-based nanodevices is owing to the penetration of electrons through a barrier. The number of electrons that can tunnel are proportional to the bias voltage, V, across the device. The higher the V, the larger number of electrons can tunnel through the barrier, thus higher current flow. Two basic tunneling-based nanodevices are resonant tunneling diodes (RTDs) and single electron tunneling junctions (SETJs). These nanodevices can be turned on and off by allowing electrons to tunnel and blocking them, respectively.

1) *Resonant Tunneling Diodes (RTDs)*: A RTD as shown in Figure 2 is two terminal devices in which the current flow is controlled by the voltage at the drain [26]. The source, S, and the drain, D, are separated from channel region known as island, I, by two barriers, B, with thickness less than 10 nm.

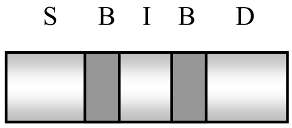

Figure 1. Schematic structure a RTD.

The island can be described as potential well [5]. This very small island obstructs the movement of electrons from moving in and out of it. Electrons are confined inside the island and their energy is "quantized" by quantum mechanics [5]. The narrower the island, the wider the energy level is. For electrons to tunnel from the source to the island, two quantum mechanic effects must be fulfilled. First, one of the quantized energy levels at the island should be equal or lower to the energy level at the source. Second, there must be an unoccupied energy level in the island. The effects are also applicable to the tunneling of electrons from island to the drain. The two effects strongly influence the flow of electrons through RTDs [5].

The benefits of using RTDs instead of CMOS in electronic circuits are related to faster operation, higher circuit density, and lower power consumption [5], [22]. The capability of RTDs to operate in negative differential resistance (NDR) state realizes multiple on and off states [5]. However, the drawbacks are non-zero current between peaks, which lowers the on and off ratio, hardness to have stable operation because tunneling current is very sensitive to bias voltages, and complexity in fabrication due to small size [1], [22].

RTDs that are incorporated with a third terminal acting as a gate to control the voltage form resonant tunneling transistors (RTTs) [27]. Pacha et al. have fabricated and tested dynamic NAND-NOR logic gates using two-input RTTs and two RTDs circuits [28]. In another project, a self latching inverter circuit has been fabricated and demonstrated at low frequencies using two vertical RTTs (VRTTs) [29]. The VRTTs are formed by RTDs and Schottky gate that control voltage bias. The fabrication of first-in first-out (FIFO) memories using molecular RTDs has been demonstrated by Rose et al. [30].

2) *Single Electron Tunneling Junctions (SETJs)*: Figure 3 illustrate a SETJ structure, which consists of two conductors set as source, S, and drain, D, separated by a thin insulator that act as barrier, B. At first glance, the operation of SETJs is quite similar to the RTDs where electrons can tunnel through the barrier when adequate voltage is biased at the source. Nevertheless, the fundamental operation of SETJs is based on a single electron tunneling a time. The movement of the electrons produces a measurable current flow.

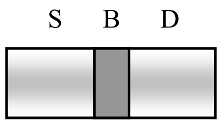

Figure 3. Schematic structure a SETJ.

In principle, for an electron to tunnel pass through the barrier in SETJ structure, its energy must equal the Coulomb energy [31]. If a single electron is tunneling through the barrier, it may prevent the addition of following electrons due to the electrostatic repulsion of the existed electron in the drain side [5]. The event of blocking the extra electron to tunnel is called *Coulomb blockade* [31].

The avail of SETJs compared to CMOS transistors are better scalability, faster operation and less power consumption [32]. At high temperature, nevertheless, electrons tend to tunnel because their thermal energy has surmounted the Coulomb blockade [5]. Susceptibility to noise is another disadvantage of SETJs [22].

Investigations on effective SETJs-based logic and arithmetic computation have been performed by Lageweg et al. on single electron encoded logic (SEEL) [33], [34] and by Cotofana et al. on electron counting [35]. By connecting SETJ to a capacitor, single electron box (SEB) is created. Klunder and Hoekstra have demonstrated programmable logic using these SEB-based circuits [36]. SETJs also can be made into three-terminal nanodevices, which realize single electron transistors (SETs). K. Degawa et al. have proposed basic SET-based logic gates useful for designing multi-value logic and mixed-mode logic circuits for applications such as logic-in-memory circuits and signal processor [37].

C. Electrostatic-based nanodevices

Electrostatic-based nanodevices operate by forcing electrons to interact with each other in the presence of electric field. Such forces are described by Coulomb's law [38]. Essentially when similar particles (if both are either electrons or protons) are closely located, they tend to repel each other. On the other hand, the opposite particles attract each other. Nanodevices that fall into this category are electrical quantum-dot cellular automata (EQCA).

Basically, electrical quantum-dot cellular automata (EQCA) use the configuration (position) of individual electron inside quantum-dot cell to represent the logic value [39], [40]. Instead of traversing the electron from input to output like in electrical wire, the configuration of electrons is propagated from the input towards the output by means of electrostatic force.

EQCA employ arrays of coupled quantum dots to implement Boolean logic functions. A basic EQCA cell consists of four quantum dots situated at the corner of the cell. The cell contains two extra mobile electrons which are forced to move between the four dots by external electric field at the input side. Note that the electrons only move between the dots within the cell but not out from the cell. When there is no external electric field applied, the electrons are forced to the opposite-diagonally corner due to the electrostatic interaction between each pair of electron called Coulombic repulsion [39], [40].

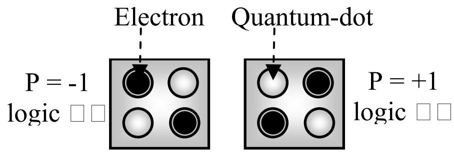

Figure 4. EQCA polarization of logic '1' and '0'.

The two possible configuration states represent logic '0' and logic '1' is shown in Figure 4. In standard practice, cell configuration P = −1 represents logic '0' and P = +1 substitutes logic '1'. The combination of EQCA cells enables the realizations of relatively complex logic function. For example, if two cells are brought close together, Coulombic interactions between the electrons cause the cells to take on the same configuration.

EQCA nanodevices exhibit greatness in low power dissipation, non-volatility and reconfigurability [6], [41]. Nonetheless, their slow operation, sensitivity to background charges, very low temperature operating requirement, and synchronization complexity must be overcome before these devices can be utilized for more complex digital designs [6]. Additionally, the circuits built of EQCA require feedback prevention circuitry because the circuits can be operated in both directions [41].

By joining EQCA in series, information can be propagated through the cells which make up an electrical wire [39], [40]. Majority logic gate, which realizes logic function of either AND or OR gate depending on the one of the inputs to be permanently logic '1' or logic '0' also has been proposed in [39], [40]. Another basic logic gate can be built using EQCA is inverter [39], [42]. More complex logic circuits such as 1-bit full-adder [43] and 12-bit data bus arithmetic logic unit (ALU) [44] also have been proposed.

IV. Magnetic-dependent Nanodevices

Magnetic-dependent nanodevices employ magnetization to operate. Although these variant of devices have been adopted in electronics circuits some years ago, it was until the discovery of giant magnetoresistance (GMR) in 1988 that realized spintronic technology [45]. There are two categories of this class; magnetostatic nanodevices and spin-based nanodevices.

A. Magnetostatic-based nanodevices

Magnetostatic-based nanodevices utilize the position of quantized magnetic dipole (direction) and magnetostatic force to hold logic value and propagate from input to output respectively [7], [46]. The nanodevices for this class are magnetic quantum-dot cellular automata (MQCA).

The principle operation of magnetic quantum-dot cellular automata (MQCA) is similar to EQCA where the representation of logic value is propagated by means of force in lieu of electrons traversing in a electrical wire. However, the phenomenon that drive the propagation is based on the magnetostatic in MQCA whereas in EQCA is electrostatic. An MQCA cell consists of two extra flux quanta (quantized magnetic dipole) which determine the logic. As EQCA, the MQCA are arranged in array-structure to perform Boolean function. An external magnetic field is required to set the logic value to the first cell. The induced magnetic flux moves in opposite dipole (antiferromagnetically) towards adjacent cell when the external magnetic field is shut off. Figure 5 shows the configuration of logic value representation of MQCA.

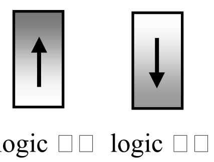

Figure 5. MQCA polarization of logic '1' and '0'.

The advantages of MQCA are high integration density, less power, non-volatile, defect tolerant, fabrication simplicity, and able to operate at room temperature [46], [47], [48]. However, no further details area made on disadvantages. MQCA have been applied to have similar application as EQCA such as wire, inverter, and majority gate. Imre et al. [48] have demonstrated majority gate that behave as programmable two-input NAND or NOR gate. Another majority gate invented by Lent et al. [39] produces AND or NOR gate. A. Imre et al. [48] also suggested that MQCA can be integrated into magnetic random access memory (MRAM) to have "intelligent memory".

B. Spin-based nanodevices

Spin-based nanodevices utilize the spin polarized state (orientation) of electrons to operate. This spin phenomenon is the influence of magnetic-based material called ferromagnetism and magnetic field. Individual spin polarized state helps drain current modulation [8], [49] which is able to perform switching operation. Spin field-effect transistors (spinFETs) are spin-based nanodevices.

As cited earlier, spinFETs depend on spin-polarized electron to behave like a normal MOSFET [8], [50]. SpinFETs operation is based on three effects; (i) the electrons injected into active region of the transistor must show high degree of spin polarization, (ii) the control signal to control the spin polarization, and (iii) the spin polarization must sustain the traveling time and distance in the active region [41]. The schematic structure of spinFETs is shown in Figure 6. The source and drain are made of ferromagnetic material or half-metallic-ferromagnet. The channel may be either semiconductor bulk induces with magnetic dopant to produce dilute magnetic semiconductor (DMS) or other materials such as GaMnN that possessed ferromagnetism [8].

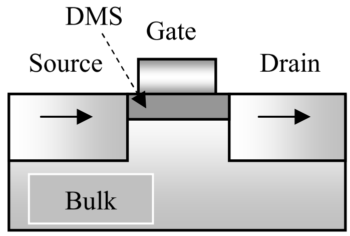

Figure 6. Schematic structure a spinFET.

A spin-polarized current can flow as in normal MOSFET only if both fixed magnetic direction in source and drain are aligned. Electrons are injected with definite spin orientation from source in which their orientation is controlled by gate voltage when transmitting in the channel. The gate-controlled voltage induces an effective magnetic field effect known as Rashba pin-orbit interaction [51]. This effect is able to control the relative spin state of electrons at drain end of the channel. If the electrons orientation is anti-aligned with the fixed magnetic direction in drain, then the spinFET will be turned on, otherwise is shut off [50].

SpinFETs have the advantages of high power gain, small off-current, low power consumption, tunable, high operating speed, nonvolatile, and better noise margin [1], [8], [50], [52]. Unfortunately, difficulty in injecting magnetic ions into semiconductor is the current technology limitation [8], [53].

S.G. Tan et al. [52] have proposed spinFETs with four ferromagnetic gate stripes on the heterostructure. The structure can be tunable (configured) to have different logic functions by varying the gate stripes using desired magnetization.

V. Mechanical-dependent Nanodevices

Mechanical-dependent nanodevices restructure their physical structure to perform an operation. The mechanical force is used to rotate or slide the component that from the nanodevices.

Restructuring-dependent nanodevices transport the electrons by restructuring their physical form. A sufficient external stimulus such as voltage, light, or magnetic is needed to initiate the process. The nanodevices belong to this class are molecular switches.

Molecular switches consist of organic molecules that locked together and can act as switches by moving on their components to have on and off configuration [17]. The most common molecular switches use a group of molecules called rotaxanes and catenanes as shown in Figure 7 [53]. Catenanes are composed of two rings locked together. Conversely, rotaxanes posses a ring trapped in a "dumbbell"-like rod. The position of the rings can represent logic '1' and '0' and it can be switched between those states using applied voltages. Such devices could show electron tunneling [54] or one-way flow of current (rectification) through the molecule [55].

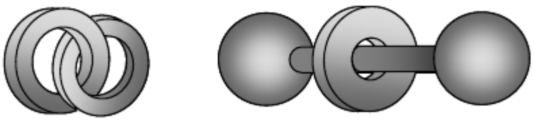

Figure 7. Schematic structure a spinFET.

The advantage of these extremely small-size devices are they can be self assembled, reconfigurable, molecules can be stable, and are perceived to have tremendous potential in building electronic devices [5], [58]. However, numerous technology challenges need to be solved such as interconnection to electrodes, effects of chemical absorption and high temperature operation [5], [22].

The molecular switches have been utilized to form hybrid CMOS/molecular memories [56], [57]. The hybrid nanoarchitecture called CMOL proposed by Likharev et al. can be configured to have logic functions and neuromorphic networks [58].

VI. Comparison

Table I summarizes the considered nanodevices in term of their advantages, disadvantages, and applications. In general, all nanodevices are superior in size (e.g. small) compared to CMOS devices. In particular, electrical-dependent nanodevices exhibit fast operation, consume low power, and scalable. Magnetical-dependent nanodevices are non-volatile and reconfigurable. Mechanical-dependent nanodevices can be self assembled, stable and reconfigurable.

TABLE I. Summary of Nanodevice.

Class	Electrical	Magnetical	Mechanical
Advantages	Small, fast, low power, scalable	Small, non-volatile, reconfigu-rable	Small, reconfigura-ble, self-assembly,
Disadvanta-ges	Susceptible to noise, fabrication complexity		
Application	Reconfigur able logic gates, full adder, ALU, non-volatile memory	Reconfigu-rable logic gates, MRAM component	Hybrid memory and FPGA

Due to small size, however, all nanodevices pose fabrication complexity. Moreover, they are susceptible to noise because operate at low voltage.

Basically, all nanodevices have been utilized to build logic gates and memory. Specifically, electrical-dependent nanodevices have been used to form more complex logic circuits such as full adder, arithmetic logic unit, and non-volatile memory. Magnetical-dependent nanodevices have been employed in magnetic random access memory. Mechanical-dependent nanodevices have been applied in hybrid memory and FPGA.

VI. Conclusion

In this paper, we have discussed different emerging non-CMOS nanodevices that are potentially to succeed CMOS in the next ten years. The nanodevices are classified into three distinct classes based on the physical phenomena behind their operation. A detail overview of the operation, the advantages, the disadvantages, and the applications of each device has been discussed. At this particular time, there is no crystal clear indication which device(s) will be the leading candidate as the CMOS complement or replacement. The reason is that the research of these emerging nanodevices is still in its nonage stage since involves new materials, immature fabrication techniques, and infancy applications. Nonetheless, we believe that the electrical-dependent nanodevices have some edge compared to the other nanodevices to be the complement to CMOS or the core technology underlying most of the future electronic circuit.

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