FPGA Implementation of Low-Frequency GPR signal algorithm using Frequency Stepped Chirp Signals in the time domain

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Abstract: *This paper concerns the FPGA implementation of a time-domain stepped frequency method, which is suitable for Ground Penetrating Radar implementation. It describes the block of the algorithm from implementation point of view. The conclusion gives information about the real-time constraints, and the device utilization for the particular reconfigurable processor.*

1. Introduction and problem formulation.

The contemporary reconfigurable hardware reveals great opportunities for rapid prototyping for various signal-processing systems. It provides flexibility of implementation and easy adjustment of the chosen algorithm. These unique features of the contemporary reconfigurable technologies make them promising candidates for mapping GPR signal-processing algorithms on real-time hardware systems, such as the one considered in this paper [1]. On the other hand, the reconfigurable hardware is not "magic". It also has some limitations. The most serious of them are: limited number of logical cells, maximum working frequency, maximum execution time of the algorithm etc.

In [1], a Stepped-Frequency Processing in Low-frequency GPR was considered. In the design of GPR algorithms, the authors used the stepped-frequency approach, intended for SAR applications. This approach makes it possible to obtain good-range resolution images, with a traditional narrow-band transmitter-receiver digital system. The method employs transmission of a burst of narrowband LFM pulses with frequency bands separated by a fixed step. More specifically [1], the purpose of investigation was to test what maximal frequency bandwidth of a wideband signal could be reconstructed using a traditional narrowband transmit-receiver digital system composed of commercial devices for signal processing. The authors presented new modifications of the two stepped-frequency algorithms, in the time and in the frequency domain, for implementation in GPR. With this aim in mind, they used the Monte Carlo simulation method for parameter optimization of the stepped-frequency processing, taking into consideration the limitation parameters of SP AD6624 and AD6624A devices. Comparison analysis of these synthetic range profiles showed that the two stepped-frequency

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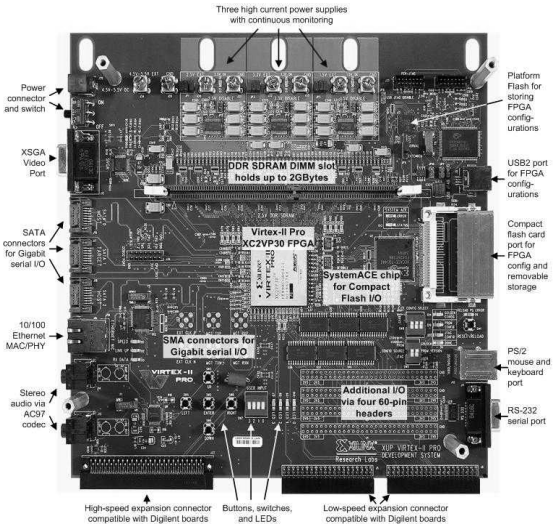

Figure 1. Xilinx XUP Virtex™-II Pro Development System [7]

processing methods were of equivalent quality. However, it could be seen that the time-domain method was more appropriate because it produced the synthetic range profile with lower noise [1].

This paper describes an implementation of this time-domain method on hardware reconfigurable platform, based on VIRTEX II Pro technology [5], XUPV2P (fig.1). A block diagram of the algorithm suitable for a reconfigurable hardware implementation is presented. All computational kernels from the algorithm are designed as separate hardware blocks, and verified individually and stacked together. The frequency stepped chirp GPR algorithm operating at range from 4.6 MHz to 38.2 MHz, with sampling frequency at baseband – f_S=2.5 MHz, generating a synthetic range profile with a resolution of 1-2 m by transmitting 14 narrowband chirps is implemented through VHDL and IP Cores [6].

2. Describing of the implementation.

A block diagram of the receiver was made considering the described stepped frequency algorithm in the time domain [1]. It consists of: down converter; interpolator; phase correction; frequency shifter; buffer for constructing the whole signal; correlator; envelope detection, normalization and image storing. The block diagram of the receiver is shown in figure 2. The number of transmitted pulses is M=14. The sampling frequency of the signal is 80Mhz, the sampling frequency of the video signal – 2,25Mhz, minimal frequency carrier f_{min}=4,6Mhz, maximal frequency carrier f_{max}=38,2Mhz, the step in frequency is d_f=2,4Mhz. The frequency sweep rate is $b=\Delta f/T_p$. T_p is the time duration of a narrow-band chirp, in our case - 1,6*ms*. The down converter is implemented according to the specifications of the Digital Down Converter (DDC) V1.0 (Xilinx IP) [6]. It encompasses the following processing: Quadrature Amplitude Demodulation, Low Pass Filter and decimation by 32. The input signal consists of 5376 samples. The tests were performed considering following parameters: System

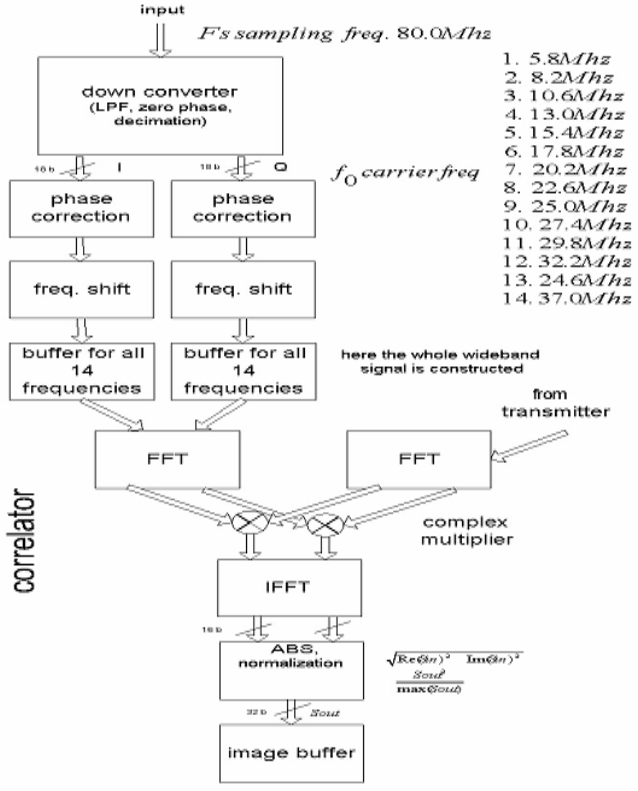

Figure 2. Block diagram of the implementated receiving structure

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frequency rate: 100MHz; Input signal frequency: 80MHz; Input data width: 16 bits; Output data width: B8=18 bits; Spurious dynamic range of the digital synthesizer: 40dB; Frequency resolution: 0.5MHz; Phase angle: fixed; Output mixer width: 20 bits, Cascaded Integrator/Comb (CIC) and Compensation filters are not included; The finite impulse response (FIR) filter is included in the synthesis of the digital down converter, the decimation rate is 16; the FIR filter length is 16 and the result precision is 12;

The time domain reconstruction follows. It consists of phase correction and frequency shifting. In order to avoid the phase discontinuities in the wideband signal the phase of each narrow band pulse should be corrected by phase-correction quotient [1]:

$$\Phi_m = \exp\left\{j\pi b T_p^2 [m + (1-M)/2]^2\right\}$$

The frequency shifting is performed by [1]:

$$v''_{bb}(t,m) = v_{bb}(t,m)\exp(j2\pi \delta f_m t),$$
$$\delta f_m = [m + (1-M)/2]\Delta f$$

$m=1..M$, $v_{bb}(t,m)$ is the signal after the quadrature demodulation. Next a buffer for signal reconstruction (coherent summing) follows. It consists of standard storage buffer based on memory block core [6]. Considering the signal processing principles the correlator consists of multiplication between received and transmitted signal in the frequency domain. Therefore we put two 64-point FFT transforms, each for the received signal and for the transmitted signal. Next an IFFT is needed to come back in the time domain (fig.2). $r(t) = \left|FFT^{-1} S(f) V(f)\right|$, $S(f) = FFT[s(t)]$, $V(f) = FFT\left[v'(t-\sigma)\right]$, where $s(t) = conj\left[v'(t-\sigma)\right]W(t)$ under $\sigma = 0$ and $W(t)$ is the weighting function [1]. Envelope detector and signal normalization follows (fig.2). The envelope detector consists of two multipliers and a sqrt block, which is based on CORDIC v.3.0 architecture [6]. Figure 3 shows the implementation of the transceiver. It consists of look-up table, which contains the signals for transmitting. According to the algorithm [1]. The number of the signals is 14 and each of them consists of 128 samples. The transmitted signal is formed by Tukey window before sending it to Digital to Analogue Converter.

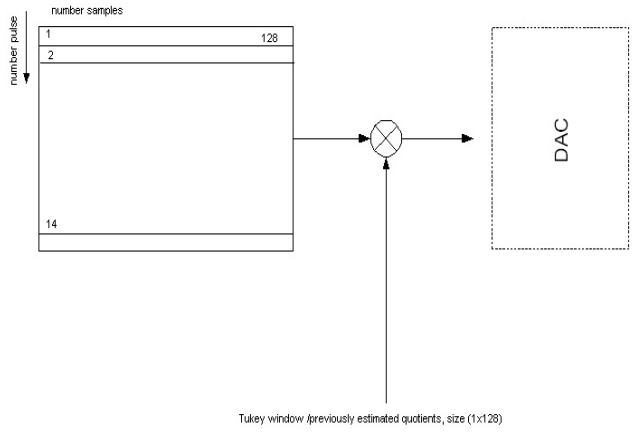

Figure 3. Block diagram of the implementated transmitting structure

3. Simulation results

The simulation results are obtained via Modelsim simulator [8]. A VHDL code was written, and studied trough Modelsim simulator. After the performed simulation, the constraints for real time imaging were defined. The correlation is performed for 108 μs. The total synthesis estimation parameters are: number of slices = 8937; BRAM = 30; Mult18x18 = 62. After the simulation performing the real time constraints were approximately found 400 μs. According to the synthesis report, the usage of the processor was almost 75%.

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3. Conclusion

Based on the reported synthesis result of the Modelsim simulator, we can conclude that the processor VIRTEX II Pro is suitable for such signal-processing task. The algorithm will be performed for about 400 μs, which gives the real time constraint.

4. Acknowledgments

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