Evaluation of SRAM Faulty Behavior Under Bit Line Coupling

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Abstract: *The faulty behavior of memory devices has traditionally been evaluated in isolation of the parasitic effects present on chip. As these effects become more dominant, however, they start to negatively influence the fault coverage of commonly used memory tests. This paper studies the way bit line coupling affects the faulty behavior of SRAM devices. Spice simulations are used to show how coupling can prevent the detection of otherwise detectable faults. Furthermore, an evaluation is done of the needed bit line coupling conditions to guarantee a high fault coverage of a given defect. This is done by identifying the most stressful data background patterns in the neighborhood of the faulty cell.*

Keywords: *SRAMs, bit line coupling, faulty behavior, data backgrounds, Spice simulation.*

1 Introduction

The large variety of rather complex faulty behavior exhibited by memory devices, along with the huge amount of different internal states a memory can assume, makes the task of testing memory devices exceptionally challenging. Therefore, researchers have traditionally limited their analysis of memory faults to simplified cases by assuming that memory faults can be tested for and detected in isolation, without taking into consideration other manufacturing deviations such as parasitic effects and process variations. This approach, however, is gradually loosing its validity, as the dimensions of manufactured memory structures continue to decrease, thereby increasing the dominance of parasitic effects on the faulty behavior.

Some research is already starting to address the need to evaluate the impact of parasitics on memory faulty behavior. The concept of fault primitives, for example, started by introducing a framework of dynamic (time-related) DRAM faults that require multiple operations (rather than one) to be detected [Al-Ars03], which has subsequently been proven for SRAMs as well [Borri03]. Time-related faulty behavior has since been analyzed for defects in peripheral memory circuits [vdGoor04] as well as address decoders [Hamdioui06]. However, there is no publication to identify the way parasitic *bit line (BL)* coupling influences the faulty behavior of SRAMs.

This paper evaluates the way SRAM faults are affected by the presence of parasitic capacitance between BLs. Using an electrical Spice simulation model, the paper shows how coupling can reduce the fault coverage of memory test. The paper also identifies the conditions needed to insure the proper detection of memory faults while taking BL coupling into consideration.

The paper is organized as follows. Section 2 discusses the effects of BL coupling capacitance on the functionality of SRAM devices. Section 3 analyzes the impact of capacitive coupling on the faulty behavior of the memory. Section 4 shows a Spice simulation model to be used to evaluate coupling effects, while Section 5 presents the simulation-based fault analysis results. Section 6 ends with the conclusions.

2 Quantifying BL coupling

Figure 1 gives a model for BL coupling in SRAMs. The shown memory consists of three BL pairs: left BL (BLl) which has the left true (BTl) and complement BL (BCl), center BL (BLc) which has the center true (BTc) and complement (BCc), and the right BL (BLr) which has BTr and BCr. A word line (WL) controls three memory cells (M) each connected to one of the BL pairs. Each BL pair also has a precharge circuitry.

The total BL capacitance (C_t) is divided into three components: internal coupling to the complementary BL (C_{ci}), external coupling to a neighboring BL (C_{cx}), and an inherent BL capacitance (C_b) composed of coupling to all other parts of the memory (cells, WLs, substrate, etc.).

$$C_t = C_{ci} + C_{cx} + C_b \quad (1)$$

The exact values of these capacitances depend on the layout of the memory and on its manufacturing technology. In general, the value of C_b accounts for a large portion of

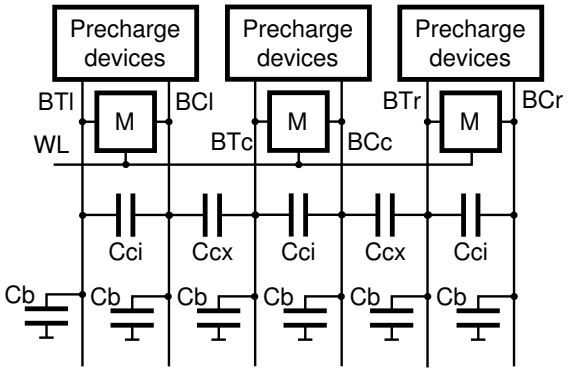

Figure 1. Model of BL coupling in SRAMs.

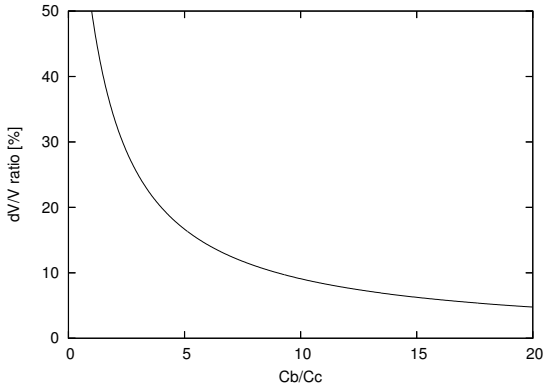

Figure 2. Plot of Equation 4 for $\Delta V/V$.

C_t. In the literature, reported C_b/C_t ratios range from 40% to over 90% [Takeda00, Ding03]. On the other hand, due to the symmetry of the layout implementation of the BLs, the values of C_{ci} and C_{cx} are rather close to each other, and therefore we consider them to be equal ($C_{ci} = C_{cx} = C_c$).

$$C_t \approx 2C_c + C_b \tag{2}$$

$$\frac{4}{3} \leq C_b/C_c \leq 18 \tag{3}$$

During a read operation, the WL accesses the cell and connects it to the precharged BLs. Based on the value stored in the cell, a voltage differential develops on the BLs that the sense amplifier subsequently attempts to detect. The presence of C_c causes neighboring BLs to influence the voltage development during a read. If we assume that a defective BL is totally floating, while the neighboring BL develops a voltage V, then the amount of coupling voltage (ΔV) induced on the floating BL can be expressed as:

$$\frac{\Delta V}{V} \approx \frac{1}{(C_b/C_c)+1} \tag{4}$$

Figure 2 plots the amount of relative coupling voltage $\Delta V/V$ in Equation 4. The figure shows that in the range of possible C_b/C_c according to Equation 3 (between 18 and 1.3), $\Delta V/V$ ranges between 5% up to a value of 43%.

3 Effects of coupling

BL coupling and the resulting cross talk noise has long been considered as a limiting factor to designing high speed, low power SRAM devices [Nambu92]. A number of solutions, such as BL twisting, have been proposed to reduce cross talk noise and increase the *signal-noise ratio (SNR)* [Ohhata92, Noda01]. These solutions, however, focus mainly on overcoming BL coupling from a design point of view, in order to prevent data destruction during a write operation [Takeda00], or in order to reduce the BL delay time during the precharge cycle, thereby increasing overall memory performance [Nambu95]. This section evaluates the impact of coupling on the faulty behavior of the SRAM.

BL coupling results in developing small coupling voltages on adjacent BLs, which influences proper sense amplifier operation. From a testing point of view, it is important to understand how a specific initialization of a neighborhood of cells affects the sensing of a given victim, so that the worst case values can be written in the neighboring cells.

When a given victim cell is accessed, the only neighboring cells also being accessed at the same time are those that belong to the same row as the victim (i.e., those connected to the same WL as the victim). In the case shown in Figure 3, when the center memory cell (Mc—the grayed out cell in the figure) is accessed the only other influential cells are the left memory cell (Ml) and the right memory cell (Mr).

Figure 3 gives a graphical representation of the impact of Ml and Mr on the sensing of Mc, when Ml and Mr both contain logic 1. When WL is activated, cell Ml is accessed which pulls BCl down by a voltage V_l. This, in turn, pulls the voltage on BTc down by V_{tc}. This makes the detection of logic 1 in cell Mc more difficult while it makes the detection of logic 0 in cell Mc easier. On the other hand, having logic 1 in cell Mr does not modify the voltage on BTr, which in turn does not modify the voltage on BCc. In short,

- In order to stress logic 1 in Mc, Ml must contain logic 1 as well.
- In order to stress logic 0 in Mc, Ml must *not* contain

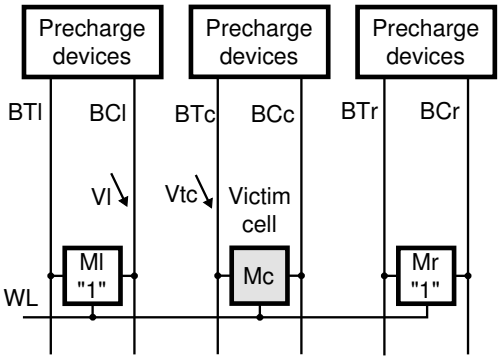

Figure 3. Effects of neighboring cells on victim when Ml=1 and Mr=1.

logic 1, thereby requiring a stored logic 0 instead.

Figure 4 gives a graphical representation of the impact of Ml and Mr on the sensing of Mc, when Ml and Mr both contain logic 0. When WL is activated, cell Mr is accessed which pulls BTr down by a voltage V_r. This, in turn, pulls the voltage on BCc down by V_{cc}. This makes the detection of logic 0 in cell Mc more difficult while it makes the detection of logic 1 in cell Mc easier. On the other hand, having logic 0 in cell Ml does not modify the voltage on BCl, which in turn does not modify the voltage on BTc. In short,

- In order to stress logic 0 in Mc, Mr must contain logic 0 as well.
- In order to stress logic 1 in Mc, Mr must *not* contain logic 0, thereby requiring a stored logic 1 instead.

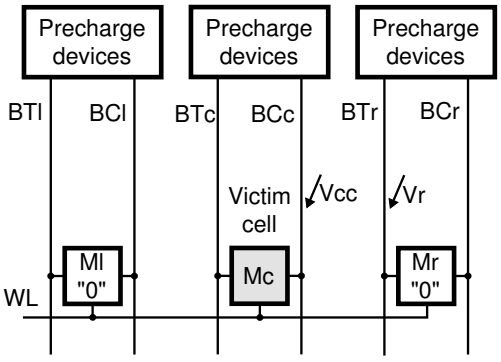

Figure 4. Effects of neighboring cells on victim when Ml=0 and Mr=0.

In conclusion, the most stressful background to detect parasitic BL coupling for an SRAM cell containing logic 1 is 11 in the neighboring cells connected to the same WL. In contrast, the most stressful background to logic 0 is 00 in the neighboring cells connected to the same WL.

4 SRAM simulation model

Figure 5 shows an SRAM Spice simulation model to be used in the evaluation of BL coupling effects on the faulty behavior. The model transistor parameters are based on the 65nm BSIM4 model card as described by the Predictive Technology Model [Zhao06, PTM]. The memory has a 3×3 cell array to enable simulation of all neighboring coupling effects. Each WL (or cell array row) is connected to 3 cells: left (l), center (c) and right (r); while each BL (or cell array column) is connected to 3 cells numbered as 0, 1 and 2. The grayed out cell in the center of the array (i.e., cell Mc1) is the defective cell under analysis.

Each BL is also connected to precharge circuits to ensure proper initial BL voltages. Read/write access to different BLs is controlled by the column access devices, which ensure that only one BT gets connected to the *true data line (DT)* and only one BC gets connected to the *complement data line (DC)* during each operation. Finally, the model contains a *sense amplifier (SA)* to inspect the read output (Data out), as well as a write driver to drive input data (Data in).

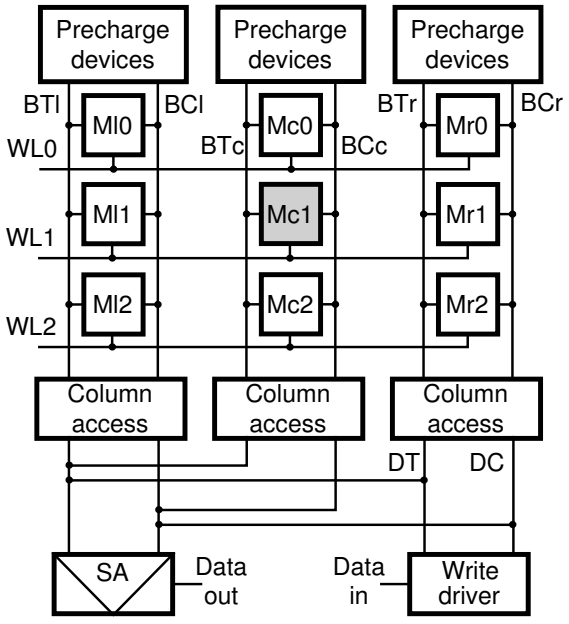

Figure 5. SRAM Spice model for evaluation of BL coupling.

The model also contains internal and external BL coupling capacitances (C_{ci} and C_{cx} as shown in Figure 1), as well as BL caps to ground (C_b). The values of C_{ci} and C_{cx} are considered equal to C_c. The value of C_b is considered to be a typical 500fF, while the ratio C_b/C_c will be modified in the simulation between 1.3 and 18 [Ding03].

Figure 6 shows a simulation of a read operation of logic

0 in cell Mc1, with $C_b/C_c = 10$. Once WL1 is accessed, a differential voltage starts to develop between BTc and BCc, which is then detected by the sense amplifier and amplified as a full 0 on DT. As a result, the data out line (Dout) stays at 0 as well.

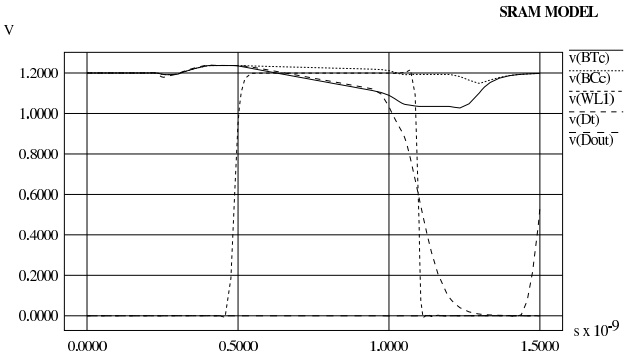

Figure 6. Read operation of logic 0 in cell Mc1.

5 Fault analysis results

Figure 7 shows the defective Mc1 memory cell to be simulated. The memory cell is a typical cross-coupled six transistor SRAM cell with two complementary nodes, true (T) and false (F). WL1 controls access of T to BTc and F to BCc through the two access transistors. An open defect resistance (R) has been injected into the cell between the access transistor and the T node to simulate the impact of BL coupling on the faulty behavior. This defect is very suitable for this analysis since it limits the ability of the cell to discharge BTc, thereby reducing the voltage differential and making the sense amplifier more prone to crosstalk errors.

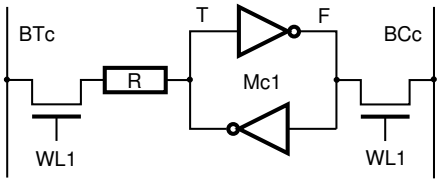

Figure 7. Defective Mc1 cell with open R.

Figure 8 shows the simulation results of a read 0 operation performed on Mc1, with $R = 1\text{M}\Omega$ and $C_b/C_c = 10$. The *data background (DB)* used for neighboring cells is 00 stored in both Ml1 and Mr1. As discussed in Section 3 this is supposed to be the worst case background for a read operation under BL coupling. Comparing the results with the fault free simulation in Figure 6 identifies a number of differences. First of all, the differential voltage developing on BLs is significantly reduced in the defective case, making it extremely difficult for the sense amplifier to identify the correct stored value in the cell. Adding to that the BL coupling voltage from neighboring cells causes the sense amplifier to detect an incorrect logic 1 in the cell rather than a logic 0, as indicated by the rising edge of the Dout signal in the simulation.

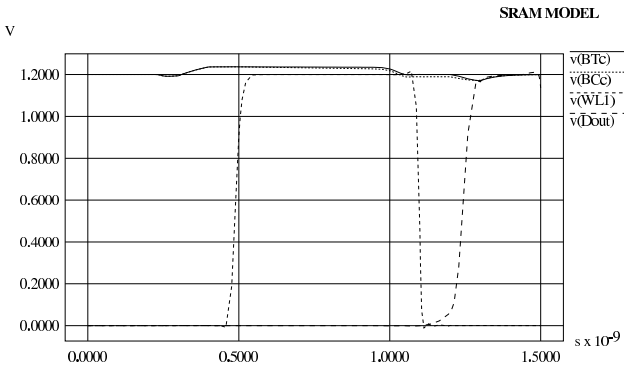

Figure 8. Read 0 on Mc1 with $R = 1\text{M}\Omega$ & DB 00.

Figure 9 shows the simulation results of a read operation performed on Mc1 using the same defective cell ($R = 1\text{M}\Omega$ and $C_b/C_c = 10$), but this time with the best case DB of 11 in cells Ml1 and Mr1. The figure again shows that as a result of the defect in the memory cell, the differential voltage developing on the BLs is very limited. However, as a result of the DB pattern in neighboring cells and BL coupling effects, the differential voltage is biased towards detecting a logic 0 in the cell, as indicated by the voltage on the Dout signal.

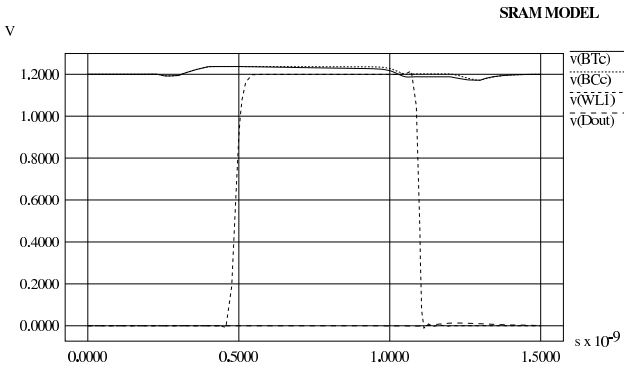

Figure 9. Read 0 on Mc1 with $R = 1\text{M}\Omega$ & DB 11.

In general, both the value of the defects resistance R as well as the mount of the coupling capacitance influence the BL voltage differential and decide the eventual output value. This creates a space of possible $(\frac{C_b}{C_c}, R)$ values where the defective cell can either function properly

or fail, as shown in Figure 10. The x-axis represents the $\frac{C_b}{C_c}$ ratio, while the y-axis represents the value of the defect resistance R. Each curve in the figure divides the space into two regions. The region below the curve is the *pass* region, while the region above the curve is the *fail* region with $(\frac{C_b}{C_c}, R)$ values that result in causing the sense amplifier to produce an incorrect read.

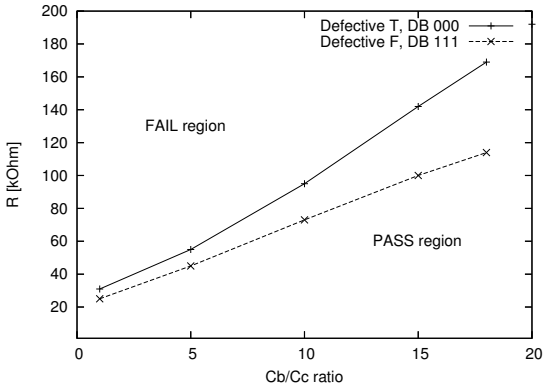

Figure 10. Pass/fail regions in the $(\frac{C_b}{C_c}, R)$ space.

The "Defective T" curve identifies the pass/fail regions for a cell with a defect between the T node and the access transistor (as shown in Figure 7), where Mc1 contains logic 0 and both neighboring cells Ml1 and Mr1 also contain a 0. As the curve indicates that as the amount of coupling capacitance increases (i.e., decreasing $\frac{C_b}{C_c}$ values), the fail region expands gradually. This result is inline with the earlier analysis in Section 2, where the amount of BL coupling voltage is found to increase with an increasing C_c. This indicates the importance of keeping the amount of BL coupling capacitance small relative to the total capacitance of the BL. It also indicates that with the continued technology scaling, the importance of testing for coupling effects will increase.

The "Defective F" curve identifies the pass/fail regions for a cell with a defect between the F node and the access transistor (the symmetrical counterpart to the defect shown in Figure 7), where all three cells Ml1, Mc1 and Mr1 contain 1. Again, an increase in coupling capacitance results in making the faulty behavior more dominant. Despite the symmetry in the SRAM cell structure, the pass region associated with the defective F node is smaller than that for T. This is probably caused by the inherent difference in speed between the NMOS and PMOS transistors.

It is interesting to note that simulations for both defects on the T and F nodes with any other DB other than the solid one did not result in any fail at all. This means that the solid background is a *necessary* condition for the detection of the defects. This confirms the conclusions drawn in Section 3.

6 Conclusions

In this paper, we discussed the influence of BL coupling on the faulty behavior of SRAMs. The paper presented a model of BL coupling and estimated the amount of BL coupling voltage expected. The effects of coupling were analyzed analytically and then using a Spice memory simulation model. The results show that the coupling mechanisms require specific data backgrounds to ensure the worst case coupling conditions, something that is important to take into consideration when designing SRAM tests. It has been shown that a solid data background is the most stressful, inducing the largest amount of coupling voltage that opposes detecting the proper read value by the sense amplifier. It has also been shown that the increasing coupling capacitance results in an accelerated increase of coupling noise, which means that with continued scaling the test consequence of coupling will become ever more significant.

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