Emerging Crossbar-based Hybrid Nanoarchitectures for Future Computing Systems

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***Abstract*—This tutorial paper discusses and analyzes differents hybrid nanoarchitectures that are structured using crossbar arrays. Such nanoarchitectures are likely to be used for building future computing systems. The hybrid CMOS/nanodevice architectures leverage the advantage of CMOS maturity and potentials in nanodevice (e.g. high density, low power consumption, reduced manufacturing costs, new functionality, etc.), to aid their mission in increasing the performance better than current CMOS-based architectures. We first describe the concept of crossbar-based nanoarchitecture and then classify the nanoarchitectures into two distinct structures; two-dimensional structures and three-dimensional structures. Subsequently, a detail analysis of each structure is presented including e.g., advantages in terms of area and performance over CMOS-based circuits. Finally, the most promising crossbar-based hybrid nanoarchitecture is suggested.**

I. Introduction

Over the last 50 years, Moore's law has been conformed in fabricating electronic instruments including computer systems. The prediction made in 1965 by Intel co-founder, Gordon E. Moore, stated that the number of transistors can be inexpensively fabricated placed on an *integrated circuit (IC)* is doubling approximately every 18 months [1]. At present, computer systems are mainly based on the complementary metal-oxide semiconductor (CMOS). Nevertheless, a consensus benchmark set by semiconductor manufacturers and researchers known as *International Technology Roadmap for Semiconductor (ITRS)* has predicted that *Complementary Metal Oxide Semiconductor (CMOS)* cannot be scaled beyond 22nm in year 2018 [2]. It is due to several challenges face by CMOS such as technology, economics, physical, and power thermal [3], [4], [5], [6].

New devices called nanoelectronic devices (nanodevices) has been aggressively developed with the purpose to complement and replace CMOS in near-term and long-term respectively. These nanodevices offer the potential to perform better than CMOS (e.g. denser integration, low power consumption, non-volatile, etc.) apart of reducing technology difficulty (e.g. manufacturing process) and economic (e.g. production and off-line testing costs) [7], [8], [9]. Realistically, to fabricate electronic circuits (inclusive of computer systems) entirely using nanodevices is not feasible at the moment due to technology constraints. Thus, the near-term idea is combining CMOS and nanodevices so that the advantages of both electronic devices can be leveraged (i.e. CMOS maturity and high density, low power consumption, reduced manufacturing costs, new functionality, etc. potentials for nanodevices). Several research groups have initiated building computation architecture circuits based on this *hybrid* CMOS and nanodevices [10], [11], [12], [13], [14]. Common to these nanoarchitectures is the structure is formed based crossbar arrays realized using nanodevices.

This paper analyzes different emerging hybrid nanoarchitectures based on crossbar arrays that have been proposed for future computing systems. Essentially, these nanoarchitectures have regular crossbar structure that can be patterned using nanoimprint and self assembly nanofabrication techniques [15]. The high degree of homogeneity offers a direct implication for defect-tolerant [16].

The rest of this paper is organized as follows. Section II presents the concept of crossbar-based nanoarchitecture. Section III classifies the nanoarchitectures into two different structures; two-dimensional and three-dimensional structure. Section IV and Section V discuss a detail analysis on each of these two-dimensional and three-dimensional structure nanoarchitectures, respectively. Section VI compares the proposed nanoarchitectures. Finally, Section VII concludes this paper.

II. The Concept of Crossbar-based Nanoarchitectures

The paper by G. Snider et al. [15] explains the definition of the basic structure in crossbar-based nanoarchitecture built from nanowires as depicted in in Fig. 1. The *crossbar* itself is the two perpendicular wires aligned in x and y dimensions. The *junction* is the crosspoint where two wires crossing perpendicularly. At any crosspoint, diode or transistor can be formed by using either *molecular nanodevices* [17], *semiconductor nanowire* [18], or *magnetic valve* [19]. The attractive facts of these configurable switches are non-volatile and extremely small size. The former enables the evasion of using separate devices (e.g. memory) to hold circuit the information for configurable circuits/systems [17], while the latter realizes the likelihood of having very high density up to approximately 10^{12} gate-equivalents/cm^2 [20]. Despite of the very highdensity, it is also estimated that the defect densities will be also high possibly at least 10% of the total density [21].

For example, Fig. 2(a) pictures the implementation of a basic logic gate on the crossbar-based architecture. The left and middle vertical wires are configured as inputs A and B, while the middle horizontal wire is set as an output C.

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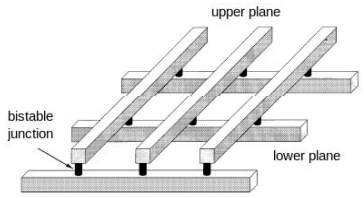

Fig. 1. Schematic of nanowire crossbar-based nanoarchitecture.

The black-colored molecular switches are configured as diode. Whilst, the white-colored molecular switches are configured as highly resistive opens. The equivalent electrical circuit is a diode-resistor logic that operates as OR gate as shown in Fig. 2(b). More complex circuit can also be performed by configuring desired molecular switches to be diode or highly resistive open.

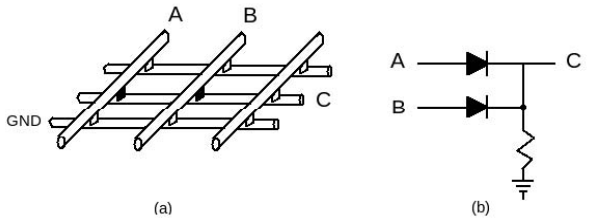

Fig. 2. OR gate implementation in crossbar based nanoarchitecture and the equivalent resistor-diode circuit.

III. Classification of Crossbar-based Hybrid Nanoarchitectures

The crossbar-based hybrid nanoarchitectures can be classified into two distinct dimensional structure namely *two-dimensional (2-D) structures* and *three-dimensional (3-D) structures*, as exhibited in Fig. 3. They are briefly defined next.

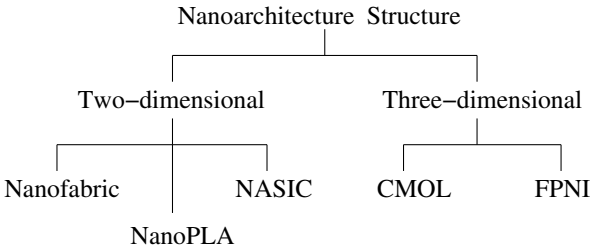

Fig. 3. Classification of crossbar-based hybrid nanoarchitectures.

- *Two-dimensional structures*: The CMOS-scale wire and nanodevice crossbars (used to from these nanoarchitectures are fabricated on the same plane (die)). The crossbar is two perpendicular wires aligned in x and y dimension as mentioned in Section II. *NanoFabrics*, *Nanoscale Programmable Logic Array (NanoPLA)* and *Nanoscale Application-Specific Integrated Circuit (NASIC)* fall into this class.
- *Three-dimensional structures*: The CMOS and nanodevice crossbars (used to from these nanoarchitectures are fabricated on different planes (dies)). The nanowire crossbar is placed on top of CMOS-scale wire crossbar, which creates a third dimension z. *CMOS/nanowire/molecular (CMOL)* and *Field-Programmable Nanowire Interconnect (FPNI)* fall into this class.

IV. Two-Dimensional Crossbar-based Hybrid Nanoarchitectures

This section discusses the three-dimensional crossbar-based hybrid nanoarchitecture namely NanoFabric, NanoPLA and NASIC.

A. NanoFabric

Nanofabric is introduced by Goldstein and Budiu and is based on the chemically assembled electronic nanotechnology (CAEN) [10]. The nanoFabric aims to replicate the current FPGA's island-style architecture using nanowires. The nanoFabric architecture consists of cluster arrays which interconnected by long nanowires as shown in Fig. 4(a).

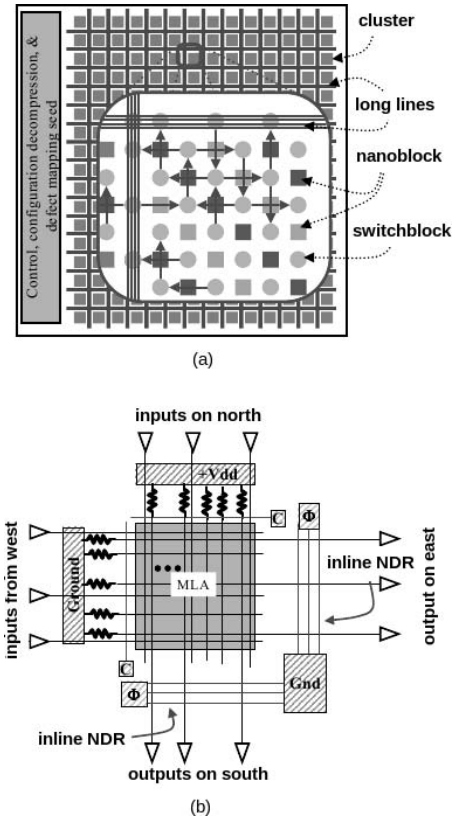

Fig. 4. Schematic of (a) Nanofabrics. (b) nanoblock [10].

Within each cluster, the main components called *nanoblock* and *switchblock* are resided. The nanoblock is an analogous function as configurable logic block (CLB) in FPGA which can be configured to perform logic functions. The

switchblocks provide interface between four adjacent nanoblocks. The nanoblocks in the boundary of the cluster are interfaced to the long interconnect nanowires. The long nanowires have various lengths such that signals are allow to transmit to one or more cluster without going through any switches.

The heart of the nanoblocks is a molecular logic array (MLA) which has three-bit input and three-bit output (north-south pins) and their complements (west-east pins) as pictured in Fig. 4(b). The MLA performs the boolean logic function. The structure is formed using semiconductor nanowires and reconfigurable switches in series with a diode at crosspoints. In order to have signal inversion and gain, negative differential resistor (NDR) latches are placed at the output of the MLA. For the switchblocks, the structure is similar to MLA but without the power/ground connections and NDR latches.

While nanodevices explicitly realize the logic and routing, CMOS provides fundamental functionality such as clocking, power, ground, configuration wires, control and primary input/output lines. Combining the advantage of these two techniques (CMOS-nanodevices) can produce a high density, e.g in [10] claimed that, the density of the FPGA fabric can be as high as 1M blocks/cm^2.

B. nanoPLA

Nanoscale Programmable Logic Array (NanoPLA) proposed by DeHon et al. uses Silicon nanowires (SiNW) or carbon nanotubes (CNT) and microscale wires (microwires) to build crossbar-based hyrid nanoarchitecture [11]. The basic block of NanoPLA is the two stages of programmable NOR-OR gates arrays as illustrated in Fig. 5(a). It is also possible to have two consecutive NOR-NOR nanoarrays by inverting the second stage output. It is logically equivalent to AND-OR logic of conventional PLA, and that is the reason the structure is called nanoPLA. Each crosspoint of nanoarrays can be electrically switchable to act as p-type diode. By applying sufficient voltage, these crosspoints can be either attracted or repulsed by the same or opposite polarities. For restoration purposes, the SiNW or CNT is doped to act as field-effect transistor (FET). Fig. 5(b) shows an m-input pFET NOR logic circuit. The m number of p-type doped SiNW covered with oxide forming FET junctions when crossing an n-type dope nanowire.

While the nanowires form the nanoarrays, microscale wires are used to access the nanoarrays. In order to access the nanoarrays form the microwires, a special decoder is used. A set of v nanowires that connect the nanoarray are intersected with w nanowires, which in turn are connected to w microwires in the decoder area as shown in Fig. 5(c). For reading the output from nanoarray the v nanowire is connected to single microwire which is placed perpendicular to them.

The experiments (that map benchmark circuits in this nanoarchitecture fabric) have shown better density of one or two order of magnitude as compared to 22nm CMOS projected technology node [23].

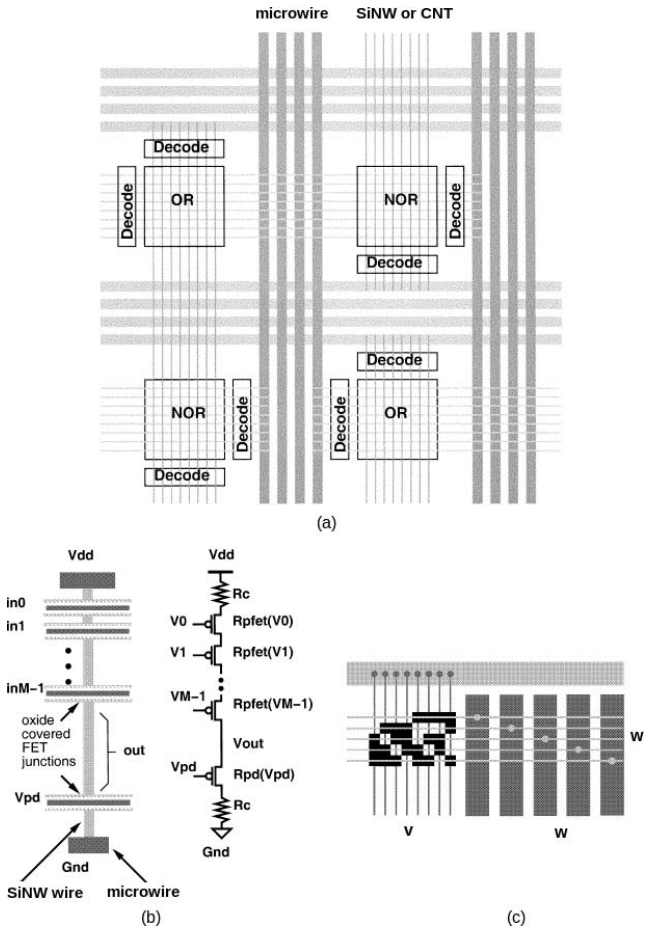

Fig. 5. Schematic of (a) NanoPLA. (b) pFET NOR logic circuit. (c) nanoblock [11].

C. NASIC

Weng et al. propose a nanoarchitecture that can be configured into an application domain known as NASIC [12], [24], [25]. Generally, NASIC is modification of the nanoPLA. Instead of having NOR logic gates NASIC can have arbitrary logic functions. The two-dimensional crossbar (grid) of Silicon nanowires having the junctions acting as field effect transistors (FETs) or P-N diodes form the basic building blocks. The basic block known a tile can be fabricated to have fundamental logic circuits like flip-flops, multiplexers, adders, etc. Microwires are used as global communication between tiles and configuration lines.

Fig. 6 presents the structure of 1-bit adder implemented in NASIC. The thicker and thinner wires are microwire and nanowire respectively. The doped *t* nanowires are in horizontal plane and doped *u* nanowire are the vertical plane. The doping of these nanowires determines the types of transistor; either pFET or nFET or even no connection between nanowire crossbar (similar to nanoPLA [11]). Pattern decoder such in [11] is needed to interface microwires to nanowires, V_{dd}, and GND.

In order to compared the difference in required area between

CMOS and NASIC, an experiments is performed. Durint experiment, a wire streaming processor is designed on 30nm [24] and 18nm [25] CMOS was compared withe the same circuit desigened using NASIC. Synthesization results each shows that CMOS occupies around 15× and 12× larger than NASIC, respectively.

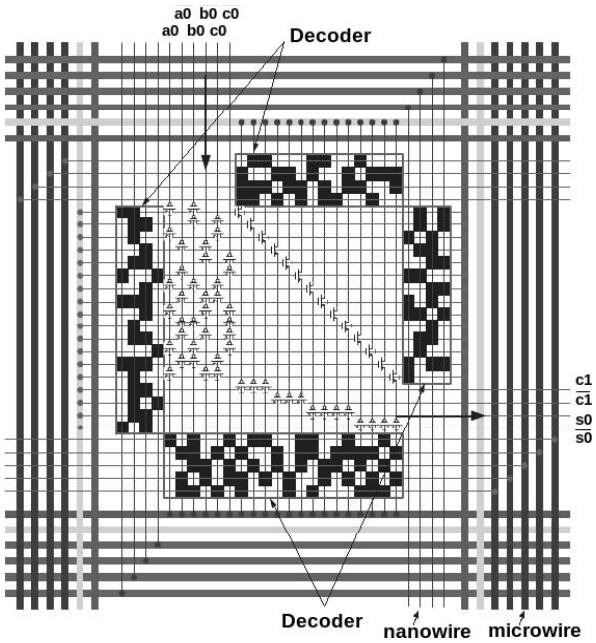

Fig. 6. Schematic of (a) 1-bit adder implemented on NASIC [12].

V. Three-Dimensional Crossbar-based Hybrid Nanoarchitectures

This section discusses the three-dimensional crossbar-based hybrid nanoarchitecture namely CMOL and FPNI.

A. CMOL

A combination of CMOS/nanowire/molecular nanodevices called as CMOL is introduced by Likharev and Strukov [26], [13]. In this structure, the nanowire crossbar with molecular nanodevice sandwiched at every crosspoint junctions are fabricated on top of CMOS stack. The top view and side view of generic structure of CMOL is illustrated in Fig. 7(a) and (b) respectively. The nanowires crossbar connected to CMOS-scale wire via interface pins (black dots) in the relay cells are rotated by some angle, $\alpha = \arcsin\,(F_{nano}/\beta F_{CMOS})$. Here, $F_{nano}(F_{CMOS})$ is the size of nanowire (CMOS) half-pitch and β is dimensionless factor larger than 1 depending on the complexity of CMOS cell [26]. The bottom-right (top-left) interface pins contact CMOS-scale wires to top (bottom) level nanowires. The top level nanowires extend along the whole CMOL chip. On the other hand, bottom level nanowires are segmented by certain length so that a tile can be interfaced to the other tiles surrounding the original tile within a *connectivity domain* [13]. The bottom level nanowires that extend over *r* tiles will have r^2 programmable nanodevices at the crosspoints of nanowires.

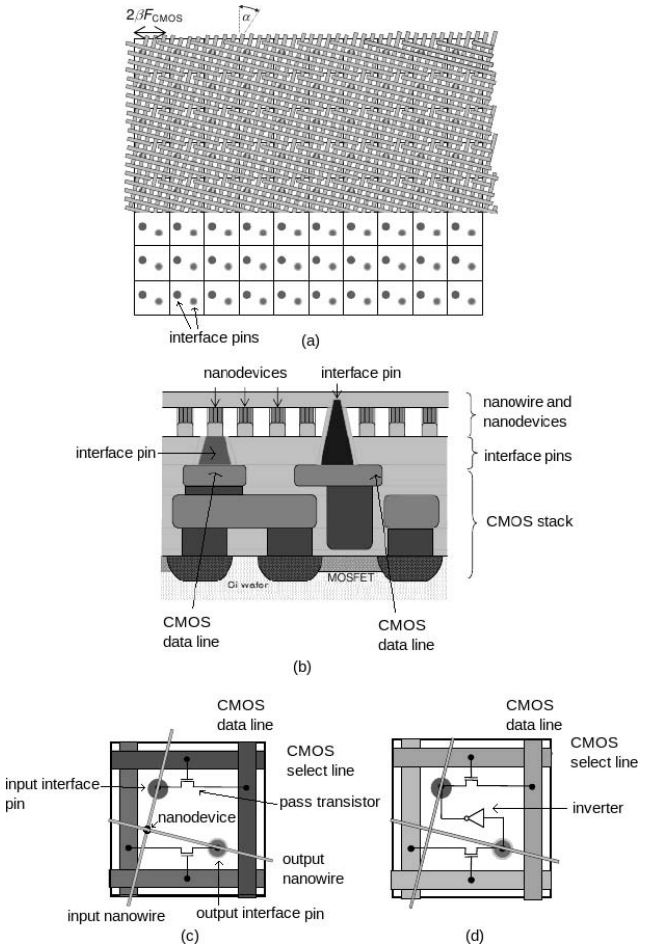

Fig. 7. Schematic of CMOL (a) top view. (b) side view. (c) memory tile. (d) logic tile [13], [26].

The most straightforward applications of CMOL are embedded and stand alone memories. The CMOL memory is comprises of $(2\beta F_{CMOS})^2$ area size of square-shape tiles where two pass transistors reside in each tiles as shown in Figure 7(c). CMOS-nanowire interface is made via the two pass transistors leading to programmable nanodevice that serve as 1-bit memory cell. The nanodevices such as single electron devices [26], [13], molecular nanodevices [17], semiconductor nanowire [18] or magnetic valve [19] in the architecture can be used as the 1-bit memory cell. In contrast, the CMOS subsystem will be the encoder, decoder, driver and input/output interfaces.

CMOL FPGA architecture has also been proposed for logic operations [13]. The architecture composes of uniform square-shape tiles. Each tile formed by one latch cell and twelve basic CMOS cell extend on all sides of the latch cell simultaneously. The latch cell consists of one latch and two pass transistors for configuration. A basic CMOS cell is built of an inverter and two pass transistor as shown in Figure 7(d). The bottom-left pass transistor is connected to input nanowire, whilst the top-right pass transistor provides the interface to output nanowire. The inverter is used to invert input signal as well as signal restoration. This tile structure basically forms a configurable

logic block (CLB) as in normal field-programmable grid array (FPGA).

Another application suggested by the is crossnet neuromorphic networks [27]. Essentially, the tiles of the crossnet neuromorphic networks compose of much bigger basic and latch cell compared to FPGA. The size is proportionally to the complexity of specific digital signal processing task to be implemented.

It is projected that 1 Terabyte CMOL-based memories can be fabricated on 2×2 cm^2 chip [26]. The comparison between CMOL FPGA and CMOS FPGA chips has been done by implementing 32-bit Kogge-stone adder in both circuit [13]. The result when using same F_{CMOS} only utilized 110 μm^2 in CMOL FPGA compared to 39,000 μm^2 in CMOS FPGA. For crossnet neuromorphic, it is estimated that the specific network architecture called Distributed Crossbar Network simply outperform CMOS 3GHz digital signal processor when running three hours image recognition processing task [28].

B. FPNI

Snider and Williams introduce a generalization of CMOL circuits, namely FPNI [14]. The FPNI trades of some of the CMOL advantages such as density and defect tolerance for easier fabrication, lower power dissipation and greater freedom in the selection of nanodevices in the crossbar junctions. The significance difference between FPNI and the other nanoarchitecture is that in FPNI the logic computations are performed in CMOS. Nanowire is used for signal routing. Moreover, the logic functions that can be implemented in FPNI are not restricted only to inverter as in CMOL. Thus more complex functions can be realized using FPNI.

The side and top view of FPNI are pictured in Fig. 8(a) and (b). As we can see, the nanowire pads that cover the interface pins (formed by two-way L-shape nanowire) are bigger compared to other parts of the nanowires. The two-way L-shape nanowires originate from the center of the pad extend to opposite side toward other nanowires. The nanowire crossbar is also rotated such that each nanowire connects to one interface pins. Furthermore, the CMOS-scale interface pins are used of conical pins in CMOL. This key idea realizes

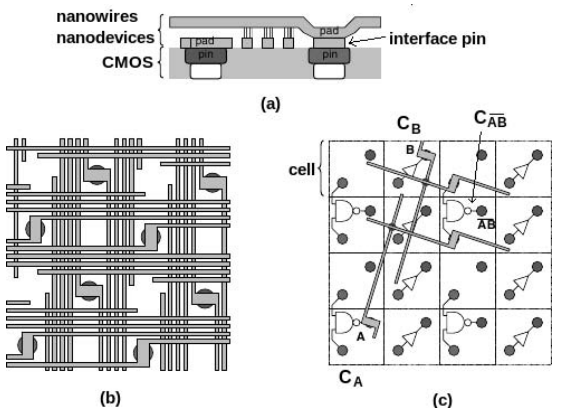

Fig. 8. Schematic of CMOL (a) side view. (b) top view. (c) arbitrary logic implemented in CMOL tiles [14].

easier fabrication process.

Fig. 8(c) shows square tiles of CMOS layer implementing logic function, $F = \overline{A.B}$, using buffers and NAND gates. The selected interface pins configured as resistor connecting the output of the NAND gate in cell C_A and the output of the buffer in cell C_B to the inputs of the NAND gate in cell $C_{\overline{AB}}$. Since each NAND gate occupies three interface pins, there are some tiles left without any logic implemented on it. This is another weakness of FPNI compared to CMOL.

However, FPNI still performs better than standard CMOS in terms of area overhead. Experiment analysis on Toronto benchmark circuits shows that FPNI have higher density, approximately 2.6$\times$ denser than 45nm CMOS technology [14].

VI. Comparison of the Proposed Crossbar-based Nanoarchitecture

Table I compares structures and function parameters of five nanoarchitectures; three two-dimensional nanoarchitectures (i.e. Nanofabric, NanoPLA, and NASIC) and two three-dimensional one (i.e. CMOL and FPNI). All nanoarchitectures are invented to operate as single computational function except CMOL. Nanofabrics and FPNI are targeted as FPGA, NanoPLA as PLA, and NASIC as processor. CMOL can implement either memory, FPGA for Boolean logic or neuromorphic network processor for specific computation (signal processing). Except FPNI, the other four nanoarchitectures utilize CMOS as supporting functions such as global communication. Instead, FPNI uses CMOS as the main computation logic which is performed by nanodevices in other four nanoarchitectures. Interconnects between nanowires and microwires in NanoPLA and NASIC are based on coded nanowire, which can be patterned during the fabrication process. However, CMOL and PFNI employ pins. No details on CMOS-nanowire interface in Nanofabric. Overall, CMOL exhibits the most promising nanoarchitecture among these five nanoarchitectures. Multi-computational functions that can be implemented on CMOL is the main reason to support this proposition. As a matter of fact, FPNI is the modification of CMOL apart of another work done to build three-dimensional CMOL [29].

VII. Conclusion

In this paper, we have discussed the emerging nanoarchitectures that can be utilized for future computing systems. The nanoarchitectures are based on crossbar-based architecture, implemented in hybrid CMOS/nanodevices structure, and realized using CMOS and nanolectronic technologies. These emerging nanoarchitectures exploit the advantages of mature and reliable CMOS technology and small self-assembled nanodevices to form electronic circuits. As CMOS, the backbone of current computing systems is predicted to hit the "red brick wall" approximately in the end of next decade, research on new architecture such presented in this paper, especially CMOL nanoarchitecture, must be initiated and further developed to ensure computer systems to be still alive in the future nanoelectronic era and beyond.

TABLE I
COMPARISON OF SEVERAL PROPOSED NANOARCHITECTURES.

Architecture	Nanofabrics	NanoPLA	NASIC	CMOL	FPNI
Circuit Dimension	2-D	2-D	2-D	3-D	3-D
Computation Functions	FPGA	PLA	Processor	Memory, FPGA neuromorphic processor	FPGA
CMOS Functions	Clocking Power, Ground Configuration wires	Addressing Data routing Configuration wires	Control Addressing Configuration wires	Inversion Demultiplexing	Arbitrary Logic
Nanodevices Functions	Arbitrary Logic Routing	NOR-NOR Logic	Arbitrary Logic Interconnect	NOR Logic Routing Memory cell	Interconnect Routing
CMOS-Nanowire Interface	–not mentioned–	Coded nanowires	Coded nanowires	Conical pins	CMOS pins

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