A Unified Aging Model of NBTI and HCI Degradation towards Lifetime Reliability Management for Nanoscale MOSFET Circuits

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***Abstract*—As planar MOSFETs is approaching its physical scaling limitation, FinFET becomes one of the most promising alternative structure to keep on the industry scaling-down trend for future technology generations of 22 nm and beyond. In this paper, we propose a unified reliability model of Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI) for double-gate and triple-gate FinFETs, towards a practical reliability assessment method for future FinFETs based circuits. The model is based on the reaction-diffusion theory and extends it such that it covers the FinFET specific geometrical structures. Apart of introducing the reliability model we also investigate the circuit performance degradation due to NBTI and HCI in order to create the premises for its utilization for assessing and monitoring the Integrated Circuits (ICs) aging process. To validate our model we simulated NBTI and HCI degradation and compared the obtained V_{th} shift prediction with the one evaluated based on experimental data. The simulations suggest that our model characterize the NBTI and HCI process with accuracy and it is computationally efficient, which makes it suitable for utilization in reliability-aware architectures as reliability prediction/assesment kernel for lifetime reliability management mechanisms.**

I. INTRODUCTION

An aggressive device dimension scaling of the Integrated Circuits (ICs) has been going on for the past decades while the supply voltage is not scaled proportionately, which inevitably leads to a rising reliability concern on multiple degradation mechanisms, such as Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI) [1]–[5], gate-oxide wear out, and so on. When the industry is entering the nanoscale era, the worries about reliability is even worsened, as their bottom-up manufactering processes are inherently prone to defects and their runtime faults are expected to be high, caused by shunkened device demensions and low supply voltages. Consequently, it has become necessary to introduce some reliability management schemes to make the system meet the lifetime specifications in advanced process nodes.

The priori lifetime requirements are mostly made based on worst-case assumptions, which leads to highly conservative margins on technology parameters, like supply voltages. In order to take full advantage of the technology improvement, new reliability prediction and assessment models with good accuracy and low complexity can be introduced, then efficient reliability-aware architectures could be implemented in future.

Moreover, apart from the pessimism implied in traditional methodologies requires to be revised, new characteristics of novel nanescale devices should be also taken into considerration in the new scheme for reliability management, as the conventional MOSFET planar structure is approaching its physical limits. Among various emerging devices for future nanotechnology circuits and systems, the multi-gate field effect transistors, e.g., MuFETs [6], FinFETs [7], represent one of the most promising alternative structures, due to their improved electrostatic control and drive current, therefore reduced Short Channel Effect (SCE) relative to bulk CMOS technology. The new geometrical features of these new structures introduce new degradation processes to the device.

Within all the degradations a device experiences during its operational life, the NBTI and HCI stresses have a very similiar physical progress. Both of these degradations are related to the generation of interface traps causing Si dangling bonds at the Si/SiO_2 interface. NBTI is prominent in PMOS devices along the entire channel when negative gate-to-source voltage is applied, while HCI is prominent in NMOS devices and occurs near the drain end due to the ”hot” carriers accelerated in the channel. The interface traps accumulates at the Si/SiO_2 interface then cause a threshold voltage (V_{th}) shift, which results in poor drive current and shorter device and circuit lifetime. Recent experimental investigations indicate that MuFET devices with standard orientation exhibit worse NBTI than planar devices due to the higher availability of Si-H bonds at the (110) oriented fin sidewalls [1]. Furthermore, a self-heating effect [8] caused by the SOI body may speed up the NBTI degradation for its thermal-activated nature. FinFET exhibits an improved HCI immunity with decreasing fin width [5], however, its immunity significantly depends on several factors, such as interface state generation, self heating effect, and temperature-dependent bandgap energy [9]. As a result, NBTI and HCI remains major reliability concerns for the FinFET devices and its circuits.

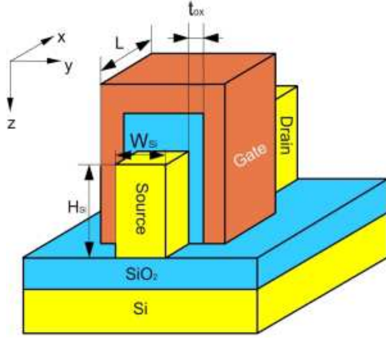

Fig. 1. SOI FinFET Schematic View.

NBTI and HCI have been well studied and understood for planar structure MOSFETs. Traditionally, NBTI degradations are modeled by Reaction-Diffusion (R-D) model [10]–[12], and HCI degradations are mainly modeled by "lucky-electron" model [13]. HCI can also be modeled under R-D theory framework as well [14], and a geometry-dependent unified R-D model for NBTI and HCI has been proposed for planar and surround-gate MOSFET [11]. However, for one thing, that model doesn't capture all the FinFET's features, e.g., the high aspect (H_{Si}/W_{Si}) ratio. For another thing, the impact of NBTI and HCI degradations on the circuits performance has been not well studied yet, while general and accurate reliability models for future circuit designs, especially for the lifetime reliability management, would be extremely helpful. Furthermore, the R-D model uses threshold voltage V_{th} shift as a proxy of NBTI or HCI stress, while lucky-electron model uses peak substrate current I_{sub}. This will increase the computation complexity and resource consumption of the implementation for reliability management, because two different kinds of sensors for voltage and current respectively have to be introduced. Since both degradations can be modeled under the same R-D framework, a unified aging model of NBTI and HCI stress will give future benifit on simplicity and efficiency for implementation.

In this paper, we propose a unified NBTI and HCI degradation model for double-gate and triple-gate FinFETs. The models fall under the R-D theory framework and captures the FinFET specific geometrical aspects. The proposed model unifies NBTI and HCI degradations, which simplifies the simulation complexity thus makes it suitable for its utilization in circuit simulation. Moreover, based on this reliability model, we also introduce a due to NBTI and HCI circuit performance degradation model that is able to capture and predict the aging process inside the ICs. To validate our model we simulated NBTI and HCI degradation and compared the obtained V_{th} shift prediction with the one evaluated based on experimental data. The simulations suggest that our model characterize the NBTI and HCI process with accuracy and it is computationally efficient, which makes it potentially applicable for lifetime reliability management schemes to be included in reliability-aware architectures.

II. Reliability Model for NBTI and HCI

A. Basic R-D Model

As mentioned before, NBTI and HCI are the physically origins for the Si-H/Si-O bonds breakage at the Si/SiO_2 interface. NBTI occurs in negatively biased transistors at elevated temperature. Holes from the inversion layer can tunnel into the gate oxide, break the Si-H bond leaving behind an interface trap. While in hot carrier injection process, the energetic "hot" electrons accelerated by the lateral electric field in the channel can inject themselves into the oxide near the drain and cause an interface trap too. The H atom released in this process diffuses away from the Si/SiO_2 interface. Consequently, interface charges are induced, raising the threshold voltage V_{th}.

Conventionally, NBTI and HCI are modeled separately. While it might be possible to evaluate these degradations individually in experiments and testing, it is hardly to separate them in a real operating circuits. Therefore, when targeting an online IC lifetime management able to capture and predict aging phenomena, a unified aging model is of interest as it reduces the resource overhead and the complexity of monitoring process.

Given the initial concentration of the Si-H bonds, i.e., N_0, the net rate of increase in interface trap density is given by

$$\frac{dN_{IT}^{NBTI}}{dt} = k_f(N_0 - N_{IT}) - k_r N_{IT} N_H^{(0)} \tag{1}$$

where k_f and k_r are the forward and reverse reaction rates, respectively. $N_H^{(0)}$ is the hydrogen density at the Si/SiO_2 interface.

The generated hydrogen species diffuse away from the interface toward the gate, driven by the gradient of the density. The process is governed by the Fick's law, as follows

$$\frac{dN_H}{dt} = D_H \cdot \nabla^2 N_H, \tag{2}$$

where D_H is hydrogen diffusion constant. This diffusion equation is geometry dependent, thus its solution requires fabrication technology details for the device under consideration, i.e., FinFET in our case.

B. Hydrogen Diffusion in Finite-Size Space

According to [15] the interface trap generation rate is very slow, thus we can assume that $dN_{IT}/dt \approx 0$ and $N_{IT} \ll N_0$, case in which Equation (1) can be simplified as follows:

$$N_{IT} N_H^0 \approx \frac{k_f}{k_r} N_0. \tag{3}$$

Given that one hydrogen atom is associated with an interface trap, the total number of broken Si-H bonds equals the total hydrogen concentration in the gate stack, which results in the following interface trap density:

$$N_{IT}(t) = \int_0^{x_{DF}(t)} N_H(x,t)dx, \tag{4}$$

where $x_{DF}(t) = f(D_H, t)$ is the length of the hydrogen diffusion front.

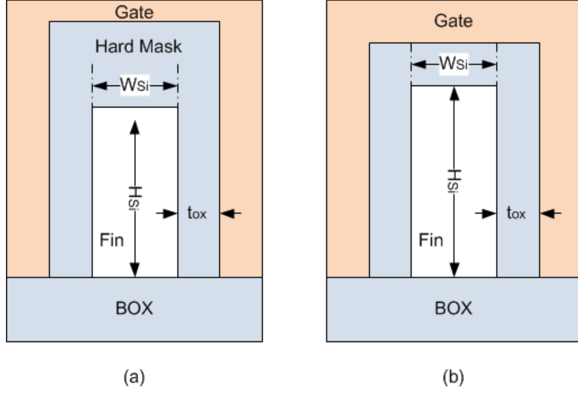

Fig. 2. Schematic view of cross section for (a) Double-Gate FinFET; (b) Triple-Gate FinFET. The main deference between these two structures is that Double-Gate FinFET has a thick dielectric hard mask on the top of the Fin.

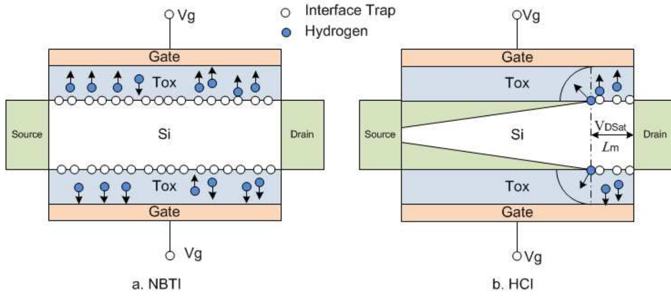

Fig. 3. Interface traps generation and hydrogen diffusion in Double-Gate (DB) FinFET Channel (top-view): (a) NBTI in DB FinFET; (b) HCI in DB FinFET.

For 1-D diffusion, the diffusion front can be expressed as $x_{DF}(t) = \sqrt{D_H t}$. Substituting this value in Equation (4) we obtain:

$$N_{IT}(t) = \int_0^{\sqrt{D_H t}} N_H(x,t)dx = \frac{1}{2} N_H(0)\sqrt{D_H t}. \qquad (5)$$

Inserting N_{IT} according to Equation (5) into Equation (3) results in the following 1-D diffusion interface trap density:

$$N_{IT}^{1-D} = \sqrt{\frac{k_f N_0}{2k_r}} (D_H t)^{\frac{1}{4}}. \qquad (6)$$

The 1-D diffusion hypothesis is based on the assumption that the gate plane has an infinite extent relative to the diffusion front, thus the source of reaction is a 2-D surface. When device dimension shrinks or the geometrical structure changes, the shape of the trap generation source can degrade into a line at the device edge or a dot at the corner, which give 2-D diffusion and 3-D diffusion of hydrogen, respectively. Solving Equation (4) in a similar way as above for 2-D and 3-D diffusion models, respectively, results in the following interface trap densities [16]:

$$N_{IT}^{2-D} = \sqrt{\frac{\pi k_f N_0}{12 k_r}} (D_H t)^{\frac{1}{2}}, \qquad (7)$$

$$N_{IT}^{3-D} = \sqrt{\frac{\pi k_f N_0}{24 k_r}} (D_H t)^{\frac{3}{4}}. \qquad (8)$$

One can easily conclude from Equations (6) to (8) that the rate of traps generation is certainly determined by the device structure.

C. NBTI and HCI in FinFETs

For a Double Gate (DG)-FinFET as depicted in Figure 2a, with a presence of hard mask on the top of the fin body, the degradation at the top corners can be neglected since the hard mask is designed to eliminate the parasitic inversion channels at there. With this assumption, we can consider that the DG-FinFET is equivalent with a normal planar double-gate device. Thus, the hydrogen diffusion due to NBTI and HCI can be illustrated as in Figure 3. The NBTI degradation now happens at both sidewall Si/SiO_2 interface with 1-D hydrogen diffusion, using Equation (6) the interface trap density can be estimated as follows:

$$N_{IT,NBTI}^{DG}(t) = N_{IT}^{1-D}(t) = \sqrt{\frac{k_f N_0^S}{2k_r}} (D_H t)^{\frac{1}{4}}, \qquad (9)$$

where N_0^S is the Si-H bond density available at the sidewall interface. We note inhere that the reaction rates k_f, k_r and the diffusion front distance D_H all have a temperate dependance, which can be expressed with the Arrhenius equation $k = Aexp(-E_a/k_B T)$.

For the HCI stress process, the hydrogen diffusion follows a 1-D rule in the velocity saturation region and a 2-D rule at the pinch-off point (see Figure 3b). In view of that, by using Equation (3), (6) and (7), and conducting a derivation similar to the work in [16] for the DG-FinFET geometrical structure, we obtain the interface density due to the combination of these two diffusion processes as follows:

$$N_{IT,HCI}^{DG}(t) = \sqrt{\frac{2k_f N_0^{HCI}}{k_r}} \left[(D_H t)^{\frac{1}{2}} + \frac{\pi \cdot (D_H t)}{6L_m} \right]^{\frac{1}{2}}, \qquad (10)$$

where L_m is the velocity saturation region length. The initial "hot" carrier concertration N_0^{HCI} is given by $N_0 \frac{I_d}{W} e^{-\varphi_{IT}/q\lambda E_m}$, I_d/W is the channel current density, φ_{IT} is the critical energy for interface-state generation, λ is the mean-free-path and E_m is the peak lateral-electric field [13]. A simple approximation of L_m can be expressed as follows [17]:

$$L_m = \sqrt{\frac{2\epsilon_{Si}}{qN_A}[V_{DS} + \phi_{bi} - (V_{DSSat} + \phi_0)]}, \qquad (11)$$

where N_A is the channel dopant concentration, ϕ_0 is the bulk potential, and ϕ_{bi} is the build-in p-n junction potential. Assuming that $\phi_0 \approx \phi_{bi}$, we obtain

$$L_m = \sqrt{\frac{2\epsilon_{Si}}{qN_A}(V_{DS} - V_{DSSat})}. \qquad (12)$$

In the case of Triple Gate (TG)-FinFET, the corner effect must be taken into account. In [16] the authors proposed a model for TG-FinFET, but it is for a square channel case in which the equality of the width and height of the Si body

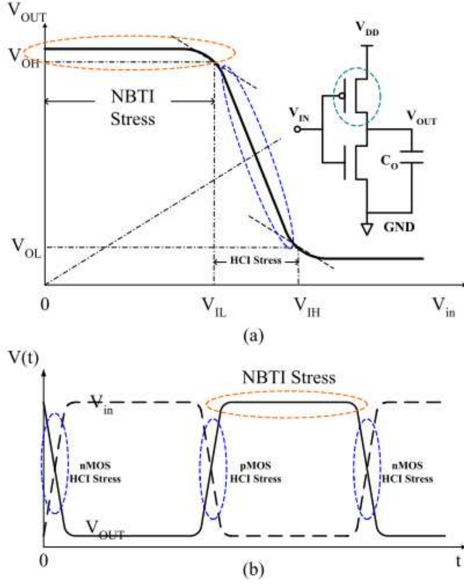

Fig. 4. Inverter NBTI and HCI Stresses Time Windows.

is assumed. Inhere we give a more generalized TG-FinFET model as follows:

$$N_{IT,NBTI}^{TG}(t) = \sqrt{\frac{2k_f N_0^S}{k_r}} \left[(D_H t)^{\frac{1}{2}} + \frac{\pi \cdot (D_H t)}{6H_{Si} + 3W_{Si}} \right]^{\frac{1}{2}}, \tag{13}$$

where H_{Si} and W_{Si} are the height and width of the Si body, respectively. For this case the HCI interface distribution will more complex due to the existence of the top gate in TG-FinFET. To simplify the issue, we assume that the top gate causes a modulation of the velocity saturation region length, by introducing a fitting parameter λ, case in which Equation (10) can be reformulated as follows:

$$N_{IT,HCI}^{TG}(t) = \sqrt{\frac{2k_f N_0^S}{k_r}} \left[(D_H t)^{\frac{1}{2}} + \frac{\pi \cdot (D_H t)}{6\lambda L_m} \right]^{\frac{1}{2}}. \tag{14}$$

The threshold voltage degradation induced by interface charges is given by

$$\Delta V_{th}(t) = \frac{qN_{IT}}{C_{ox}} = \frac{qt_{ox}N_{IT}(t)}{\epsilon_{ox}H_{Si}L_g}, \tag{15}$$

where t_{ox} is the gate oxide thickness, ϵ_{ox} is the oxide dielectric constant, and L_g is the gate length. So far, we obtained the reliationship between device parameter V_{th} and interface state density. In principle, V_{th} shift is proportional with the number of interface traps at the Si/SiO_2, which is a good proxy for the aging status of the device.

III. Lifetime Reliability Management

A. Lifetime and Aging Definition

To an electronic device or circuit, the term "Lifetime" means the time until an important material/device parameter degrades to a point that the device or circuit can no longer function properly in its intended application. Hence, by defining ΔV_{th} reaching some fraction P (in practice, this critical portion of a parameter degradation is defined to be 10% [18]) of the voltage threshold to be the End-of-Life, the aging status and its upper limit can be expressed as

$$Aging = \frac{\Delta V_{th}}{V_{th}} \equiv N_{IT}(t) \leq P. \tag{16}$$

B. Lifetime Reliability Management

Lifetime reliability management implies two concepts: reliability assessment and reliability prediction, which are associated to the current and the future reliability status, respectively.

In order to implement an online reliability management system, the current reliability status must to be firstly understood. The model we introduced in previous section is assumed to work under a DC condition. From the perspective of circuit operation, NBTI and HCI stresses have different time windows. HCI stresses the device only during the switching period when current flows through the channel, while NBTI happens even when the source/drain voltage is zero. The stress time window for NBTI and HCI is illustrated in Figure 4 for an inverter circuit. This stress time window is characterized by the device duty cycle, which is application specific. Furthermore, NBTI degradation has a well-known recovery subprocess when the stress is released [10]. In the work [19], the author gives the relationship between AC and DC stress condition, which is:

$$\begin{aligned} \Delta N_{IT}(AC) &= \alpha_{eff} \cdot \Delta N_{IT}(DC) \\ &= \sqrt{\frac{1}{t_0}\int_0^{t_0} \frac{V_{GS}^2(t)}{V_{GS,max}^2} dt} \Delta N_{IT}(DC), \end{aligned} \tag{17}$$

where t_0 is a sufficiently long time period such that $t_0 \gg T_{clk}$ and T_{clk} is the cycle period. By combining Equation (16) and (17) we obtain the following expression of the aging under AC conditions:

$$\Delta Aging(AC) = \Delta N_{IT}(AC) = \alpha_{eff} \cdot \Delta N_{IT}(DC). \tag{18}$$

Thus, we can have the current aging status evaluated as

$$Aging = \int_0^t dA dt = \sum_0^n \frac{\Delta V_{th}(AC)}{V_{th}} \cdot t_i, \tag{19}$$

where t_i is the ith time interval between two adjacent measurements.

IV. Results and Discussion

With trillions of transistors on a single chip in modern ICs, the aging process will further degrade into a failure distribution, rather than in an analytical curve as predicted by our model. Since in this paper we focus on the prediction of the evolution of the degradations in time, we carry on the model evaluation on one device only, i.e., an inverter as presented in Figure 4.

The main parameters of our model are as follows: (i) the reaction rate constants, k_f and k_r, and the diffusion front distance D_H, all of them being temperature dependent. For these parameters, the Arrhenius model is utilized then all of

them turn to depend on an activation energy, E_f, E_r, and E_H, respectively. Those activation energies can be measured by experiments and only depend on materials; (ii) the technology and geometry related parameters, e.g., ϵ_{Si}, N_0, N_A, H_{Si}, W_{Si}, which values can be derived from technology specifications; (iii) electronic parameters, which are V_{DS}, V_{DSSat}, E_m, L_m and can be calculated by SPICE alike models; and (iv) the fitting parameters introduced in our model. They are the modulation fitting parameter λ in Equation (14), which can be extracted by HCI test for TG-FinFETs relative to DG-FinFETs, and the AC effective activity factor α_{eff} in Equation (17), which is application specified and can be deduced via application profiling.

To verify our proposal, NBTI and HCI V_{th} shift prediction are evaluated based on experimental data in [1], [20], and [21] and compared with the degradations predicted by our model. We note that the fitting parameter values utilized in the reliability model we proposed were derived based on the technology definition and experiments . The results are depicted in Figure 5 for NBTI and in Figure 6 for HCI. Note that in the figures the solid lines correspond to the predicted values while the individual points correspond to values computed based on experimental data. One can observe that our proposal provides a good accuracy when compared with data derived from experiments. Worth to mention that for NBTI we obtain a root-mean-square-error less than 2%. The HCI prediction is less accurate however, since HCI has a dependence on the lateral electric field (E_m) and gate voltage, while NBTI just depends on the gate voltage only. In order to improve the accuracy of HCI model, more precise model for the lateral electric field distribution and pinch-off length should be introduced and this constitute a future work subject.

By modeling NBTI and HCI stesses in a unified R-D model framework, the number of fitting parameters in our model decrease significantly, then it further simplifies the parameter extraction model computation progress. Hence, a higher performance can be achieved by our model when comparing with other models, e.g., [22]. Furthermore, the degradation caused by NBTI and HCI stresses is indicated by a single proxy, i.e. threshold voltage shift ΔV_{th}, which reduces the resource consumption of the implementation for reliability management, since only one kind of aging sensor for voltage have to be introduced. In view of that the proposed model can be implemented with less resources and requires less computation effort, thus it enables a potential simple monitoring and prediction agent for reliability-aware computation architectures and platforms.

We also conducted a simple evaluation on the proposed unified reliability model, which results are depicted in Figure 7. From Figure 7, it can be observed that the V_{th} shift increases fast initially and changes decreasing slowly after that. This is due to the power-law of the hydrogen diffusion rate, therefore the interface state generation rate.

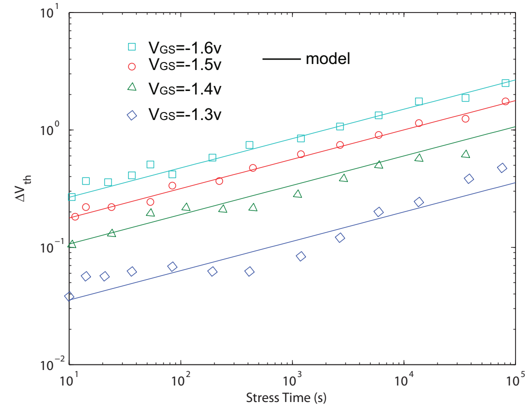

Fig. 5. V_{th} Degradation due to NBTI.

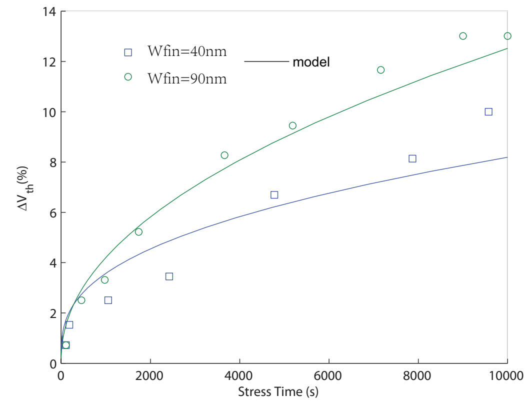

Fig. 6. V_{th} Degradation due to HCI.

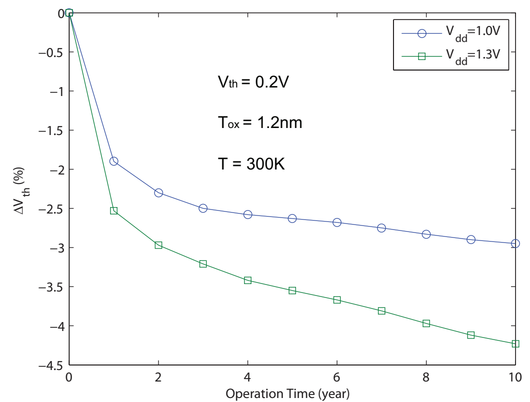

Fig. 7. V_{th} degradation due to the combined effect of NBTI and HCI.

V. Conclusions

In this work we proposed a unified reliability model for Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI) degradation specific for double-gate and triple-gate FinFETs and circuits. The proposed model is based on the reaction-diffusion theory and extends it such that it covers the FinFET specifics. Moreover we also investigated the circuit performance degradation due to NBTI and HCI in order to create the premises for the utilization of our proposal in assessing and monitoring the Integrated Circuits (ICs) aging process. To validate our model we simulated NBTI and HCI degradation and compared the obtained V_{th} shift prediction with the one evaluated based on experimental data. Our simulations suggest that the proposed model characterize the NBTI and HCI process with accuracy and it is computationally efficient, therefore we are currently working towards its implementation into lifetime reliability management mechanisms to make part of reliability-aware architectures.

References

[1] G. Groeseneken, F. Crupi, A. Shickova, S. Thijs, D. Linten, B. Kaczer, N. Collaert, and M. Jurczak, "Reliability Issues in MuGFET Nanodevices," in *Reliability Physics Symposium, IRPS. IEEE International*, May 2008, pp. 52–60.

[2] H. Lee, C.-H. Lee, D. Park, and Y.-K. Choi, "A Study of Negative-Bias Temperature Instability of SOI and body-tied FinFETs," *IEEE Electron Device Letters*, vol. 26, no. 5, pp. 326 – 328, May 2005.

[3] H. Shang, L. Chang, X. Wang, M. Rooks, Y. Zhang, B. To, K. Babich, G. Totir, Y. Sun, E. Kiewra, M. Ieong, and W. Haensch, "Investigation of FinFET Devices for 32nm Technologies and Beyond," in *International Symposium on VLSI Technology Digest*, 2006, pp. 54 –55.

[4] J. Park, J.-M. Park, S.-O. Sohn, J.-B. Lee, C.-H. Jeon, S. Y. Han, S. Yamada, W. Yang, Y. Roll, and D. Park, "Reliability Investigations for Bulk-FinFETs Implementing Partially-Insulating Layer," in *Proceedings of 45th Annual IEEE International Reliability Physics Symposium (IPRS)*, April 2007, pp. 378 –381.

[5] Y.-K. Choi, D. Ha, E. Snow, J. Bokor, and T.-J. King, "Reliability Study of CMOS FinFETs," in *IEEE International Electron Devices Meeting(IEDM) Technical Digest*, Dec. 2003, pp. 7.6.1 – 7.6.4.

[6] L. Risch, "Pushing CMOS Beyond the Roadmap," *Solid-State Electronics*, vol. 50, no. 4, pp. 527 – 535, 2006, papers Selected from the 35th European Solid-State Device Research Conference - ESSDERC'05.

[7] Y.-K. Choi, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "Sub-20 nm CMOS FinFET Technologies," in *International Electron Devices Meeting, IEDM Technical Digest*, 2001, pp. 19.1.1 –19.1.4.

[8] B. Tenbroek, M. Lee, W. Redman-White, J. Bunyan, and M. Uren, "Self-heating Effects in SOI MOSFETs and their Measurement by Small Signal Conductance Techniques," *IEEE Transactions on Electron Devices*, vol. 43, no. 12, pp. 2240 –2248, Dec. 1996.

[9] W.-S. Liao, Y.-G. Liaw, M.-C. Tang, S. Chakraborty, and C. W. Liu, "Investigation of Reliability Characteristics in NMOS and PMOS FinFETs," *IEEE Electron Device Letters*, vol. 29, no. 7, pp. 788 –790, July 2008.

[10] M. Alam, H. Kufluoglu, D. Varghese, and S. Mahapatra, "A comprehensive model for PMOS NBTI degradation: Recent progress," *Microelectronics Reliability*, vol. 47, no. 6, pp. 853 – 862, 2007.

[11] H. Kufluoglu and M. Ashraful Alam, "A Geometrical Unification of the Theories of NBTI and HCI Time-exponents and its Implications for Ultra-scaled Planar and Surround-Gate MOSFETs," in *IEEE International Electron Devices Meeting, IEDM Technical Digest*, Dec. 2004, pp. 113 – 116.

[12] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "An Analytical Model for Negative Bias Temperature Instability," in *Proceedings of the 2006 IEEE/ACM international conference on Computer-aided design*, ser. ICCAD '06. New York, NY, USA: ACM, 2006, pp. 493–496.

[13] C. Hu, S. C. Tam, F.-C. Hsu, P.-K. Ko, T.-Y. Chan, and K. Terrill, "Hot-Electron-Induced MOSFET Degradation: Model, Monitor, and Improvement," *IEEE Transactions on Electron Devices*, vol. 32, no. 2, pp. 375 – 385, Feb 1985.

[14] D. Lachenal, F. Monsieur, Y. Rey-Tauriac, and A. Bravaix, "HCI Degradation Model based on the Diffusion Equation including the MVHR Model," *Microelectron. Eng.*, vol. 84, pp. 1921–1924, September 2007.

[15] M. Alam, "A Critical Examination of the Mechanics of Dynamic NBTI for PMOSFETs," in *IEEE International Electron Devices Meeting, IEDM Technical Digest*, Dec. 2003, pp. 14.4.1 – 14.4.4.

[16] H. Kufluoglu and M. Alam, "Theory of interface-trap-induced NBTI degradation for reduced cross section MOSFETs," *IEEE Transaction on Electron Devices*, vol. 53, no. 5, pp. 1120–1130, May 2006.

[17] A. Bhattacharyya, *Compact MOSFET Models for VLSI Design*. Wiley-IEEE Press, 2009.

[18] J. W. McPherson, *Reliability Physics and Engineering: Time-To-Failure Modeling*. Springer, 2010.

[19] H. Kufluoglu, "MOSFET Degradation due to Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI), and its Implications for Reliability-aware VLSI Design," Ph.D. dissertation, Purdue University, USA, 2007.

[20] W.-S. Liao, Y.-G. Liaw, M.-C. Tang, S. Chakraborty, and C. W. Liu, "Investigation of Reliability Characteristics in NMOS and PMOS FinFETs," *IEEE Electron Device Letters*, vol. 29, no. 7, pp. 788 –790, July 2008.

[21] S.-Y. Kim, T. su Park, J.-S. Lee, D. Park, K.-N. Kim, and J.-H. Lee, "Negative Bias Temperature Instability (NBTI) of Bulk FinFETs," in *43rd Annual IEEE International Reliability Physics Symposium, Proceedings*, 2005, pp. 538 – 540.

[22] W. Wang, V. Reddy, A. T. Krishnan, R. Vattikonda, S. Krishnan, and Y. Cao, "Compact Modeling and Simulation of Circuit Reliability for 65-nm CMOS Technology," *IEEE Transaction on Device and Materials Reliability*, vol. 7, no. 4, pp. 509–517, DEC 2007.