A Flexible Active-Matrix Electronic Paper With Integrated Display Driver Using The μ-Czochralski Single Grain TFT Technology

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***Abstract*—This article describes the development of an Electronic Paper display. This E-Paper display will use the μ-Czochralski Single Grain Thin-Film Transistor Technology for driving a Quick-Response Liquid Power Display. The display driver will be integrated on the display itself. The display is flexible, including the driving electronics. Technology used offers great possibilities for future applications e.g. flexible electronics, three dimensional IC, System-on-Panel, ultra fast responding E-Paper displays etc. At the time of writing, several test circuits are being manufactured with the μ-Czochralski Single Grain Thin-Film Transistor Technology at the Delft Institute of Microsystems and Nanoelectronics (DIMES). A working prototype is scheduled for the first quarter of 2009.**

I. Introduction

With the use of μ-Czochralski Single Grain Thin-Film Transistor (SG-TFT) Technology [1], it is possible to fabricate low-temperature poly-silicon TFTs by excimer-laser crystallization of amorphous silicon. This technology offers great possibilities such as flexible electronics and 3D integration of ICs by stacking TFTs on top of each other [2]. We will use the SG-TFT Technology to make a flexible Electronic Paper (E-Paper). The first devices with E-Paper displays are now available for consumers. E-Paper offers several advantages over conventional displays and traditional paper.

For the display we with use a Quick-Response Liquid Powder Display (QR-LPD) [3] [4]. The display is flexible, has a paper-like appearance (paper white, wide view angle) and can retain an image without power, making it a perfect candidate for an E-Paper display. QR-LPD requires a relative high driving voltage of up to 70V, this posses some challenges on the display driver circuit. The display driver circuit can be divided in two parts, a high voltage and low voltage circuit part. The high voltage part is designed with great care and precision, ensuring that the SG-TFTs will survive 70V but still are able to control the output with enough precision for gray-scale levels. As for the low voltage digital circuit, this will be designed in VHDL. The synthesis will follow an automated circuit design [5] using the synthesis library specially designed for the SG-TFT Technology. The synthesis library consists of full custom basic cells while taking into account the constrains of the technology.

II. Technology

The E-Paper display that we are developing at the TUDelft is based on two technologies. The first is the μ-Czochralski Single Grain Thin-Film Transistor technology. This is used for the integrated electronics. The second is Quick-Response Liquid Powder Display technology developed by Bridgestone, the electrophoretic material for the E-Paper display. The following two subsection briefly describes the two technologies.

A. μ-Czochralski Single Grain Thin-Film Transistor

The μ-Czochralski Single Grain Thin-Film Transistor (SG-TFT) technology is used to make high performance transistors out of a-Si (amorphous silicon) by Excimer-laser crystallization (Figure 1). The electrical performance of these SG-TFTs are comparable to single-crystal transistors [6]. These transistors can be used for digital, analog and RF circuits. The process to make these SG-TFTs starts with a so called grain filter, this is done by patterning a grid of cavities in the SiO_2 backplane [1]. After that, a-Si is deposited on top. The Excimer-laser crystallization melts the top part of the a-Si, but leaves a seed at the bottom of the cavity. From these seeds high quality poly-Si islands will grow (Single Grain). Inside these grains source and drains are made by implanting with phosphorus and boron for NMOS SG-TFT and PMOS SG-TFT respectively. Although planar defects are present inside the Single Grains, it has been reported that these defects are less active then random grain boundaries [7] [8]. The fabricated SG-TFTs show electrical performance comparable to single-crystal transistor (see Table I).

All the fabrication steps are relatively low temperature ($<350°$). This makes it possible to fabricate SG-TFT on cost-effective plastic substrate for flexible electronics. In this case a flexible display with integrated display drivers. Another advantage of this technology is that it is possible to stack SG-TFTs on top of each other. A concept of this can be seen in Figure 10, each layer is used for a different purpose; display, digital electronics and analog electronics.

B. Quick-Response Liquid Powder Display

E-Paper has a paper-white appearance with high contrast and high reflectivity. For our E-Paper, we will use the electrophoretic material that has these properties: QR-LPD [4].

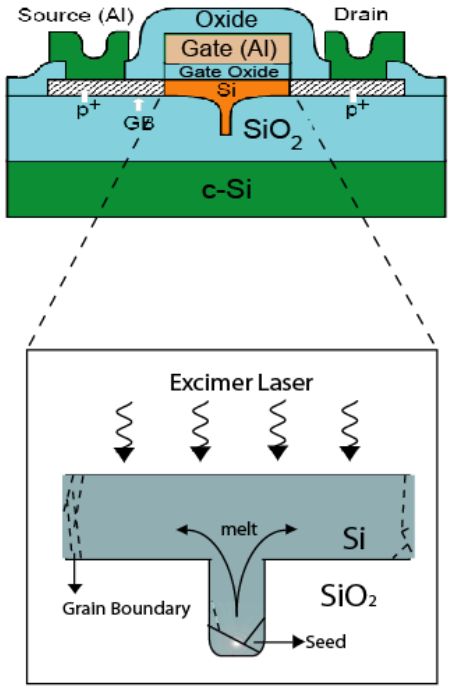

Fig. 1. μ-Czochralski Single Grain Thin-Film Transistor

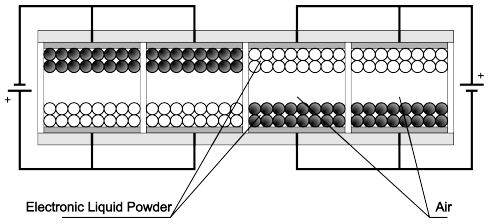

Fig. 2. Simple structure of QR-LPD

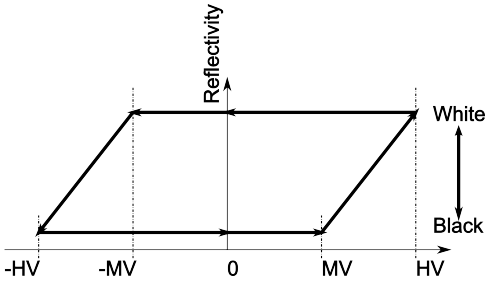

Fig. 3. Hysteresis plot, reflectance versus applied voltage. (Where HV stands for High Voltage and MV for Middle Voltage)

The QR-LPD (Quick-Response Liquid Powder Display) developed by Bridgestone uses a new "Electric Liquid Powder". This electrical sensitive powder combines the properties of a powder and liquid. The QR-LPD has a simple display structure (Figure 2). In a single cell there are two types of powder, negatively charged white powder and positively charged black powder. Plain air fills the remaining space of the cell. Two electrodes on top and bottom generate an electric field. With this electric field the liquid powder can be controlled. When applying a negative voltage over a cell, the top electrode will attract the black particles and the top of the cell will turn black. And when a positive voltage is applied to a cell, the white particles will move to the top electrode making the cell top white. The powder particles can move fast through the air within the cell, resulting in an ultra fast pixel response time of 0.2ms. The attractive forces (electrical and non-electrical) of the liquid powder particles [3] define a clear threshold voltage, this makes the QR-LPD an excellent bistable electrophoretic material. To overcome these attractive forces, the QR-LPD requires a relative high driving voltage of 70V with the threshold voltage at 35V. In Figure 3 a plot can be seen showing the relationship between the voltage applied and the reflectivity [4]. The clear threshold and the large hysteresis makes the display bistable.

III. The Electronic Display

We are designing a monochrome E-Paper display with the screen format of 320×240 pixels (QVGA). Each pixel will have 64 gray-scale levels (6 bits) and will be 120×120μm big. The viewable screen size will be 3.84×2.88cm, a screen diagonal of 4.8cm (slightly larger than 1.8 inch). Our aim is to reach 25 frames per second, making it possible to view animations fluently. This means that the system clock frequency will be at least 2 MHz.

The E-Paper display will use the technologies described in Section II. The SG-TFTs are needed for the active-matrix backplane (driving the QR-LPD), display drivers. This can be seen in Figure 4. The connections to the active-matrix backplane are organized as a matrix. Writing is done by selecting a line (Gate Driver) and then outputting the correct voltage on the columns (Data Driver) writing a single line at the time. This driving scheme is shown in Figure 7 but simplified. The Timing Control expects input signals similar to the VGA signals. Similar signal names are used, like clk, hsync, vsync. The Timing Control controls the Data Driver and the Gate Driver, so they stay synchronized for a correct output.

Subsection III-A describes implementation of the high voltage parts of the E-Paper display. The structure of the active-matrix back plane and the high voltage DACs (Digital to Analog Converters). In subsection III-B the implementation of the three main low-voltage circuits, the Gate Driver, the Data Driver, and the Timing Control are described.

A. High Voltage

A high voltage of 70V is required for driving the QR-LPD. The structure of the active-matrix back plane can be seen in Figure 5, the pixel is modeled as a capacitance (polymer between two electrodes). Each pixel is controlled by a transmission gate consisting of two complementary CMOS transistors. When the transmission gate is active, the voltage on the columns will transfer to the storage capacitance and the pixel electrode. All the pixels share a common electrode named Vcommon, this is an ITO plane (both electrical con-

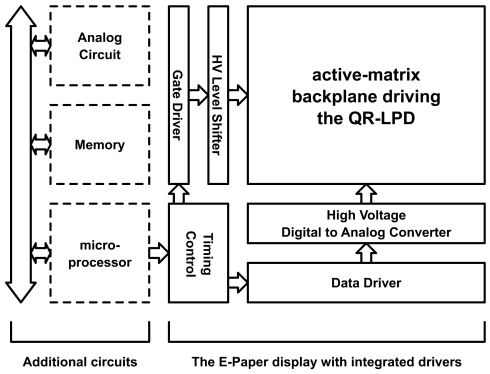

Fig. 4. A block diagram of the E-Paper display with integrated drivers and additional circuits

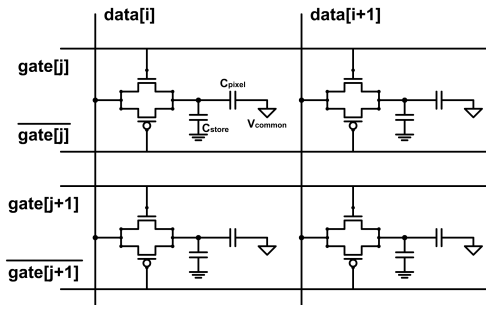

Fig. 5. schematic

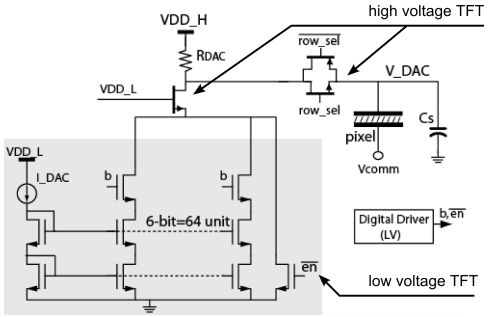

Fig. 6. Current driven DAC

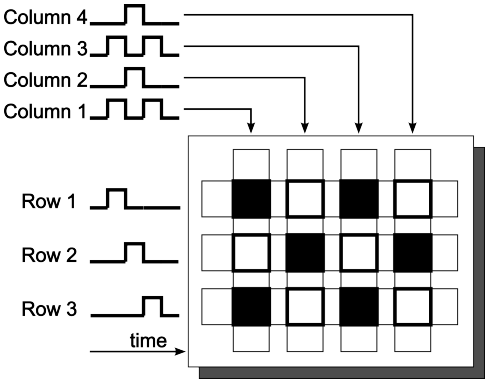

Fig. 7. Basic driving matrix scheme

ductant and optical transparent) on top of the E-Paper. With this common pixel electrode, writing and erasing is possible without negative voltages. For example making pixels black is done with 70V on the columns and Vcommon at 0V, erasing (making pixels white) is done with 0V on the columns and Vcommon at 70V.

Pixel reflectivity (black-grey-white) is a function of a potential difference over the liquid powder between the two electrodes. The relation between the reflectivity and the potential difference is not a linear function. This can be seen in the hysteresis plot in Figure 3. The display drivers supply these voltages when writing. An image is written one row at the time. With 320 columns, 320 voltages need to be generated at the same time. This is done with 320 DACs (Digital to Analog Converters). Many DAC architectures can be found in the literature [9] [10], mostly using passive network combined with switches. The main challenge in the display driver is to drive the pixel with a very high voltage up to 70V. The SG-TFT has a breakdown voltage at around 6V. A special high voltage TFT is under development to endure the high voltage without a breakdown, at the cost of its speed. These high voltage TFTs are not suitable as DAC switches since they are slow. On top of this, this DAC architecture needs to be driven with high voltage signals, requiring a (fast) level-shifter to convert the low voltage 5V digital signals to 70V signals just for the DAC, which is not practical. A better choice for DAC architecture will be a current driven DAC. The simplified schematic of the DAC is shown in Figure 6. The current sources and its switches can be built using the low voltage and fast SG-TFT. The current drives a resistive load which generate the output voltage. Between the resistive load and the current sources, a high voltage TFT is used to protect the current DAC network from the breakdown due to a large voltage swing. The cascode current sources are employed to minimize the current variation and cascode also reduces feed through effect due to the switching of the switches.

B. Low Voltage

The digital logic is running at 5V. The digital circuitry is generated using the automated circuit design path [5]. Starting from VHDL (a hardware description language), it then gets synthesized using the standards cells of the SG-TFT technology. Since the SG-TFT technology is relative new, only five standard cells are made. This makes it easy to adapt when the SG-TFT gets updated/improved. The following standard cells are made: Inverter, NAND, NOR, D-type FlipFlop and Buffer. This is enough to make all digital logic. The display driver consists of three major digital components, the Data Driver, the Gate Driver and the Timing Control. The basic driving scheme is illustrated in Figure 7. First, the correct voltages are put on all columns. Second, a row is activated by the Gate Driver. If potential difference over the pixels in the activated row exceeds the voltage threshold, the electric liquid powder of the pixels will move and thereby change the reflectivity of a pixel in the row.

The Data Driver is big serial to parallel shift register, shifting data words of 6 bits each clock cycle. The 6 bits

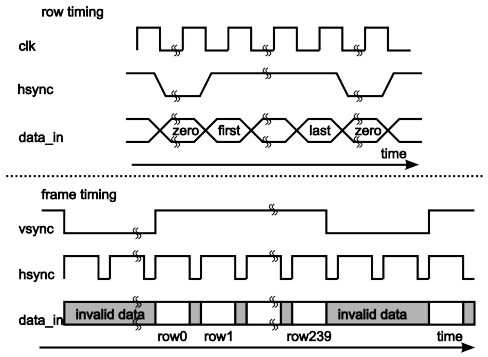

Fig. 8. top: Horizontal timing for a single row; bottom: Vertical timing for whole frame

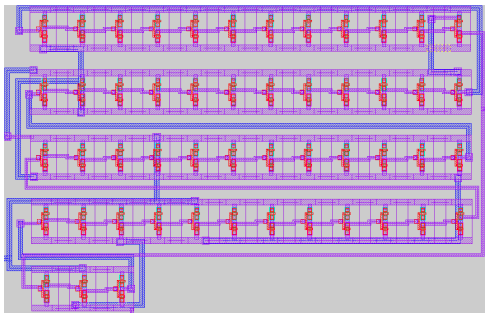

Fig. 9. Layout of the 51 stage ring oscillator

TABLE I
SG-TFT PERFORMANCE PARAMETERS

SG-TFT Device	Mobility μ_{FE} (cm^2/Vs)	Sub-threshold Swing (V/dec)	Threshold voltage (V)	Ioff(A)
NMOS	600	0.2	0.5	$1.3{\cdot}10^{-13}$
PMOS	270	0.13	-2.3	$1{\cdot}10^{-14}$

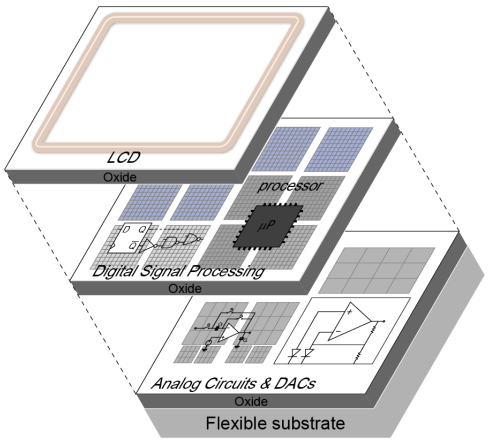

Fig. 10. Stacked ICs using the SG-TFT technology

are needed for the 64 grey scale levels for each pixel. When all the data words for a row are shifted in the Data Driver, the Data Driver then forwards all the pixel values to the DACs, so the correct voltages are on the columns of the E-Paper display. The Gate Driver activates a row of interest, by turning on the transition gates of that row. The voltages on the columns will create a potential differences over the electric liquid powder, changing the pixel values. By scanning with the Gate Driver, activating one row at the time, a frame is written row by row. The expected input signals for the Timing Controls can be seen in Figure 8. The use of the signals clk, hsync and vsync are similar to the driving signals of a VGA screen [11]. The shifting of pixel data can be seen in top of Figure 8, each clock cycle a data word is shifted in the Data Driver with the hsync signal marking the valid data words. The filling of a frame is illustrated at the bottom with the vsync denoting which hsync-rows contain valid data. The Timing Control uses these sync-signals to control the Data Driver and the Gate Driver, instructing them when data needs to be shifted, when the data needs to be outputted to the DAC and when the rows need to be activated. All this to keep the Data Driver and Gate Driver synchronized for the correct picture.

IV. PROGRESS

Previous experimental results show that the electrical performance of the SG-TFTs are comparable to single-crystal transistors [6]. These results are summed up in Table I. At the time of writing, several test circuits are being manufactured with the SG-TFT Technology at DIMES (Delft Institute of Microsystems and Nanoelectronics). Several of these test circuits are to test the high voltage transistors. These are designed to endure the driving voltage needed by the QR-LPD. Other test circuits are related to the low voltage digital circuits. Using the automated circuit design path, a 51-stage ring oscillator (Figure 9) and a 4 bit counter are designed. The first one is to test the speed of the inverters, the second one is for verification of the automated circuit design. The E-Paper prototype will be adjusted according to these test results. A working E-Paper prototype is expected for the first quarter of 2009.

V. CONCLUSION

This paper presents a combination of two new technologies and gives a preview for what is expected in the near future in the field of flexible electronics and electronic paper. The technologies used for this E-Paper, show promising features. The μ-Czochralski Single Grain Thin-Film Transistors show comparable electronic performance with the single-crystal transistors. With the low temperature process steps, integrated circuits can be manufactured on plastic substrate for flexible electronics. It is even possible to stack these SG-TFTs on top of each other, making 3-dimensional chips. With the possibility to use the SG-TFTs in digital, analog and RF circuits, we can expect highly integrated circuits for mixed signals applications as well. As for the E-Paper segment, the combination of Quick-Response Liquid Powder Display and the SG-TFT technology, will offer promising applications in the near future, giving new dimension to high integration.

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