An Analysis of Internal Parameter Variations Effects on Nanoscaled Gates

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***Abstract*—The predicted deterioration of the component quality, due to the shrinking of components to near atomic scale, threatens the effectiveness and the applicability of conventional digital system design methodologies in the giga and tera-scale integration era. Three aggression sources support the previous statement: i) the increasing device parameter variability induced by the extreme reduction of the critical feature sizes and the intrinsic nature of new devices; ii) the intense and practically unpredictable internal noise; and iii) the large number of physical defects. This paper provides a detailed analysis of the noise and parameter variations effects on a basic processing gate. We derive formulas to calculate the expected value and the variance of the gate output under the effects of noise, threshold, and gain fluctuations. Using these expressions we also derive a cost-performance equation that evaluates the gate error probability from its parameter variability, noise, power, and area or redundance. The proposed model is generic for any computing gate in the current digital paradigm. To illustrate the model applicability we calculate the error probability curve for a 90 nm CMOS inverter showing that for this technology the noise is the main limiting factor. A tradeoff analysis of area-power-redundancy-reliability for nanogates is performed indicating that the use of nanoscale individual elements for fabricating gates in deep-nanoscale technologies may not be a viable option. The results clearly suggest that the use of redundant structures is necessary and that averaging structures with mid-high redundancy factors may constitute a reasonable solution for building reliable nanoscale gates.**

***Index Terms*—Fault tolerance, logic design, nanotechnology, nonlinear functions.**

I. Introduction

THE ADVANCE of the electronic fabrication technology is pushing the device dimensions near to the atomic scale. Scaled MOS devices are expected to shrink until dimensions below 10 nm [1], [2] and emerging technologies promise an even further reduction to 1–2 nm [2] using devices based on single electron tunneling (SET) [3], quantum effects, carbon nanotubes [4], [5], or molecules [6]. The reduction of device dimensions in that range promises more than three orders of magnitude increase in the integration density and, accordingly, an increase of system performance and functionality. However, it is also expected a dramatic reduction with several orders of magnitude of the device quality and, in general, of the circuit reliability [2], [7].

As device dimensions shrink down, the characteristics of individual atoms become relevant. The addition or substraction of an atom layer [8] or the actual atom positions, instead of the probabilistic distribution of thousands of them, determine the device's behavior increasing its parameter variability [9]. Nowadays, for technologies just below 100 nm, the variability of MOS devices is already a concern and a cause of yield reduction [10]. Besides, the device density increase forces the reduction of the power supply levels to keep the dissipated energy below the material limit (i.e., 100 W/cm^2 for silicon [11], [12]). Consequently, the signal levels are reduced decreasing the noise margins and increasing the device's sensitivity to noise which may eventually limit Moore's law [13]. On the top of these physical phenomena, the dimension reduction makes the fabrication process more complex increasing the number of defects and further decreasing the yield. All these effects might be reduced by improving the techniques to manipulate and control the matter at the nanoscale. However, controlling the fabrication process at the atomic scale is going to be probably unaffordable due to time and economic reasons. Therefore, a great effort is done in finding fabrication techniques based on alternative methods [2] such as self-assembling materials. These methods are inexpensive and fast, but their error rate is higher than the one corresponding to imprint or mask based techniques [6].

The large decrease of device reliability creates a new design environment where design paradigms able to alleviate this problem are necessary. The problem is similar to what first computer designers faced. In fact, John von Neumann works on *NAND multiplexing* and *majority voting cells* [14] have become a principal reference in this area and have guided the design of most fault-tolerant systems. Other fault-tolerant techniques are using reconfiguration to overcome defects [15] or encoding strategies to detect and correct errors produced by data faults [16], [17]. All these techniques have been revisited looking for architectural solutions for nanocomputing [7], [18]–[23]. In general, these architectures fall into two categories either von Neumann based or reconfiguration based. Designs based on von Neumann's ideas highly increase the complexity of the circuits, but protect the system against transient faults and defects. Systems based on reconfiguration use regular grids of identical elements simplifying the fabrication, but can only protect the systems against static defects. Both alternatives require a minimum reliability for the individual gates in order to be able to provide a reliable system, which may not be attainable in emerging nanotechnologies. Thus, to evaluate the feasibility of these architectures it is first necessary to evaluate

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the error probability of the fabricated gates. This requires the identification of the fluctuation sources and the defect sources on the devices and the construction of statistical models capable of describing their effects on the device response. Using these models it is possible to predict the gate error probability considering not only the common fabrication defects but also the more subtle effects of noise and parameter variations.

The goal of this paper is the construction of a simple model able to evaluate the impact of gate internal parameter variations and noise on the gate reliability. In this line of reasoning, we first demonstrate how the variation of each individual parameter modifies the gate response. Then, we develop a global model which is considering the effects of these parameters all together. This global model allows us to evaluate the reliability of the gate when all its internal parameters fluctuate and to determine the main causes of reliability degradation. The proposed model is up to a certain point technology independent as it mostly covers the basic characteristics of a computing gate operating according to the digital paradigm and not the detailed features of any given technology. This approach permits its easy adaptation to any computing gate independently of the manufacturing technology. To illustrate the applicability and versatility of our model we calculate the error probability for a 90 nm CMOS inverter as a function of the noise-power supply voltage ratio and the fluctuations of its physical parameters. Our results indicate that noise is probably the main limiting factor for this technology, as also indicated in [13] and [24]. The proposed model also constitutes a performance-cost expression, which indicates how the system reliability (i.e., gate error probability) can be improved by means of increasing the power consumption and/or area cost. Finally, using this expression we evaluate the potential reliability of deep nanoscale gates. The results indicate that the use of single nanoscale basic building blocks cannot be a practical solution for systems with large variability. They clearly suggest that the utilization of basic cells with redundant organization is more appropriate and that structures based on averaging a set of elements [23], [25], [26] can be one of the simplest solutions for building nanogates with a certain required reliability.

The paper is organized as follows: Section II presents the basic gate functional model and its main parameters. In Section III the statistical description of the model is presented. The cost-performance function is derived in Section IV discussing its applicability and showing how the model can be applied to current CMOS technology. The section also indicates how power, area, and redundancy can be used to reduce the gate error probability. Section V argues why the averaging cell structure is a good candidate for building gates in deep nanoscale technologies and that such an approach may constitute a first tolerant layer to build reliable nanoelectronic systems. Finally, Section VI presents the conclusions.

II. Basic Gate Transfer Function

In order to be utilizable in the realization of practical data processing systems, computing gates should comply with four requirements [27] as follows: i) a nonlinear transfer function is necessary to provide noise immunity; ii) power gain is necessary to restitute the working signal levels; iii) gate chaining must be possible to allow for the implementation of complex functions; and iv) the gates must be able to implement a complete logic set. From the functional point of view, all these requirements may be summarized by a nonlinear function with two stable regions and a transition region with a gain greater than one, as depicted in Fig. 1. We use a simple model for this basic gate described mathematically as

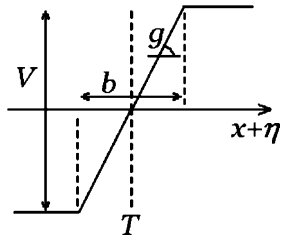

Fig. 1. Elementary gate model.

$$y = h(x) = \begin{cases} V/2 & x+\eta > T + V/2g \\ g(x+\eta-T) & \text{otherwise} \\ -V/2 & x+\eta < T - V/2g \end{cases} \quad (1)$$

which is a nonlinear piecewise function defining two stable states separated by a distance V (i.e., the supply voltage) with a linear section connecting these states. The linear section is determined by the gate gain g, which must be greater than one in order to restitute the output levels. This gain along with V determines the extension of the transition region ($b = V/g$). The switching point is defined by the gate threshold T that defines the input voltage at which the gate output is half the supply voltage. Finally, the internal noise of the gate is given by η. Such a simple model covers the gate behavior and has the advantage that it reduces the characterization to a simple voltage–voltage measurement. In Section IV-A we discuss in more detail the application restrictions imposed by this simple model.

III. Analysis of the Effects of Variations

In this section we analyze how the gate output in (1) is affected by the variation of the gate parameters. As already mentioned, we focus this work on the functional internal gate parameters (i.e., internal noise, threshold, and gain). We use these three parameters because they allow us to link the gate functional response to the gate physical characteristics. They depend on the gate physical implementation characteristics such as material properties, process parameters, gate dimensions and structure, and working temperature. Hence, by analyzing how these three parameters affect the gate response we can evaluate how the fluctuations of all physical parameters affect the gate behavior.

For simplicity we assume that dynamic fluctuations in transients are properly avoided by setting a proper clocking scheme. Therefore, we consider a static model to analyze the response of the gate once the stable state is reached. This allows us to base the analysis on simple statistical information. We are interested in characterizing the gate response from a designer point of view. Thus, we are interested to characterize the mean gate transfer function and the deviations from this mean response. From statistics it is easy to see that the output expected value and variance conditioned to the input value provide this information [28]. We can calculate the output expected value conditioned to

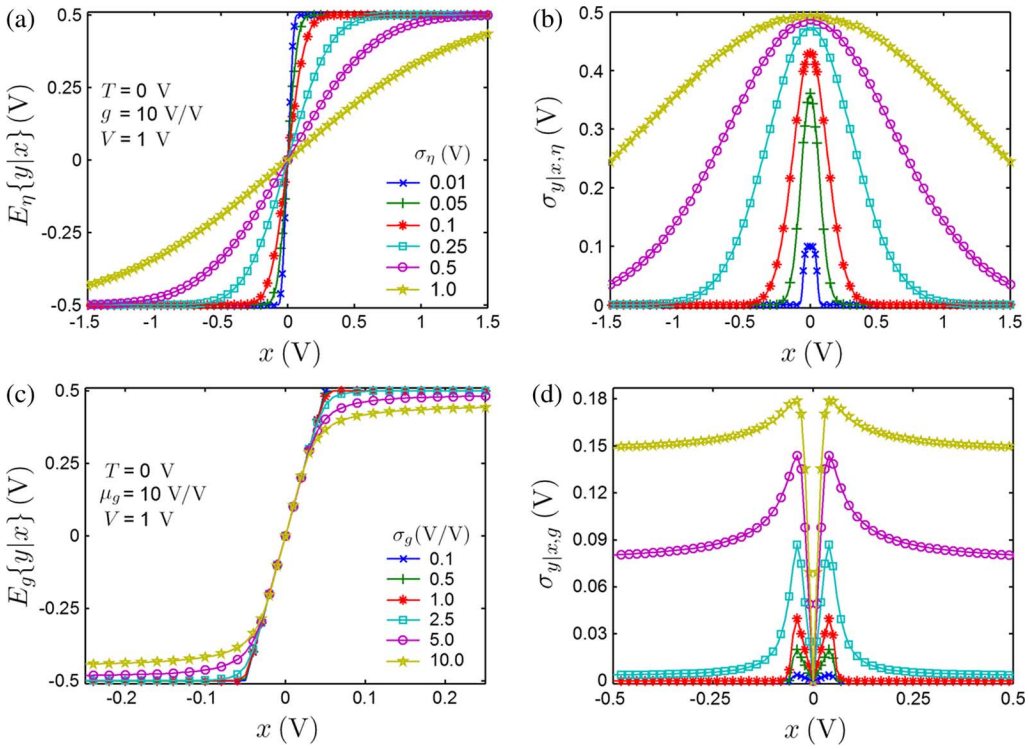

Fig. 2. Gate output expected value and standard deviation due to variations of (a), (c) internal noise (and threshold) and (b), (d) gain fluctuations for gates with $\mu_g = 10, \mu_T = 0$ V and $V = 1$ V. Symbols: simulated data; lines: model predictions.

the input x due to parameter u, $E_u\{y|x\}$, and the output variance conditioned to the input x due to parameter u, $\sigma^2_{y|x,u}$, by integrating the following expressions:

$$E_u\{y|x\} = \int_u h(x) f_u(u) du, \tag{2}$$

$$\sigma^2_{y|x,u} = \int_u h^2(x) f_u(u) du - E^2\{y|x\} \tag{3}$$

where $f_u(u)$ is the probability density function (pdf) of the random variable u, which is a generic variable indicating any of the random variables of interest. As previously discussed, the three parameters we are analyzing are dependent on several uncorrelated physical effects. Based on this fact and considering the central limit theorem [28] we assume that the gate parameters are normally distributed variables characterized by a mean μ_u and a standard deviation σ_u.

The expressions obtained in the analysis presented in the remainder of the section are validated by simulating the gate response with random parameters. The simulation calculates random values for each considered parameter and simulates the gate static response. After sufficient iterations are performed (more than 1 000 000), the output expected value and variance are calculated for each input value. These values are used as a reference for checking the proposed model.

A. Noise Fluctuations

Noise is one of the major sources of fluctuations in electronic design. Engineers have been fighting against it since the beginning of electronics. In fact, the digital technology was adopted in part because it permits to build systems with a very high noise tolerance. However, as signal levels are reduced the relative noise amplitudes grow and noise margin becomes insufficient. In this section we analyze how noise modifies the gate functionality. Solving the integrals in (2) and (3) for η we obtain the following exact analytical expressions (a detailed derivation is presented in [29]):

$$\begin{aligned} E_\eta\{y|x\} = {} & \frac{1}{2} g(x-T)\left(\operatorname{erf}(A_H) - \operatorname{erf}(A_L)\right) \\ & - \frac{V}{4}\left(\operatorname{erf}(A_H) + \operatorname{erf}(A_L)\right) \\ & - g\sigma_\eta \left(\frac{e^{-A_H^2} - e^{-A_L^2}}{\sqrt{2\pi}}\right), \end{aligned} \tag{4}$$

$$\begin{aligned} \sigma^2_{y|x,\eta} = {} & \frac{V^2}{4} - 2g^2\sigma_\eta(x-T)\left(\frac{e^{-A_H^2} - e^{-A_L^2}}{\sqrt{2\pi}}\right) \\ & + \left(-\frac{V^2}{8} + \frac{g^2\sigma_\eta^2}{2} + \frac{g^2}{2}(x-T)^2\right) \\ & \times \left(\operatorname{erf}(A_H) - \operatorname{erf}(A_L)\right) \\ & - g^2\sigma_\eta^2\left(\frac{A_H e^{-A_H^2} - A_L e^{-A_L^2}}{\sqrt{\pi}}\right) \\ & - E^2_\eta\{y|x\} \end{aligned} \tag{5}$$

where erf stands for the error function and

$$A_H = \frac{T + b/2 - x}{\sigma_\eta\sqrt{2}} \quad \text{and} \quad A_L = \frac{T - b/2 - x}{\sigma_\eta\sqrt{2}}. \tag{6}$$

Fig. 2(a) and 2(b) presents the expected value and standard deviation (variance square root) calculated from simulated data and the model predictions for a gate with $g = 10$, $T = 0$ V, and $V = 1$ V for several values of

$\sigma_\eta = 0.01,\ 0.05,\ 0.1,\ 0.25,\ 0.5,$ and 1.0 V. As expected, the model predict the noise effects, but the expressions in (4) and (5) are complex and it is not easy to observe the noise effects. From Fig. 2(a) and 2(b) we note that the noise effects are more pronounced around the switching point were $|x - T| \simeq 0$. To make the noise effects on the gate functionality more visible, we can simplify (4) and (5), by considering that $|x - T| \ll \sigma_\eta$, as follows:

$$E_\eta\{y|x\} \simeq \frac{V}{\sigma_\eta\sqrt{2\pi}}(x - T), \tag{7}$$

$$\sigma^2_{y|x,\eta} \simeq \frac{V^2}{4} - \frac{1}{6}\frac{V^3}{g\sigma_\eta\sqrt{2\pi}} - \left(\frac{V}{\sigma_\eta\sqrt{2\pi}}\right)^2 (x - T)^2. \tag{8}$$

From (7) and (8) (the simplified model) we can easily observe how noise affects the gate response. One of the most relevant effects is the reduction of the effective gain in the input-output relation ($V/\sigma_\eta\sqrt{2\pi}$ instead of g). This indicates that larger input signal levels are required to reach the stable states. It is also interesting to note that due to the nonlinear nature of the system the variance is not constant. It decreases as the input signal separates from the threshold value (switching point). Finally, the maximum variance is reduced by the factor $V^3/6g\sigma_\eta\sqrt{2\pi}$, which means that the maximum variance increases with increasing gain values.

We note here that the simplified models presented in this subsection and in the remainder of the section are only included to highlight the effects of each parameter fluctuations. They are not intended to be used for any calculation as the validity range of their assumptions does not cover the intended application range.

B. Threshold Variations

The switching level of a gate is defined by the threshold parameter. This parameter indicates the input level at which the gate output is at half the supply voltage range (for symmetric supply voltages this is zero). Small variations on this parameter unbalance the gate. Fluctuations larger than the input levels prevent the gate from switching between its stable states producing a permanent malfunction. The exact solution of the integrals in (2) and (3) for T (see [29] for details) is

$$\begin{aligned} E_T\{y|x\} =& \frac{1}{2}g(x - \mu_T)\left(\mathrm{erf}(B_H) - \mathrm{erf}(B_L)\right) \\ &+ \frac{V}{4}\left(\mathrm{erf}(B_H) + \mathrm{erf}(B_L)\right) \\ &+ g\frac{\sigma_T}{\sqrt{2\pi}}\left(e^{B_H^2} - e^{B_L^2}\right), \end{aligned} \tag{9}$$

$$\begin{aligned} \sigma^2_{y|x,T} =& \frac{V^2}{4} - 2g^2\sigma_T(x - \mu_T)\left(\frac{e^{B_H^2} - e^{B_L^2}}{\sqrt{2\pi}}\right) \\ &+ \left(-\frac{V^2}{8} + \frac{g^2\sigma_T^2}{2} + \frac{g^2}{2}(x - \mu_T)^2\right) \\ &\times \left(\mathrm{erf}(B_H) - \mathrm{erf}(B_L)\right) \\ &- g^2\sigma_T^2\left(\frac{B_H e^{B_H^2} - B_L e^{B_L^2}}{\sqrt{\pi}}\right) \\ &- E_T^2\{y|x\}, \end{aligned} \tag{10}$$

where

$$B_H = \frac{x - \mu_T + b/2}{\sigma_T\sqrt{2}} \quad \text{and} \quad B_L = \frac{x - \mu_T - b/2}{\sigma_T\sqrt{2}}. \tag{11}$$

The analysis for T is similar with those for η yielding the same results as in Fig. 2(a) and 2(b). Furthermore, the simplified expressions for T are similar with (7) and (8), but parameters σ_η and T become σ_T and μ_T, respectively. Therefore, threshold and noise effects are equivalent: reduction of the gate gain and a nonconstant variance. It should be noted that, unlike noise effects, the effects of threshold fluctuations are permanent being a cause of defects while noise varies along time producing transient faults. Furthermore, time filtering does not reduce threshold fluctuations effects. Therefore, it is important to keep threshold variations as small as possible.

C. Gain Variations

Gate gain determines the gate signal restitution capability. A large gain allows digital gates to keep the working levels close to the supply voltage levels. This parameter also defines the nonlinearity degree of the gate response determining the noise margin. According to digital design rules, gates with gains below one are considered defective as the signal levels degrade by passing through each gate and complex circuits cannot be built with them. In our gate model, we consider a positive gain. If a gate has a negative gain we consider it unable to operate and its output is kept constant at 0 V (at half the gate output range). Emerging nanotechnologies are expected to produce gates with low gains, which due to parameter variation may produce gates with gain below one. Therefore, the effect of such defective gates should be analyzed. To derive the model for gain variations we solve the integrals in (2) and (3) for the g parameter [29] and we obtain the following exact solutions:

$$\begin{aligned} E_g\{y|x\} =& \,\mathrm{sgn}\{x - T\}\frac{V}{4}\left(1 - \mathrm{erf}\left(\frac{|K| - \mu_g}{\sigma_g\sqrt{2}}\right)\right) \\ &- \frac{\sigma_g}{\sqrt{2\pi}}(x - T)\left(e^{-\frac{(|K| - \mu_g)^2}{2\sigma_g^2}} - e^{-\frac{\mu_g^2}{2\sigma_g^2}}\right) \\ &+ \frac{\mu_g}{2}(x - T) \\ &\times \left(\mathrm{erf}\left(\frac{|K| - \mu_g}{\sigma_g\sqrt{2}}\right) + \mathrm{erf}\left(\frac{\mu_g}{\sigma_g\sqrt{2}}\right)\right), \end{aligned} \tag{12}$$

$$\begin{aligned} \sigma^2_{y|x,g} =& \frac{V^2}{8}\left(1 - \mathrm{erf}\left(\frac{|K| - \mu_g}{\sigma_g\sqrt{2}}\right)\right) \\ &+ \frac{\sigma_g^2 + \mu_g^2}{2}(x - T)^2 \\ &\times \left(\mathrm{erf}\left(\frac{|K| - \mu_g}{\sigma_g\sqrt{2}}\right) + \mathrm{erf}\left(\frac{\mu_g}{\sigma_g\sqrt{2}}\right)\right) \\ &- \frac{\sigma_g}{\sqrt{2\pi}}\mu_g(x - T)^2\left(e^{-\frac{(|K| - \mu_g)^2}{2\sigma_g^2}} - e^{-\frac{\mu_g^2}{2\sigma_g^2}}\right) \\ &- \frac{\sigma_g}{\sqrt{2\pi}}|K|(x - T)^2 e^{-\frac{(|K| - \mu_g)^2}{2\sigma_g^2}} \\ &- E_g^2\{y|x\} \end{aligned} \tag{13}$$

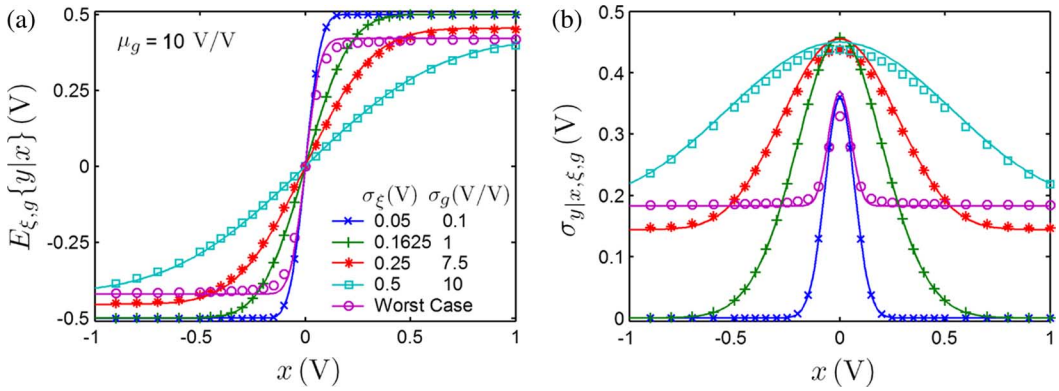

Fig. 3. (a) Gate output expected value and (b) standard deviation for gates with $\mu_g = 10$, $\mu_T = 0$ V, and $V = 1$ V under the action of gain and ξ (internal noise and threshold) fluctuations. Symbols: simulated data; lines: model prediction.

where $K = V/2(x - T)$ and sgn stands for the signum function. The output expected value and standard deviation from simulated data and model predictions for gates with $\mu_g = 10$ V/V, $T = 0$ V, and $V = 1$ V for $\sigma_g = 0.1$, 0.5, 1.0, 2.5, 5.0, and 10.0 V/V are presented in Fig. 2(c) and 2(d). As before, these expressions are too complex to clearly observe the effects of gain fluctuations. From the figures we can see that gain effects are more relevant for $|x - T| \gg 0$. Therefore, to simplify (12) and (13) we consider their limit expressions at $|x - T| \to \infty$ resulting in

$$E_g\{y|x\} \simeq \begin{cases} L_{E_g} & x > L_{E_g}/\mu_g + T \\ \mu_g(x - T) & \text{otherwise} \\ -L_{E_g} & x < -L_{E_g}/\mu_g + T \end{cases} \tag{14}$$

where

$$L_{E_g} = \frac{V}{4}\left(1 + \text{erf}\left(\frac{\mu_g}{\sigma_g\sqrt{2}}\right)\right) \tag{15}$$

and

$$\sigma^2_{y|x,g} \simeq \frac{V^2}{16}\left(1 - \text{erf}^2\left(\frac{\mu_g}{\sigma_g\sqrt{2}}\right)\right). \tag{16}$$

From (14) and (16) it is possible to observe the effect of gain fluctuations. For ratios $\mu_g/\sigma_g \gg 1$, the fluctuations of g do not modify the gate response ($L_{E_g} \simeq V/2$ and $\sigma^2_{y|x,g} \simeq 0$). This situation changes when $\mu_g/\sigma_g < 4$ (i.e., defective elements are present). Nonfunctional elements ($g < 1$) reduce the effective separation between the stable levels (down to $V/2$) and increase the variance for large values of $|x - T|$ up to $V^2/16$. For values $|x - T| \approx 0$ the expected gain is equal to μ_g independently of the amount of variation on g. Thus, g variations do not significantly affect the transition region behavior.

D. Global Analysis

Once the effects of each parameter variation are identified we can model the gate response when all three parameters vary. The exact analytical model requires solving integrals in (2) and (3) for all three parameters converting them into triple integrals with no analytical solution. Therefore, to model the global response we use a different approach. First, by observing (1) we see that it is possible to define a new random variable $\xi = \eta - T$ with $\mu_\xi = -\mu_T$ and $\sigma^2_\xi = \sigma^2_\eta + \sigma^2_T$, which produces the same effects as the parameters η and T together. Second, by observing the gate output expected value and standard deviation for the three parameters (Fig. 2) we can see that the gate effective gain depends on η and T. Parameter g determines the separation between the stable levels and produces an offset on all the standard deviation curves. From these observations, we assume that it is possible to separate the effects of both random variables as follows: i) by solving (2) and (3) for parameter ξ we calculate the effects of η and T; and ii) by substituting the fixed supply voltage V in the resulting expressions with an expression dependent on g, namely V_G, and by adding the value σ^2_G to the variance equation. Based on this strategy we can express the gate output expected value and the variance due to both parameters, ξ and g, as follows [29]:

TABLE I
POINT AVERAGE ROOT MEAN SQUARE ERROR (E_{aRMSE}) AND MAXIMUM ERROR (E_{MAX}) NORMALIZED BY THE CURVE RANGE ($\max - \min$) IN % BETWEEN SIMULATED AND MODEL DATA WHEN ξ AND g VARY

$E_{\xi,g}\{y_i\|x\}$	$\mu_g = 5$	$\mu_g = 10$	$\mu_g = 50$
E_{aRMSE}	0.140	0.071	0.022
E_{MAX}	1.952	0.994	0.228
$\sigma^2_{y_i\|x,\xi,g}$	$\mu_g = 5$	$\mu_g = 10$	$\mu_g = 50$
E_{aRMSE}	0.613	0.388	0.160
E_{MAX}	15.862	9.712	3.407

$$\begin{aligned} E_{\xi,g}\{y|x\} = {} & \frac{1}{2}g(x - \mu_T)\left(\text{erf}(C_H) - \text{erf}(C_L)\right) \\ & - \frac{V_G}{4}\left(\text{erf}(C_H) + \text{erf}(C_L)\right) \\ & - g\frac{\sigma_\xi}{\sqrt{2\pi}}\left(e^{-C_H^2} - e^{-C_L^2}\right), \end{aligned} \tag{17}$$

$$\begin{aligned} \sigma^2_{y|x,\xi,g} = {} & \frac{V_G^2}{4} - \frac{V_G^2}{8}\left[\text{erf}(C_H) - \text{erf}(C_L)\right] \\ & + \frac{1}{2}g^2(x - \mu_T)^2\left[\text{erf}(C_H) - \text{erf}(C_L)\right] \\ & - 2g^2(x - \mu_T)\frac{\sigma_\xi}{\sqrt{2\pi}}\left[e^{-C_H^2} - e^{-C_L^2}\right] \\ & - g^2\frac{\sigma_\xi^2}{\sqrt{\pi}}\left[C_H e^{-C_H^2} - C_L e^{-C_L^2}\right. \\ & \left. - \frac{\sqrt{\pi}}{2}\left(\text{erf}(C_H) - \text{erf}(C_L)\right)\right] \\ & - E^2_{\xi,g}\{y|x\} + \sigma^2_G \end{aligned} \tag{18}$$

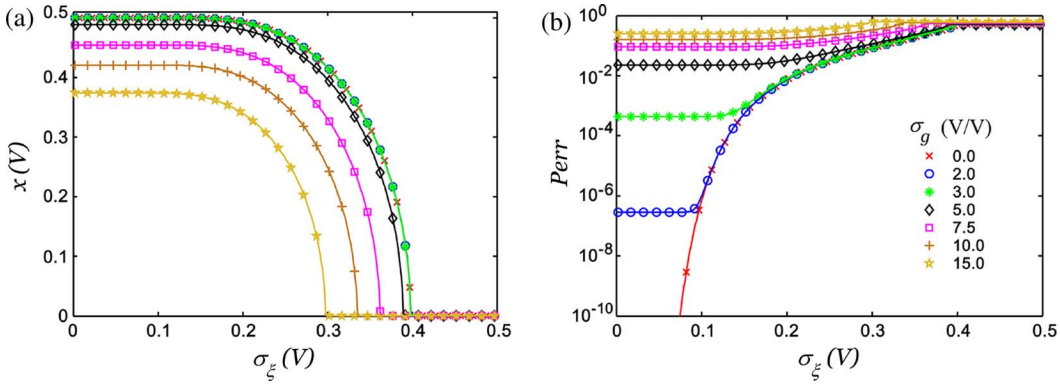

Fig. 4. Results for gates with $\mu_g = 10$, $\mu_T = 0$ V, and $V = 1$ V with fluctuations of their internal parameters. (a) Asymptotic high state signal level, x_h. (b) Upper bound for the gate error probability.

where

$$C_H = \frac{V_G/2g - (x - \mu_T)}{\sigma_\xi \sqrt{2}} \text{ and } C_L = \frac{-V_G/2g - (x - \mu_T)}{\sigma_\eta \sqrt{2}}. \tag{19}$$

The expressions to approximate V_G and σ_G determine the accuracy of this model. These expressions can be obtained by intuition and successive trial and error attempts. In this paper, we use the simplest approximation, which consist in a constant value calculated from (12) and (13) at the limit $|x - \mu_T| \to \infty$. This approach provides the following values:

$$V_G \simeq \frac{V}{2}\left(1 + \text{erf}\left(\frac{\mu_g}{\sigma_g\sqrt{2}}\right)\right), \tag{20}$$

$$\sigma_G^2 \simeq \frac{V^2}{16}\left(1 - \text{erf}^2\left(\frac{\mu_g}{\sigma_g\sqrt{2}}\right)\right). \tag{21}$$

This approximation has an acceptable accuracy as Fig. 3 suggests for the reference gate setup ($\mu_g = 10$, $\mu_T = 0$ V and $V = 1$ V). The output expected value and the standard deviation calculated from simulated data and the model predictions are presented showing good agreement. Table I presents the point average root mean square error (E_{aRMSE}) and the point maximum error (E_{MAX}) normalized by the curve range. The table presents the errors for three mean gate gains ($\mu_g = 5$, 10, and 50) showing that the model increases its accuracy as the mean gain increases. For mean gains above 10–20 V/V this approximation constitutes a good model. If gates with lower μ_g need to be analyzed other approximations for the V_G and σ_G values must be considered as discussed in [29].

IV. Gate Error Probability

We analyze the static response of the gates assuming that any transient state is finished before the data are evaluated (i.e., the clock period is larger than the propagation time of the gates). Therefore, we define the error probability as the probability of having an output value lower or higher than μ_T at the moment the information is evaluated for a high or low output, respectively. This probability depends on the effective separation between the stable levels, which depends on the parameter fluctuations and noise. Thus, it is necessary to estimate the signal working levels inside the circuits. To calculate them we define an infinitely long chain of gates and determine their asymptotic values. Fig. 4(a) presents how the high state voltage level evolves with increasing fluctuations of the main parameters. The low state voltage level follows a symmetrical trajectory around the axis defined by μ_T. The plot indicates that the working levels are stable up to $\sigma_\xi/V \simeq 0.2$. As this ratio increases, the asymptotic signal working levels are reduced due to the smoothing effect until it is not possible to distinguish between the two levels. The reduction due to gain fluctuations is not important until $\sigma_g/\mu_g > 0.25$.

Using the model from Section III-D and the asymptotic signal working levels we can evaluate the gate error probability when its internal parameters fluctuate. However, the model does not provide any information about the gate output pdf. Analyzing the simulated data we found that the output pdf has three delta functions, at the high and low output values and at μ_T, and a lower continuous function for the other output values. We can approximate this pdf by a trinomial distribution disregarding the continuous probability function. We tested this approximation by comparing its results with simulated data and we found that it provides a good upper bound for the gate error probability [29]. This approach yields better results than general bounds, such as Chebyshev's inequality [28], which are valid for any pdf, but provide upper bounds, which are too large in most cases of interest. Fig. 4(b) shows the evolution of the gate error probability for a gate with $\mu_g = 10$, $\mu_T = 0$ V, and $V = 1$ V, when its three parameters vary. Gain variations determine the minimum gate error probability as it imposes a probability of having nonfunctional gates. Threshold and noise fluctuations determine the minimum supply voltage as the gate is not able to operate for ratios $\sigma_\xi/V > 0.4$, where high and low states are equiprobable.

A. Model Application

In the previous sections we introduced a model to study the effects of fluctuation sources on the gate reliability. We based all the derivation on two assumptions: i) the gates can be modeled by the piecewise transfer function in Fig. 1 and ii) the parameters can be modeled as independent Gaussian distributed random variables (η, T, and g). The first assumption is based on the fact that any computing gate in the digital paradigm must have certain characteristics summarized by the piecewise model. Therefore, the transfer function is generic for the current computing paradigm. The second assumption is not fundamental and responds to a need for simplification. Thus, it is necessary to test

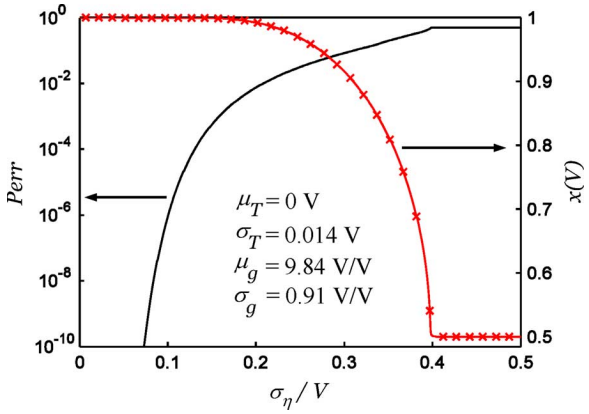

Fig. 5. Output error probability and average output levels for a 90 nm CMOS inverter.

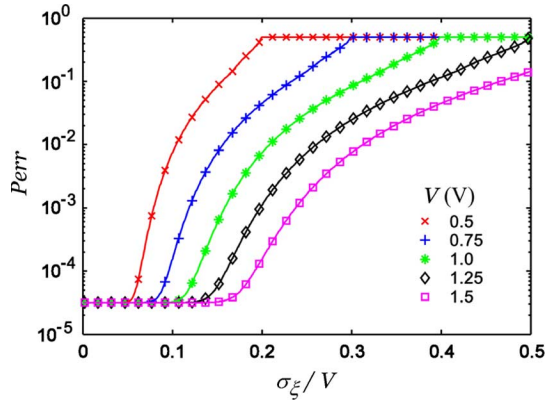

Fig. 6. Gate error probability in gates with $\mu_g = 10$ and $\sigma_g/\mu_g = 0.25$ for several power supply voltages $V = 0.5,\ 0.75,\ 1.0,\ 1.25$, and 1.5 V.

whether it is an acceptable assumption for each modeled gate. However, even if the assumption is not completely valid the model is still able to provide a rough estimation of the gate reliability which is its actual goal. This section presents the application of the proposed model to the evaluation of a 90 nm CMOS inverter. Before doing that we first demonstrate that assumptions i) and ii) are legitimate for such a technology.

The output of any CMOS gate can be usually approximated by the simple piecewise model, especially the inverter. In fact, most analysis use this simplified model to evaluate the CMOS gates noise margins [30]. Therefore, the first assumption is valid for the present example. To check the independence and normality of the gate parameters we utilized Monte Carlo simulations of an actual 90 nm CMOS inverter with minimum dimensions. Analyzing the corner models provided with the BSIM3 model we have estimated the 3σ deviations for the fluctuations of the channel length and width, the threshold voltages, and the channel doping concentrations, which we assume to be uncorrelated for the N and P transistors. The oxide thickness fluctuations are considered to be equal for both devices. Analyzing the resultant gate threshold and gain for 50 000 runs, we found that both parameters are normally distributed and practically uncorrelated ($\rho = 0.24$) [29]. Noise, internal or external, has several sources (up to ten different internal sources are identified in [31]). Their effects can be added together as an input or output voltage source [32]. Thus, independent Gaussian distributions are reasonable approximations for the fluctuation sources in the CMOS inverter.

The simulation results render the parameters to model T and g. Disregarding the small asymmetry of T and translating the parameters to our model we obtain $\mu_T = 0$ V, $\sigma_T = 0.014$ V, $\mu_g = 9.84$, and $\sigma_g = 0.91$. Using these data, Fig. 5 shows the error probability and the high level asymptotic output value for the 90 nm CMOS inverter as a function of the noise to power supply voltage ratio. In this example the noise source is valid to model any noise source in the circuit (internal or external). The error probability for $\sigma_\eta/V < 0.1$ is low enough to produce reliable gates. However, if this threshold is overcome due to supply voltage scaling the reliability of the gate is seriously reduced.

The gate error probability relationship constitutes a cost-performance function useful for circuit designers. This expression indicates how to trade off gate reliability by power (V) and area (which reduces σ_T and σ_g) cost depending on the gate characteristics. In the following subsections, we analyze the effect of increasing the power supply voltage, area, and redundancy on the reliability of nanoscale gates showing that for deep nanoscale devices redundancy is a better option than increasing the power or scaling up the devices.

B. Power Versus Reliability

The simplest way to reduce the effects of the gate fluctuation sources is to increase the separation between the high and low states by increasing the supply voltage (V). It increases the noise margin effectively reducing the error probability. Fig. 6 shows the gate error probability evolution when $\mu_g = 10$, $\sigma_g/\mu_g = 0.25$, and $V = 0.5,\ 0.75,\ 1.0,\ 1.25$, and 1.5 V. Focusing on our model, when V is increased the asymptotic working voltage levels increase, which allows the gate to withstand larger values of σ_ξ (reducing the effects of η and T). However, increasing V does not affect the gain fluctuations effects that determine the minimum error level. Therefore, increasing the supply voltage to reduce the gate error probability when the parameter variations are a concern might not be the best solution. The price to pay for this reliability improvement is a higher dissipated power per gate. Due to the material dissipation limit, it is not possible to arbitrarily raise V. In fact, nanotechnology gates need to operate with the lowest possible V to compensate the increase of the number of dissipating devices per unit area.

C. Area Versus Reliability

The variability in the gate parameters is directly related to the relative fluctuations on the gate physical parameters. Given a certain resolution and accuracy of the manufacturing processes, the larger the structure we want to build the lower the relative error. Therefore, if we increase the size of the building parts of a circuit the parameter variations decrease, and, obviously, the area cost increases. The effect of such a reliability increase measure in our gate model is the reduction of σ_T and σ_g. The precise relationship among the gate area and the parameter variations is dependent on the utilized fabrication technology and it is out of the scope of this work. The same effect is achieved for noise when we apply filters, σ_η decreases. Increasing the device size and filtering the signals undoubtedly improve the gate reliability

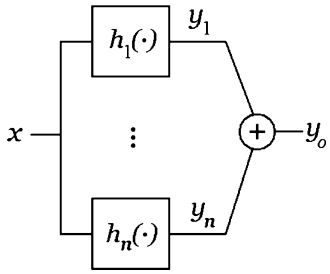

Fig. 7. Schematic structure of the averaging cell.

(see the curves in Fig. 4). However, it also reduces the performance achievable by the technology, increases the power dissipated per gate, and stops the technological evolution. Besides, unlike MOS devices, which response are maintained when their dimensions scale up, most nanoscale devices behavior depends on the implemented nanometric dimensions (e.g., carbon nanotubes, molecules, or SETs). For such devices, it is not possible to increase their sizes to increase the reliability. A possible solution to overcome this limitation is the use of averaging structures as discussed in the following subsection.

D. Redundancy Versus Reliability: The Averaging Cell

For nanoscale devices that cannot be scaled up the use of parallel configurations with averaging as depicted in Fig. 7 can provide an interesting redundant scheme. The basic structure is composed by n devices performing the same function. The gate output is produced by adding all the individual outputs together and each device contributes in an n^{th} part of the cell output. All the devices are built with the same technique, but independently from the rest. Consequently, their parameters are independent and identically distributed (iid). We can model the cell output, y_o, expected value and variance from the statistical information of the individual outputs, y_i, taking advantage of the fact that y_i are iid random variables. Then,

$$E\{y_o|x\} = \sum_{i=1}^{n} \frac{1}{n} E\{y_i|x\} = E\{y_i|x\}, \tag{22}$$

$$\sigma^2_{y_o|x} = \sum_{i=1}^{n} \frac{1}{n^2} \sigma^2_{y_i|x} = \frac{\sigma^2_{y_i|x}}{n} \tag{23}$$

where $E\{y_i|x\}$ and $\sigma^2_{y_i|x}$ are given by (17) and (18). From this description, we can see that the expression for the averaging cell expected value and for the single gate are equivalent, but the variance is reduced by a factor n. The error probability is calculated following the same procedure as for the single gate, but considering an n-trial trinomial distribution. Considering that trinomial distributions with large n approach the normal distribution, for large redundancy factors ($n > 50$) we simply use the Gaussian approximation for the output pdf using the parameters in (22) and (23) [29]. As the output expected values for the averaging structure and for the gate are equivalent, the asymptotic signal working levels are the same as those presented in Fig. 4(a).

Fig. 8 presents the error probability for the averaging structure with $n = 1$, 3, 5, 9, 15, 25, 50, and 100 parallel elements with $\mu_g = 10$, $\sigma_g/\mu_g = 0.5$, and $V = 1$ V. From the curves we observe that the limit of the cell reliability is still given by

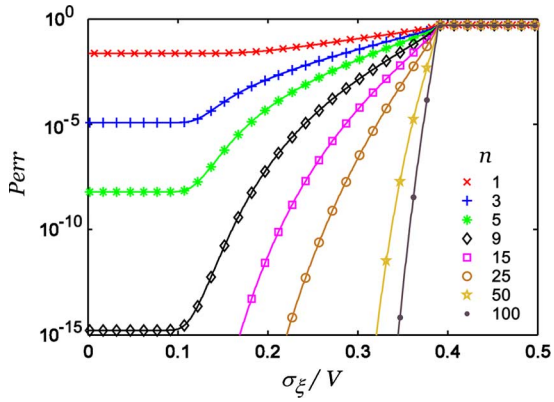

Fig. 8. Output error probability for an averaging cell with $n = 1, 3, 5, 9, 15, 25, 50$, and 100 $\mu_g = 10$, $\sigma_g/\mu_g = 0.5$, and $V = 1$ V.

the ratio σ_ξ/V, which can only be increased by increasing the supply voltage or by improving the device quality. However, the averaging of the redundant devices decreases the error probability on the valid region allowing the cell to operate reliably until its working limit. This suggests that by using redundancy factors in the range 50 to 500 it is possible to ensure a reliable gate behavior for devices with large fluctuations in the three considered parameters in the valid region. The cost of this technique is the increase of the total area and power dissipation per logic function. However, it allows the use of nanometric devices that would not be possible otherwise. Besides, as we can determine the number of nanodevices required in order to achieve a certain reliability, it might be possible to adjust the cost to optimal conditions for each design. Furthermore, the numerical values for the error probability in Fig. 8 indicate that this technique may provide a simple and competitive solution to tolerate the gate errors caused by the considered fluctuations sources, when compared to other fault-tolerant schemes [33].

V. Discussion

The expected reliability of nanodevices [2], [7] clearly indicates that tolerant gates or system structures are required in order to build reliable electronic systems. If reliability of the final systems cannot be assured it will not be possible to manufacture any electronic system based on nanotechnology. Hence, tolerant techniques such as reconfiguration or NAND multiplexing are expected to be fundamental. However, the error coverage and applicability of such techniques must be carefully analyzed. Reconfiguration only covers the static defects and requires the capability of testing and reconfiguring up to 10^{12} devices. NAND multiplexing covers all the errors without testing the devices, but requires highly complex structures that might be unfeasible to manufacture in nanotechnology [34].

The use of the averaging function to increase the reliability of gates may seem naive and nonoptimal. Nonetheless, such a structure is able to make use of devices that other techniques would discard as defective (e.g., devices with large opposed deviations of the threshold can compensate each other). Also, important to note is that this structure is potentially able to take advantage of undesired effects such as the interaction among the parallel elements to provide a more reliable cell [25], [26]. In any case, in the nanoscale, this simple technique represents a

feasible and competitive solution to tolerate faults caused by the fluctuation sources as Fig. 8 indicates. Furthermore, the structure is also able to tolerate manufacturing defects on the nanodevices as it converts each defective nanodevice in an output degradation of V/n. In [34] we present a possible implementation of this structure, which may be built using molecular devices self-assembled in nanopores as indicated in [35] or using carbon nanotubes in structures similar to those manufactured for implementing vias [4]. Such a structure allows the integration of 100 molecules in an area of approximately 78.5 nm^2 (considering molecules with diameter 1 nm). This means an integration density increase of 2400 when compared to a 65 nm CMOS inverter (0.19 μm^2) indicating that even when using large redundancy factors this technology is able to reach tera-scale integration densities. Obviously, the effects of correlated variation sources among the devices cannot be tolerated. For this reason the averaging cell is not intended as a global solution to the nanoscale reliability problem, but as a first protection layer with a low cost in manufacturing complexity and area for a hierarchical complete solution.

VI. Conclusion

We presented a statistical description of a generic computing gate functionality considering the variability of its internal parameters. The effects of noise, threshold, and gain fluctuations were identified and a model considering all of them was developed. This description provides a cost-performance expression relating the gate reliability with the power and area costs. It can be used to quickly estimate the reliability trade-offs for any technology based on the digital computing paradigm. As an application example the error probability for a 90 nm CMOS inverter as a function of the noise to power supply voltages has been calculated showing that noise is the principal limit for this technology reliability. Then, using the proposed model we have analyzed various reliability tradeoffs for nanotechnology gates. The results indicate that building gates out of single devices in deep-nanometric technologies may be unfeasible due to the large expected variability of its parameters. Finally, we proposed the use of averaging structures to build gates with an adjustable reliability. These gates may constitute a first layer of a set of hierarchical reliability enhancing techniques meant to potentially build practical electronic systems out of highly unreliable nanodevices.

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