Towards "Zero-energy" using NEMFET-based Power Management for 3D Hybrid Stacked ICs

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***Abstract*—In this paper we describe and evaluate a 3D hybrid power management architecture which makes use of Nano-Electro-Mechanical Field Effect Transistors (NEMFET) as power switches that cut-off the power supply of inactive blocks. 3D stacking combines the appealing extremely low leakage currents of the NEMFETs with the versatility of CMOS technology by allowing for the power switches to be fabricated on a separate die. This simplifies the power planning in general, allows for always-on blocks to also be implemented with NEMFETs, and can increase the computation platform performance because of extra area cleared by the switches. Moreover it leverages the integration of other NEMS/MEMS devices, e.g., energy harvesters, sensors, on the same layer with the power switches. To validate this proposal and evaluate its performance in a real-life scenario we perform a careful assessment of the implications of this hybrid power management architecture on the rest of the system. To this end we consider the 3D embodiment of an embedded openMSP430 processor based SoC platform running a bio-medical sensing application for heart rate detection and measure the effects of the 3D hybrid architecture on sensitive metrics used in power gating designs, e.g., delay degradation, power-up and power-down behavior, and overall energy consumption. Our experiments indicate that, due to the extreme low leakage current of the NEMFETs, the system idle energy is decreased by 2.74x at the expense of a 4x area overhead on the NEMS tier. Moreover, due to the 3D hybrid approach the energy-delay product of the embedded SoC platform is reduced by 9%, with a potential improvement of up to 60% for applications with lower activity, e.g., wireless sensor networks. Last but not least the 3D stacked architecture prevents clock period degradation issues, since the IR Drop is reduced with a factor of 4x. Based on our experiment we believe that such 3D hybrid NEMS/CMOS approach creates the premises for the substantial reduction of an increasingly important component of the total energy consumption, the leakage power while idle, thus it makes nanosystems meet the limited energy budget of local energy harvesters, and become potentially autonomous "zero-energy" devices.**

***Index Terms*—Low power electronics, Energy efficiency, Nanoelectromechanical systems, Through-silicon vias**

I. Introduction

Our future is evolving towards a world where ubiquitous nanosystems will add intelligence to almost every object that surrounds us (The Internet of Things) such that sensing and actuating functionalities will be "hidden" in the environment. These nanosystems will be context aware and able to interact wirelessly with people and with each other. To be able to fulfill their requirements they will have to work autonomously into a "zero-power" regime, based on their low-power consumption and energy scavenging from the environment. The "zero-power" characteristic in this context is defined as the unique system ability to feed itself with the energy existing in various dynamic environments and harvest various types of energy sources, e.g., solar, thermal, vibrations, electromagnetic, convert them in electrical power, and store it, thus operating without conventional batteries. To achieve that such nanosystems have to make use of efficient energy scavenging and conservation techniques as well as to effectively spend the energy during the calculation process and to save it when the system is inactive.

Heterogeneous System on Chip (SoC) designs tend to use coarse/fine-grained Power Shut-Off with many power domains to fit the limited energy budget provided by energy scavengers. In turn, the complexity of the Power Distribution Network (PDN) increases altogether with Power Supply Noise (PSN), i.e., the noise on the PDN. While energy conversion devices to increase the power density and conversion efficiency are developed, ultra low-power hybrid circuit design techniques can close up the gap between the limited scavenged energy and the power budget of general purpose programmable embedded systems.

In this paper we envision such a hybrid technology nanosystem and propose an approach that exploits potential 3D hybrid integration of Nano-Electro-Mechanical-Systems (NEMS) and CMOS circuitry to reduce the system energy requirements and increase the energy conversion and consumption efficiency. We base our proposal on recent developments in the field of 3D integration, which have suggested that NEMS 3D power gating technique [1] can be a viable candidate to address these issues.

While it is clear that 3D stacking has a number of advantages as follows: (i) it combines the appealing extremely low leakage currents of the NEMFETs with the versatility of CMOS technology by allowing for the power switches to be fabricated on a separate die; (ii) it simplifies the power planning in general, allows for always-on blocks to also be implemented with NEMFETs, and can increase the computation platform performance because of extra area cleared by the switches in the CMOS tier; and (iii) it leverages the integration of other NEMS/MEMS devices, e.g., energy harvesters, sensors, on the same layer with the power switches, its implications in practical real life designs are not well understood.

The main goal of this paper is to explore these implica-

tions of the ultra low-leakage, variation tolerant 3D hybrid NEMS-CMOS power management architecture and evaluate its performance and energy efficiency in a real-life scenario. To this end we consider the 3D embodiment of an embedded openMSP430 processor [2] based SoC platform running a bio-medical sensing application for heart rate detection [3] and measure the effects of the 3D hybrid architecture on sensitive metrics used in power gating designs, e.g., delay degradation, power-up and power-down behavior, and overall energy consumption.

Our experiments indicate that, due to the extreme low leakage current of the NEMFET, the system idle energy is decreased by 2.74x at the expense of a 4x area overhead on the NEMS tier. Moreover, due to the 3D hybrid approach the energy-delay product of the embedded SoC platform is reduced by 9%, with a potential improvement of up to 60% for applications with lower activity, e.g., wireless sensor networks. Last but not least the 3D stacked architecture prevents clock period degradation issues, since the IR Drop is reduced with a factor of 4x. Based on our experiment we believe that such 3D hybrid NEMS/CMOS creates the premises for the substantial reduction of an increasingly important component of the total energy consumption, the leakage power while idle, thus it makes nanosystems meet the limited energy budget of local energy harvesters, and become potentially autonomous "zero-energy" devices.

The remainder of the presentation is organized as follows: We first introduce the 3D hybrid power management architecture and the NEMS device utilized for the implementation of the sleep transistors in Section II. In Section III we present the evaluation methodology, the considered platform and application, describe in detail the performed delay and energy analysis, and present the obtained results. We conclude the paper with some final remarks in Section IV.

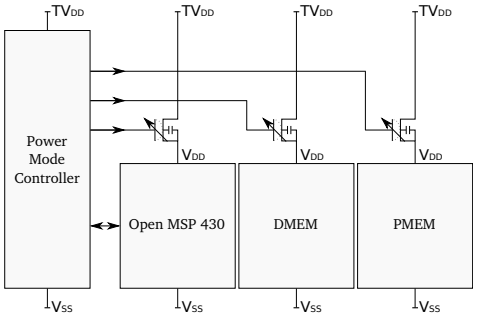

Figure 1 Power Shut Off Technique.

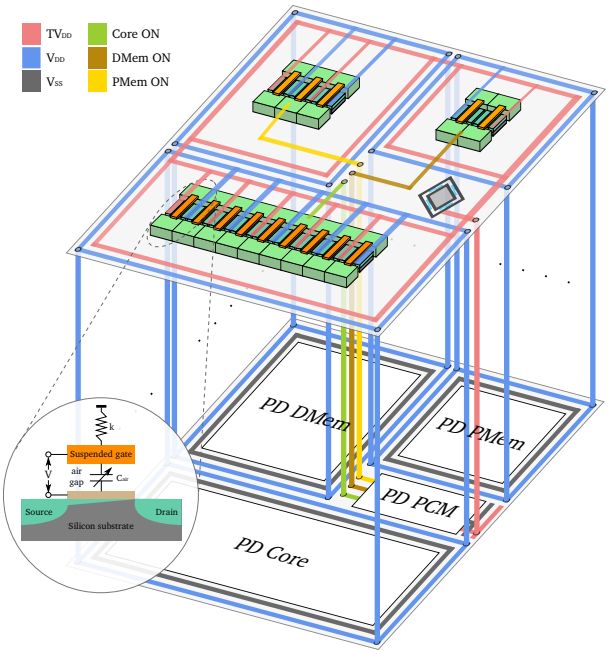

Figure 2 3D Stacked NEMFET Based Power Management Architecture.

II. Integrated 3D-stacked Hybrid Power Management

A straightforward and effective way to reduce the runtime power consumption of a certain application is to make use of a power shut-off technique (Power Gating) for inactive (sleeping) components of the computation platform. This can be done by placing a PMOS transistor between the supply rail and the circuit, as depicted in Figure 1, or an NMOS transistor between the subsystem and the ground rail.

Traditionally speaking those Sleep Transistors (ST) are High-V_t CMOS transistors but in [1] we recently proposed a novel 3D power management approach that makes use of NEMS as power switch transistors in CMOS power gated integrated circuits. The proposed architecture, relies on NEMS technology dies containing NEMFET STs placed between dies containing the actual power gated circuits. Figure 2 presents the two-tier stack used for the current evaluation. The bottom CMOS tier comprises the active logic circuit, while the top tier incorporates the NEMFET STs. By moving the bulky STs to a different die, precious area surrounding/inside the gated blocks previously allocated to them in the planar case can be reclaimed. Furthermore, signal interconnect length inside/between gated components is reduced, thereby potentially resulting in increased performance. "True" VDD (TV_{DD}) supply rings surrounding gated blocks are translated to the NEMS tier, thus more area is gained. The NEMS tier can also accommodate various NEMS sensors, e.g., temperature sensor for thermal monitoring in heat-sensitive multi-tiers stacks or vibration energy scavengers [4]. Energy scavengers can be placed directly near the power consumers, shortening the power supply rails and reducing the voltage drop and energy losses on them. Thermal sensors can monitor temperature and provide feedback information to the power controller. Moreover this approach can make use of the extreme low NEMFET leakage without requiring an expensive and currently not available NEMFET-CMOS hybrid fabrication technology.

The main drawback of the Power Shut-Off (PSO) technique is the reduction of the voltage across the power supply network (IR Drop) due to the switch transistor internal resistance. Instantaneous drop in power supply at the point of gate switching causes excessive delay which if not taken into consideration

can result in critical path delay violations. For example, it has been indicated in [5] that an 1% supply voltage decrease can cause approximately 4% degradation in gate delay in a 90 nm, 0.9 V technology.

While Nano-Electro-Mechanical Field Effect Transistor (NEMFET) has been proven to be a promising candidate to replace High-V_t transistors as power shut-off devices that cut-off the power supply [1], due to their extreme low leakage current, the behavior of the proposed 3D hybrid NEMS-IC power management architecture needs to be further investigated in order to evaluate its potential implication in real life applications.

A. The Suspended Gate FET

The Nano-Electro-Mechanical Field Effect Transistor (NEMFET) [6], with the cross-section depicted in the Figure 2 insert, has a movable gate suspended over the transistor's channel which results in the following outstanding device characteristics:

1) very abrupt switching due to the electromechanical instability (similar to a MEM switch) at a certain threshold gate voltage, called pull-in voltage,
2) ultra low "off" current (I_{OFF}), which makes it a very good candidate to replace traditional High-V_t FETs in power gated circuits.

A comparison between the "on" state resistance R_{ON} and the "off" state leakage current I_{OFF} of NEMFET, based on [7] and 65 nm High-V_t CMOS based Sleep Transistors (STs) is presented in Figure 3 for different area in terms of standard cells. The R_{ON} values are computed for an IR-drop of 10 mV over the ST, and the I_{OFF} values consider a 1.2 V power supply. In order to obtain a fully dynamic behavior of the NEMFET, based on the energy formulas determined in [8], we compute the switching energy for the optimal sized NEMFET power switches in terms of R_{ON} with respect to 1.2 V pull-in voltage. The preliminary energy consumed during power-up is approximated using Equation 1.

$$E(t) = V_S \int_0^t i(t')\mathrm{d}t' \approx E_0 + \frac{1}{2} C_{gap}(t) V_S(t)^2 \qquad (1)$$

where V_S is the source voltage, $i(t)$ the switching current, $C_{gap}(t)$ is the gap capacitance between the gate beam and the FET channel, and E_0 the energy loss while instantaneously charging $C_{gap}(0)$.

III. Performance Evaluation

Even though the NEMFET advantages at the device level are obvious, the evaluation of the actual impact of such a replacement on the overall energy consumption of an SoC with NEMFET based PSO, running a real life application, e.g., bio-medical sensing, is not straightforward. The validation of designs containing PSO requires additional considerations when compared with the normal timing closure sign-off flow. We note that the Energy-Delay Product (EDP) is the main figure of merit for the evaluation of a certain design for the envisaged application domain and this can briefly argued

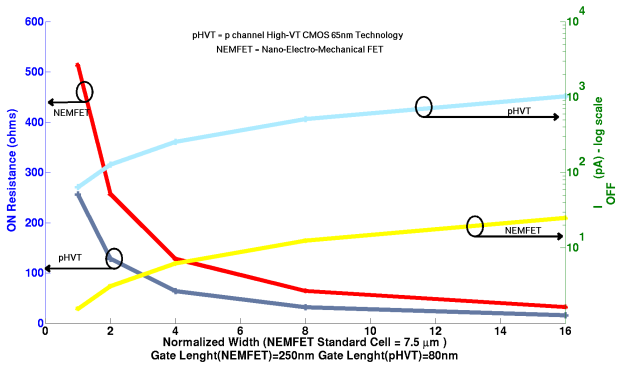

Figure 3 R_{ON} and I_{OFF} for NEMFET and 65 nm High-V_t CMOS Switch Transistors.

as follows. When evaluating the energy consumption of an application executing on a certain computing platform using a low power technique, two components are of importance:

1) The performance degradation (which has direct impact on active energy consumption) due to power shut-off circuit insertion, IR-Drop, and area overhead;
2) The leakage and the total energy savings due to sleep circuit insertion.

The figure of merit for low power applications that encompasses both of the above factors is the energy-delay product, which is the right trade-off metric for low energy systems, where every electron taken from a battery operated system is one too much. In the following subsections, the reference platform, the application, and the necessary steps required to determine the EDP are described in detail.

A. Reference Platform and Application

The considered experimental platform consists of a typical SoC for low power embedded devices, based on the open-source 16-bit synthesizable processor core openMSP430 [2], a clone of the commercial Texas Instruments MSP430 microcontroller. The program and data memory sizes are 4 kB and 2 kB, respectively. Although not used by the reference application, all the peripherals of the openMSP430 core (16-bit multiplier, timer, 6 8-bit input/output ports) are part of the platform in order to account for their leakage power.

The chosen application, a heart beat rate monitor, detects the QRS complex in an digitized electrocardiogram (ECG) signal. The QRS event corresponds to the depolarization of the ventricles, comprising a series of three deflections seen on a typical ECG signal. The middle one, i.e. the R wave, is the well-known "peak" of the ECG. The application program identifies the R peaks in the ECG signal and measures the interval between two consecutive R peaks. The algorithm we use is based on the open source arrhythmia detection software from EP Limited [3], which uses the filtering based Pan-Tomkins [9] method for R peak detection. For this method the input data are channeled through a five steps filtering process consisting of a low pass filter, a high pass filter, a derivative, an absolute value, and an integrator function, in this order. The

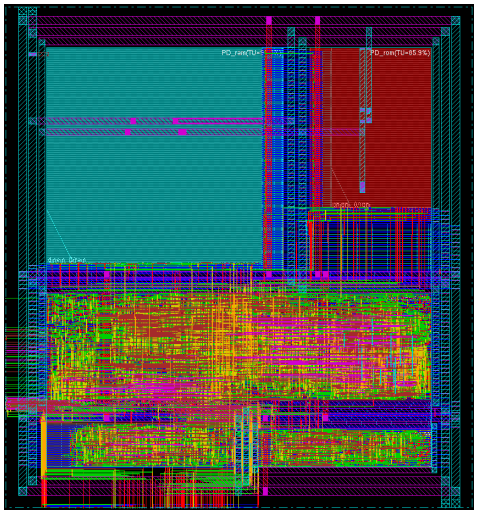

Figure 4 2D Layout of the CMOS tier design .

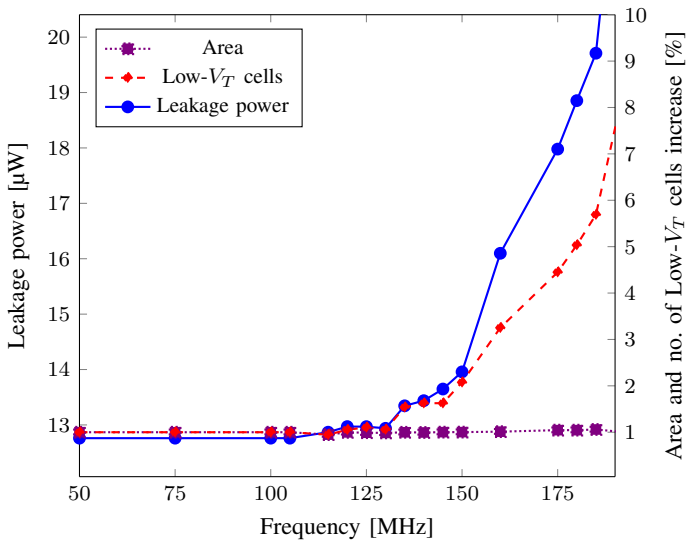

Figure 5 Leakage power versus synthesis frequency.

utilized filter equations are valid for an ECG sample frequency of 200 Hz.

The reference platform was implemented using Cadence Encounter Digital Implementation [10]in a 65 nm commercial Low Power CMOS technology with the signed-off layout depicted in Figure 4. A high operating frequency of the SoC means that it has to be synthesized with tighter timing constraints, which results in a design with faster and/or bigger cells. As a consequence leakage and dynamic power increase. For the presented SoC this effect has been evaluated by synthesizing the design for different target operating frequencies. Figure 5 presents the leakage power versus the synthesis frequency for the worst-case leakage corner: $V_{DD} = 1.32\,\text{V}$ and $T = 125\,°\text{C}$. Around 150 MHz a steep increase in leakage power can be observed. The leakage power mainly increases due to the increase of the number of Low-V_t elements. This figure suggests that the operating frequency can be increased up to 150 MHz without causing a significant increase in the leakage power. A similar trend was observed for dynamic power, thus we decided to synthesize our design for a target operating frequency of 150 MHz.

The hybrid NEMS-CMOS stack assumes a face-to-back bonding [11] with Through-Silicon-Vias (TSV) which can be easily extended to multiple tiers. The TSVs connects the two tiers power supply rings, as indicated in Figure 2. We used the RC-elements equivalent TSV model from [12], based on the geometric and electric characteristics [13] mentioned in Table I. We manually placed for each TSV in the layout, decoupling capacitor and resistors cells from the standard cell technology, with equivalent values, for the sake of simulation accuracy. Power figures used in the performance evaluation are obtained using Cadence VoltageStorm with layout extracted parasitics from Cadence Sign-Off QRC. As input an activity vector generated by gate-level netlist simulation of the core running the reference application in Cadence NCSim was used.

TABLE I
ESTIMATED TSV PARAMETERS

Number of TSVs	150
Diameter	5 µm
Pitch	10 µm
Height	20 µm
Resistance (w/ contact)	0.2 Ω
Lumped capacitance	40 fF

B. *Delay degradation*

The "interruption" of the power/ground (P/G) rails by the power switch can significantly affect both net and cell delays in clock and data paths. The switch transistor acts as a resistance between the "true" VDD and the "virtual" VDD, and in this way it produces an IR Drop on the power supply net. Since the peak voltage on the supply net is reduced, the voltage swing range in the presence of the IR Drop is smaller than the nominal voltage, which increase the net delay and input slew at the receiver. As the cell propagation delay is a function of input slew and output load, the cell delay is also negatively affected by the IR drop presence. Furthermore, since the effective cell supply voltage is lower than the nominal operating voltage, the cell delay is further increased. To make things worse, the IR Drop equally affects signal as well as clock paths, inducing variations in clock skew and clock jitter.

To evaluate the impact of IR Drop on the delay we first perform a rail analysis on the *Reference* single-tier design with classic High-V_T power switches in a mixed timing-leakage worst-case corner: $V_{DD} = 1.08\,\text{V}$ and $T = 125\,°\text{C}$ and extract the dynamic IR Drop waveforms. Based on these we rerun the timing analysis. As shown in Table II due to the high IR Drop of 107.13 mV the clock period increases to 6.855 ns and the target operating frequency cannot be met any longer. To address this issue we increase the number of High-V_T STs by moving them to a different tier in a *Stacked* CMOS 2-tier

TABLE II
CLOCK PERIOD ANALYSIS

Implementation type	Average IR-Drop [mV] on STs	on V_{DD} Rail	Total	Clock period [ns]	IR Drop aware clock period [ns]
Reference	71.40	35.73	107.13	6.577	6.855
Stacked	4.46	35.55	40.01	6.426	6.525
Hybrid	18.43	35.55	53.98	6.426	6.561

implementation. By substituting the High-V_T STs with the equivalent area of NEMFET STs in the *Hybrid* implementation the IR Drop on the STs rises from $4.46\,\text{mV}$ to $18.43\,\text{mV}$ due to the higher NEMFET R_{ON} resistance. NEMFET transistor sizing is performed according with the methodology described in [1]. However, since the supply rails become the dominant IR Drop source the total IR Drop value of *Stacked* and *Hybrid* designs are in the same range and produce similar decrease in effective clock frequency.

Overall, in comparison with the *Reference* design, the *Hybrid* proposed architecture provides almost 4x reduction of STs IR Drop and 2x reduction of total IR Drop at the expense of a 4x area increase. By reducing the fluctuation swings of the design supply voltage, the effects of process variation on circuit performance also decrease. Therefore, the tolerance of our power management architecture to process variation is enhanced.

C. Energy

Power gating is suited for blocks/systems that operate at a very low duty cycle, i.e., are being shut-off most of the times. There are four different power contributions in a duty-cycled system with power gating, as graphically depicted in Figure 6:

- *active*: Dynamic power consumption of the running system;
- *leakage(on)*: The leakage power when everything is turned on;
- *leakage(off)*: The leakage power of the always-on cells, i.e., power controller, isolation and state retention cells, when the system is in the "off" state (idle).
- *power-up/power-down*: The power consumed during on↔off state transitions.

The expression of the total energy consumed by the system is given by Equation 2.

$$\begin{aligned} E_{total} &= T_{ON} \cdot P_{ON} + T_{OFF} \cdot P_{OFF} + E_{trans} \\ &= T_{ON} \cdot (P_{active} + P_{leak,on}) + T_{OFF} \cdot P_{leak,off} \\ &\quad + T_{trans} \cdot P_{trans}, \end{aligned} \tag{2}$$

where E_{trans} is the energy during on↔off state transitions, T_{trans} the time spent by the system during power-up or power-down, and P_{trans} the power consumed during start-up or shut-down.

For the considered application, the cost of analyzing the sample data at the given sampling rate of $200\,\text{Hz}$ is 1292 cycles. However when a heart beat is detected this number

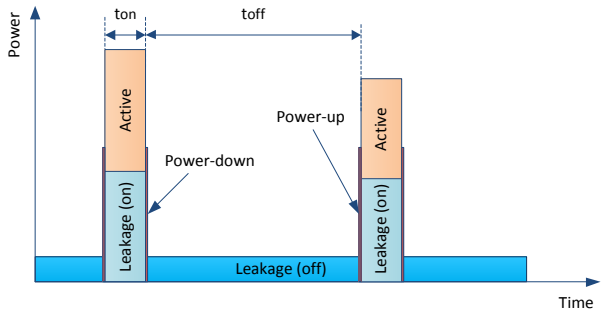

Figure 6 Energy consumption of a power-gated system.

increases to 2036 cycles. The heart beat occurs once or twice per second so on average $198.5 \cdot 1292 + 1.5 \cdot 2036 = 259516$ cycles per second. Multiplying this with the clock period gives the time when the system is active T_{ON}.

Power components, energy and the energy-delay product for the studied design implementations are listed in Table III. Power start-up time is determined through Spice simulation to be 2 clock cycles and the power-up energy for the NEMFET switch is computed using Equation 1 with the start-up maximum in-rush current. The NEMFET STs low leakage power offers a 2.75x advantage in the OFF power over the classic High-V_T STs. This advantage can be boosted even further by implementing the power management controller and the isolation cells using the same low-leakage NEMFET device.

We note that in spite of the reduced off leakage power the total improvement on the energy-delay product figure is only 9%. This happens because of two reasons: (i) the test application has a too high duty cycle, and (ii) the ON power term is dominant in the total energy equation. The ON state power consumption can be further reduced by optimizing the design in terms of power and the software application to optimally utilize the hardware resources, thus reducing the run time. To characterize the energy consumption efficiency versus various applications, we plot in Figure 7 the energy consumption of the platform for different operating duty cycles. We assume the same ON and OFF state power figures as for the bio-medical application. The duty-cycle is defined as: $T_{ON}/(T_{ON} + T_{OFF})$.

One can observe in the figure that the energy requirements follow the same trend for all implementations, with a steep decrease until the application duty-cycle reaches 0.0001. Optimizing and reducing the application duty-cycle lower than this doesn't bring much energy savings any longer. However, from this point further, for even lower activity applications the relative savings in energy consumption due to our power architecture when compared to High-V_T STs start to increase, reaching up to 60% lower energy consumption.

Piezoelectric vibration scavengers had previously been proven to be viable candidates for hybrid MEMS/NEMS-CMOS integrated energy generators [14], [15]. State-of-art piezoelectric scavengers from [15] report a normalized power

TABLE III
POWER AND ENERGY RESULTS

Implementation type	ON power [mW]	OFF power [nW] STs	OFF power [nW] Always-on cells*	OFF power [nW] Total	Power-up energy [pJ]	Total energy [µJ]	Energy-Delay Product [µJ·ns]
Reference	5.0340	56.28	26.02	81.28	48.04	9.05	62.01
Stacked	5.0343	900.44	26.02	925.44	48.04	9.46	61.72
Hybrid	5.0339	4.52	26.02	29.52	32.83	8.61	56.47

Active time=1.73 ms, Idle time=993.35 ms, Transition time=5.32 ms @ 150 MHz.

* Always-on cells = Power management controller and isolation cells

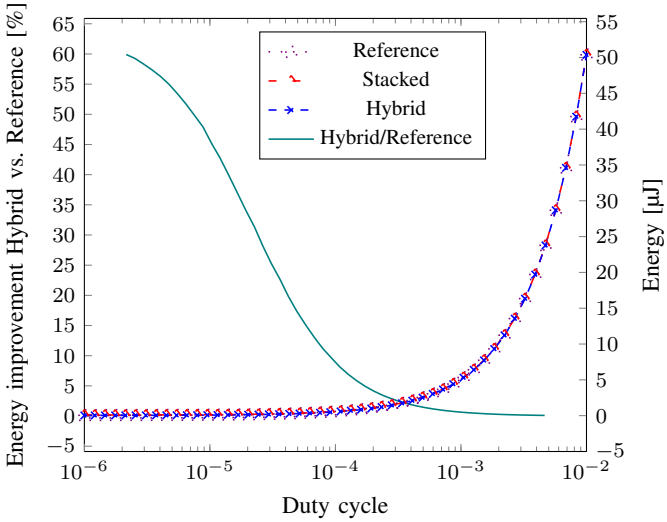

Figure 7 Energy Consumption versus Duty-cycle.

density of up to 6.45 µW/mm^3/g^2. Thus, assuming a 1 g constant acceleration, a piezoelectric scavenger with 1.33 mm^3 volume can meet our energy demand of 8.61 µJ, rendering the battery unnecessary. The additional circuitry necessary for managing the energy scavenger can be implemented on the same tier as the digital circuitry, while the scavenger and the NEMFET power switches can share the other tier. Alternatively, the large energy scavenger can be split into several tiers. 3D stacked integration using TSVs use thinned 50-100 µm dies, therefore a single package can accommodate the energy harvester, power circuitry, and digital circuit.

Hence, we can conclude that our proposed architecture can help ubiquitous embedded nano-systems cope with very tight energy budgets. We believe it to be a promising candidate in reaching truly "zero-energy" ubiquitous nanosystems. Low activity applications such as sensing application are likely to benefit from the NEMFET-based power management architecture. Furthermore, an interesting future work consists of a design space exploration of combined low power techniques: e.g. NEMFET-based power gating, and voltage and frequency scaling. Thus, comprehensive research is needed in order to achieve the optimal solution from the "zero-energy" perspective.

IV. CONCLUSION

In this paper we described and evaluated a 3D hybrid power management architecture which makes use of Nano-Electro-Mechanical Field Effect Transistors (NEMFET) as power switches that cut-off the power supply of inactive blocks. This approach has a number of advantages as follows: (i) it combines the appealing extremely low leakage currents of the NEMFETs with the versatility of CMOS technology by allowing for the power switches to be fabricated on a separate die; (ii) it simplifies the power planning in general, allows for always-on blocks to also be implemented with NEMFETs, and can increase the computation platform performance because of extra area cleared by the switches on the CMOS tier; and (iii) it leverages the integration of other NEMS/MEMS devices, e.g., energy harvesters, sensors, on the same tier with the power switches. To validate this proposal and evaluate its performance in a real-life scenario we considered the 3D embodiment of an embedded openMSP430 processor based SoC platform running a bio-medical sensing application for heart rate detection and measured the effects of the 3D hybrid architecture on sensitive metrics used in power gating designs, e.g., delay degradation, power-up and power-down behavior, and overall energy consumption. Our experiments indicated that: (i) the system idle energy is decreased by 2.74x at the expense of a 4x area overhead on the NEMS tier; (ii) the energy-delay product of the embedded SoC platform was reduced by 9%, with a potential improvement of up to 60% for applications with lower activity, e.g., wireless sensor networks; and (iii) the IR Drop was reduced with a factor of 4x thus no clock period degradation was experienced. Based on our experiment we believe that such 3D hybrid NEMS/CMOS creates the premises for the substantial reduction of an increasingly important component of the total energy consumption, the leakage power while idle, thus it makes nanosystems meet the limited energy budget of local energy harvesters, and become potentially autonomous "zero-energy" devices.

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