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Fault Tolerant Structures for Nanoscale Gates

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***Abstract*—Predicted device reliability for nanoelectronics indicates that redundant design will be necessary to build reliable nanosystems. Up to date, several fault tolerant techniques have been proposed and analyzed. However, the fabrication complexity of those circuits, which directly affects the final circuit reliability, is not usually considered. In this paper, we compare two fault tolerant techniques, NAND Multiplexing (NM) and Averaging Cells (AC), as possible solutions to improve the nanoscale gate reliability. First, we propose nanodevice specific layouts for the two techniques. Then, we introduce nanotechnology oriented models to evaluate the area cost and reliability of the gates. Our simulations indicate that NM based gates are more reliable than AC gates when the error probabilities of the circuit parts are lower than 0.003. However, when this value is exceeded (which is expected for electronic nanotechnologies) AC gates are more reliable at a lower area cost.**

***Keywords*—Defect Tolerance, Fault Tolerance, NAND Multiplexing, Averaging Cell, Complexity Estimation.**

I. Introduction

Electronic gates exhibit a certain error rate due to several uncertainty sources such as fabrication defects, variations on the device parameters, internal noise (i.e., thermal noise and shot noise) or external noise sources (i.e., crosstalk, substrate noise, and cosmic rays). The shrinking of the electronic devices near to the atomic scale [1], [2] increases the effect of these error sources. Therefore, as the electronic technology goes into the deep nanoscale, the device reliability decreases rapidly [2]. The power supply voltage scaling that reduces the maximum density of dissipated energy reduces the noise margins too. This can lead to extremely low signal-to-noise ratios (approaching 0–1 dB [3]) and increases the gate sensitivity to device parameter variation, which is currently a cause of yield reduction [4] and it is expected to become even more relevant in the near future [5]. Predictions for nanoscale technologies indicate that the device reliability will decrease several orders of magnitude [6] and current implementations confirm this tendency [7].

In order to build reliable electronic systems using electronic nanotechnologies it is necessary to include fault and defect tolerant capabilities into the electronic systems. The error sources have very different characteristics and ways to affect the victim gate. Therefore, the design of a reliable system will require the combination of several layers of different tolerant techniques [8]. Current tolerant mechanisms use hardware redundancy to detect and/or correct the errors. The most utilized techniques are NAND Multiplexing (NM) and majority voting gates, as proposed by von Neumann [9] in 1955. More recent techniques based on Averaging Cells (AC) [10]–[12] and reconfiguration [13] have been also proposed. A different path to error tolerance is the augmentation of the processed data with codes that can detect and/or correct errors [14], [15]. This technique is widely used in telecommunications, but its application on ICs, which experience a higher error rate, must be carefully evaluated because the coding and decoding circuits are also affected by errors.

In this paper we compare two fault tolerant architectures that can be used to build a first tolerant layer responsible to improve the reliability of the basic logic nanogates. The objective is not to find a global solution using a single technique, but to provide logic gates with an improved reliability in order to start a pyramidal structure to achieve reliable nanoelectronic systems. This first layer must be able to provide coverage to both dynamic and static errors with minimum circuit complexity. Therefore, the best techniques for this level are NM (as indicated in the comparison presented in [16]) and AC (due to its simplicity). To compare both structures we first define layouts for NM and AC NAND gates using molecular nanodevices. To evaluate the reliability of the resulting gates considering the fabrication complexity we introduce nanoscale oriented models able to estimate the error probabilities of each part composing the circuits according to their fabrication complexity. Using the physical dimensions of the gates obtained from the layouts and the proposed models we calculate the area cost and the error probability for those gates. Our simulation results indicate that NM based gates are more reliable than AC gates when the error probabilities of the circuit parts are lower than 0.003. However, when this limit is exceeded (which is expected to be the case for electronic nanotechnologies) AC gates are more reliable at a much lower area cost.

The paper is organized as follows: Section II introduces the nanoscale oriented models. Section III describes the basic principles of both tolerant techniques and proposes a possible physical implementation for each NAND gate. Section IV describes the simulation procedure to calculate the gate error probabilities and Section V presents the obtained results. Finally, section VI draws the conclusions.

II. Fabrication Complexity Estimation

The fabrication of a nanoelectronic gate comprise several steps. The first step is the fabrication of the nanodevices and

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nanoconnections. Then, it is necessary to place these building blocks on precise locations. Finally, devices and connections must be electrically contacted at the exact contact areas. As far as we are aware of there are no precise models able to characterize the complexity and error probability of each of these steps. However, we can assume that the error probability is proportional to the dimensions of each part. As a first approximation to the problem we consider a linear relation between the error probability and the dimensions of each element. Based on that, the error probability for each element can be expressed as:

$$P_{\text{Dev}} = \frac{\alpha}{V_{\text{Dev}}} \tag{1}$$

$$P_{\text{Cont}} = \frac{\beta}{A_{\text{Cont}}} \tag{2}$$

$$P_{\text{Wire}} = L_{\text{Wire}} \frac{\gamma}{A_{\text{Wire}}} \tag{3}$$

where α stands for the device error probability per volume unit, β for the contact error probability per area unit, and γ for the wire or connection error probability per area and length unit. V_{Dev}, A_{Cont}, L_{Wire}, and A_{Wire} are the device volume, contact area, wire length and wire section, respectively. In order to calculate the area cost and the error probability for a given gate, it is necessary to define its physical structure as the element dimensions depend on the circuit topology and the redundancy factor N.

III. Defect Tolerant Gate Architectures

The design of a first layer of tolerant nanogates requires architectures capable of tolerating static (defects) and dynamic (faults) errors. This requirement discards the reconfiguration techniques and focus the interest in NM, AC, and majority voting gates. As indicated in [16], NM presents a better error tolerance capacity than the majority voting gates. The NM architecture is based on combinatorial techniques and the restitution capability of NAND logic functions. AC is selected because its structure is extremely simple and it presents a promising tolerance to nanodevice errors [10], [12]. AC gates, by using the averaging function, convert the device critical defects in an analogue signal degradation that is restored afterwards by the non-linear transfer function of the following stage (assuming its noise margin is not overcome). Both considered gate architectures and their potential implementations with nanodevices are discussed in the following subsections. In order to compare the performance of both techniques, we consider that the nanodevices are of minimum size with a prismatic shape of length L and section D^2. The minimum distance between two parts of a circuit is assumed to be D.

A. NAND Multiplexing Structure

A NAND Multiplexing gate replicates all the elements of the basic logic function and adds two extra sets of redundant NAND gates and two interconnection randomizers (elements that randomly connect the output lines of one layer to the input lines of the following layer in order to distribute the errors along the bundle) to restitute the activation fraction of the signal bundles. Fig. 1 depicts the logic scheme for an NM NAND gate. In this scheme all the signals are digital. Thus each wire transmits a single bit. The global bundle activation determines whether the bundle encodes a ’0’ or a ’1’ bit.

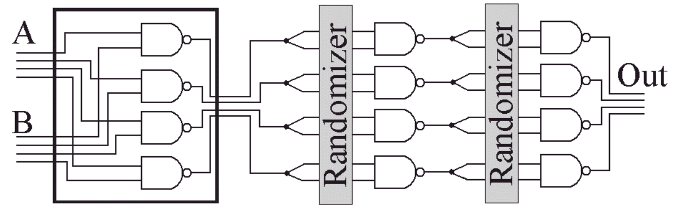

Figure 1. Scheme for a NAND Multiplexing NAND gate.

To evaluate the cost and the reliability offered by this technique, it is necessary to propose a physical implementation for the NAND gates and randomizer blocks. As contacts at the nanoscale are difficult to implement [17], we select a NAND structure that minimizes those. The proposed NAND structure is presented in Fig. 2. It consists of two blocks: the first processes the information using a diode-like architecture and the second, formed by a CMOS-like inverter, restitutes and inverts the signal. A nanodevice based layout for the NAND gate is presented in Fig. 3 (left). Note that the layout is 3-D, the axes in the figure indicate the orientation of each part. The placement and orientation of the devices are optimized to reduce the total area and complexity of the NM gate (supply voltage connections at the top and bottom of the cell and input and output lines on the sides). The NAND gate is composed by five devices, eleven contacts (indicated by numbers in the figure), and one interconnection. To obtain a correct gate output, it is necessary that all the devices, contacts and interconnections present no error (i.e., no defects nor faults at any single part). Using (1), (2), and (3) and the dimensions of each element of the NAND gate we can calculate the NAND error probability as:

$$P_{\text{err}_{\text{NAND}}} = 1 - (1 - P_{\text{Dev}})^5 (1 - \frac{\beta}{2DL + 8D^2})^3 (1 - \frac{\beta}{LD})^5 (1 - \frac{\beta}{D^2})^3 (1 - (L + 2D)\frac{\gamma}{D^2}). \tag{4}$$

This error probability arises from the individual error probabilities and sizes of each part of the cell. The first parenthesis correspond to the five devices, the second, third and fourth parenthesis to contacts 1-3, 4-8, and 9-11, respectively (see Fig. 3 left). The last parenthesis capture the error probability in the interconnection.

The randomizer block is built by hardwiring the outputs of one NAND stage to the inputs of the next. In principle, the pattern must be random. However, a pattern that disperses the outputs originated in adjacent gates, to avoid the propagation of error clusters, is usually valid. In order to analyze this block we assume that it is possible to manufacture interconnections with sections D^2 of any length. We also

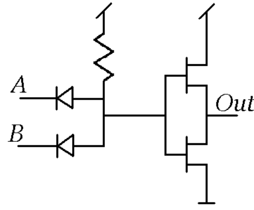

Figure 2. Circuit topology used to implement the NAND gates.

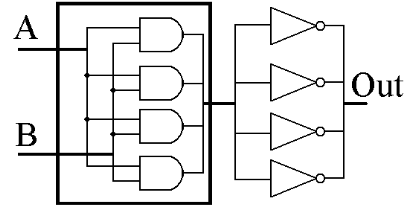

Figure 4. Scheme of a tolerant NAND gate using the averaging cell technique.

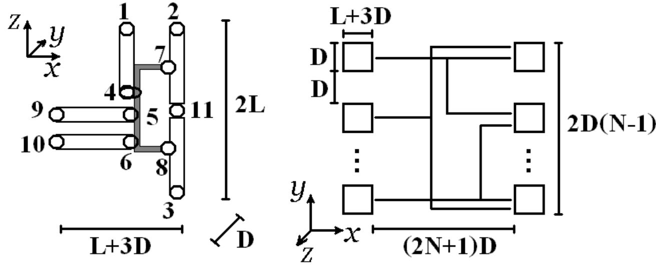

Figure 3. Proposed layout for a NAND gate (left) and a randomizer block (right) using nanodevices.

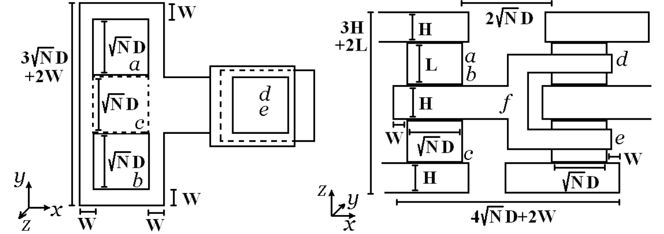

Figure 5. Proposed layout for the averaging cell NAND gate using nanodevice clusters and metallic interconnections.

assume that the randomizer is built using only two levels of interconnections (there is no information about how this block can be manufactured so we use the same assumptions as for a typical CMOS process). Fig. 3 (right) illustrates the proposed schematic layout for this block with its approximate dimensions. The squares in the scheme represent the NAND gates. In general, to fully connect the N output lines into the $2N$ input lines, it is necessary to place N wires vertically. Therefore, the average length of this block is estimated to be $(2N + 1)D$ and the maximum and minimum distance for any single interconnection (considering a Manhattan routing and obviating the distance between the two interconnection layers) is $(2N + 1)D$ and $(4N - 1)D$, respectively. As a first approximation we use the average value to calculate the interconnection error probability which is expressed as:

$$P_{\text{err}_{\text{Wire}}} = 3ND\frac{\gamma}{D^2}. \quad (5)$$

Using the geometric information in Fig. 3 and Fig. 1 we can estimate the area for an NM NAND gate as:

$$A_{\text{NM}} = 8N^2D^2 + 22ND^2 + 6NDL, \quad (6)$$

which indicates a quadratic relation between the area cost and the redundancy factor.

B. Averaging Cell Structure

We propose to use a structure for the averaging cell gate that only replicates the devices (Fig. 4). The layout structure requires a large connection able to interconnect all the nanodevices. Having a non-redundant connection reduces the gate protection against errors. However, the reliability penalty is not large and it greatly simplifies the gate structure as no molecular scale features need to be built. It transmits an analogue value that represents the digital bit. Thus, when the signal is above a defined threshold the wire transmits a '1' and a '0' otherwise. All the redundant elements receive the same input values and their outputs are combined into a single line by averaging (i.e., adding the output currents over a resistor).

The proposed NAND gate is implemented following the same circuit topology used for the NM NAND gate (Fig. 2). The considered layout also takes advantage of the 3-D stacking capability of molecular nanodevices. Fig. 5 depicts the layout for an AC NAND gate from two different perspectives (see the axes in the figure). In this gate the five devices are replaced by clusters of nanodevices working in parallel (indicated by letters a to e in the figure). Clusters a, b, c compose a diode-like AND function and d, e a NOT function. The internal wire connecting both logic functions is designated by f. This interconnection connects all the devices together. Thus, the total connection area is $\sqrt{N}D$. It means that the minimum dimensions required to build this structure are determined by the cluster size, not by the nanodevice dimensions. Parameters W and H indicate the minimum distance from the nanoclusters to the borders of the metal interconnections and the minimum thickness of a metal line, respectively. These two parameters are dependent on the manufacturing technology. In AC gates the minimum dimensions are determined by the cluster size. We assume values $W = H = \sqrt{N}D$ as a worst case scenario. This layout has been proposed considering the capacity of some nanodevices to self-assemble into defined regions to build nanoclusters of devices as demonstrated in [18].

From Fig. 5 we can observe that the contact areas for any given nanodevice considerably increase with the redundancy factor (N). The error probability for one individual AND gate (considering that all the parts must be functional) is given by the error probability of the three devices and the six contacts

that compose the gate and equivalently for the NOT gate. Then,

$$P_{\mathrm{err}_{\mathrm{AND}}} = 1 - (1 - P_{\mathrm{Dev}})^3 (1 - \frac{\beta}{ND^2})^6, \quad (7)$$

$$P_{\mathrm{err}_{\mathrm{NOT}}} = 1 - (1 - P_{\mathrm{Dev}})^2 (1 - \frac{\beta}{ND^2})^4. \quad (8)$$

This structure provides a high tolerance to errors in the nanodevices. However, errors appearing in the interconnection between the two logic functions or defects short-circuiting any nanocluster are critical. To model the latter probability it is necessary to introduce a new scaling law for the probability of having a defective nanocluster. This probability increases with the cluster area. It can be estimated by

$$P_{\mathrm{Cl}} = \kappa A_{\mathrm{Cl}}, \quad (9)$$

where κ stands for the error probability per area unit of a critical defect in the nanocluster and A_{Cl} for the cluster area. Then, the probability of a critical defect in the structure can be approximated as:

$$P_{\mathrm{err}_{\mathrm{Crit}}} = 1 - (1 - ND^2\kappa)^5 (1 - \frac{\beta}{L\sqrt{N}D})^2 \\ (1 - (8\sqrt{N}D)\frac{\gamma}{ND^2}). \quad (10)$$

Using the dimensions in Fig. 5 we can also estimate the area cost of this gate as:

$$A_{\mathrm{AC}} = (3\sqrt{N}D + 2W)(4\sqrt{N}D + 2W) = 30ND^2, \quad (11)$$

which has a linear dependence on the redundancy factor N. We note here that the parameter L is not relevant for the area calculation of this cell because in the proposed layout it only affects the vertical axis (z).

IV. Simulation Procedure

Using (4), (5), (7), (8), and (10) we calculate the error probability of each element of both tolerant NAND gates. Then, we obtain the gate error probability by a Mote Carlo analysis with 10^6 runs. To approximate the working conditions of these gates and include realistic inputs, the analysis considers a chain of three gates as depicted in Fig. 6. The initial NAND and NOT gates are used to produce a high signal with a realistic error probability. The resulting signal is fed to the second NAND gate which is the device under study. The simulation considers two logic 1 inputs as this is the worst case scenario for a NAND gate (no possible error masking due to the logic function).

The simulation procedure for NM gates assigns a bit for each gate element (NAND gates and wires). This bit indicates whether the element is defective or functional and is calculated according to (4) and (5). The output of each layer (NAND and randomizer blocks) is computed assuming perfect elements. Then, the outputs corresponding to defective elements are inverted. This process is done layer by layer to emulate the error propagation inside the NM gate. If the activation fraction at the second gate output is higher than 0.5 the gate is considered to be defective.

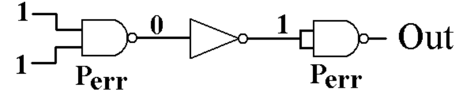

Figure 6. Circuit simulated to calculate the error probability of both tolerant gates.

The procedure for AC gates is slightly different. In this case, using the error probability from (7) and (8) we calculate the number of defective elements in each nanocluster and, consequently, the analogue output value (each gate provides an Nth part of the output voltage). If any of the intermediate outputs crosses the 0.5 threshold (considering an output range 0 to 1 V) the gate is considered defective. This procedure yields the error probability of the gate failing due to the nanodevices. To obtain the error probability for the entire AC NAND gate we add $P_{\mathrm{err}_{\mathrm{Crit}}}$ – given in (10) – to this value to consider the gate critical defects.

V. Results

One of the most promising nanotechnologies for implementing deep nanometric electronic systems is based on molecular devices [2]. These devices have diameters around 1 nm according to [18]. Considering this dimension, we can assume that our nanodevices have a volume of 2x1x1 nm^3 ($L = 2$ nm and $D = 1$ nm). Using these dimensions, we calculate the area cost for each gate from (6) and (11). Fig. 7 shows the area cost as a function of the redundancy factor. As indicated by (6) and (11), NM area increases with N^2 while AC with N. This fact is important as it determines the acceptable redundancy factor for each tolerant architecture. For example, under our assumptions, an NM NAND gate with $N = 220$ has the same area cost as a 65 nm CMOS NAND while AC gates can use redundancies over 1000 at a lower area cost. As current CMOS technology advances, the gate area decreases rapidly. If we consider the area estimation for a 45 nm CMOS NAND, the NM acceptable redundancy ratio for practical implementations is reduced below 170.

To evaluate the gate error probability for both structures it is necessary to define the parameters α, β, γ, and κ. Little experimental information is available. However, we can define a structural error probability, P_{ErrStr}, (the error probability for the minimum size element) to be in the range $\langle 10^{-4}, 10^{-1} \rangle$. Then, from (1), (2), and (3) we calculate α, β and γ. κ represents the probability of finding a short-circuit in a cluster (we consider values of 10^{-7}, 10^{-8}, and 10^{-9} nm^{-2}). Using these data we calculate the error probability for both structures. Fig. 8 compares the reliability of an NM NAND gate with a redundancy factor $N = 100$ (given the area cost of NM this redundancy factor is reasonable, see Fig. 7) with an AC NAND gate having the same redundancy factor and also with one having the same area cost ($N = 2780$). Our simulations indicate that for P_{ErrStr} below 0.003 NM provides the best fault tolerant capacity. However, when the error probability of the structural elements grows above this value, AC gates

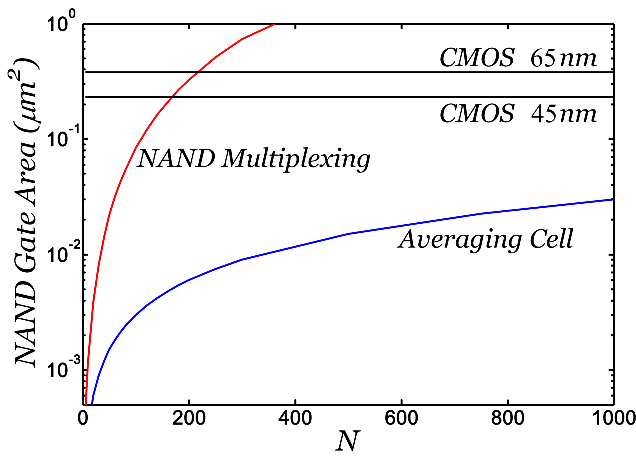

Figure 7. Area cost as the redundancy factor increases for both techniques. Constant lines indicate an estimation for a NAND gate in CMOS 65 nm and 45 nm technologies.

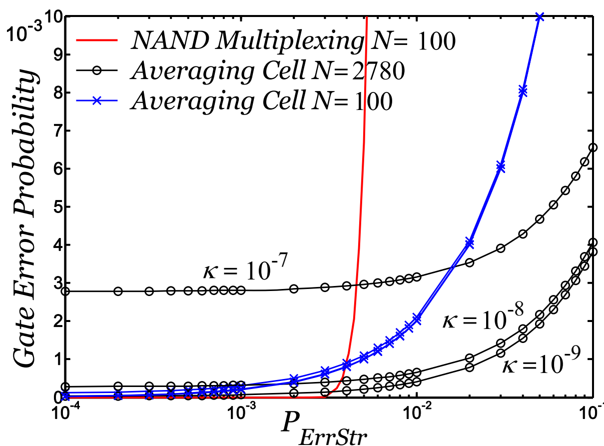

Figure 8. Error probability for a NAND gate using NAND Multiplexing technique with $N = 100$ and using averaging cell technique with the same redundancy factor and the same area cost ($N = 2780$).

present better reliability at a lower area cost. In general, as expected, increasing the redundancy factor increases the gate reliability. However, as indicated by the results in Fig. 8, the cluster error probability limits the maximum redundancy factor for practical AC gates. Note that this limitation is only relevant for very large redundancy ratios. For $N = 100$, the three curves considering different values of κ are nearly identical.

VI. Conclusions

In this work we have studied two techniques (NM and AC) as possible ways to implement the first layer of a hierarchical tolerant system. This layer is responsible of improving the logic gate reliability. We have compared the area cost and reliability improvement delivered by these two hardware redundancy based techniques. The comparison considered the fabrication complexity of the redundant structures, which can determine the practicality of a circuit and which is usually neglected in similar analysis. For this reason we derived models able to estimate the dependency of the error probability on the dimensions of the circuit's parts. We have proposed a simple linear dependency between the error probability and the element dimensions. Our simulations have indicated that NM gates have better reliability than AC gates for small structural error probabilities. However, for structural error probabilities above 0.003, which is the expected situation in future nanotechnology devices, AC gates presented a better reliability. Besides, the area cost of AC gates scales with N while NM gates scale N^2. This fact limits the practical redundancy factors for NM below 200. In this respect AC gates are able to use larger redundancy factors ($N > 1000$) with a reasonable area cost.

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