MANUFACTURABILITY ISSUES OF REDUNDANT NANOGATES

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Abstract
Predicted device reliability for nanoelectronics indicates that redundant design will be necessary to build reliable nanosystems. The study of such systems requires the evaluation of the error probabilities associated to the fabrication process complexity. In this paper we compare two layouts for a basic NAND gate used to implement NAND Multiplexing (NM) redundant gates. To analyse the effects of the layouts, we derive models to calculate the error probability of each gate part according to the resolution errors of the manufacturing process. Our results indicate that gates built with diode-logic topologies are more reliable than gates built with CMOS like topologies and that the resolution errors limit the redundancy of practical NM gates.
Keywords: *Defect Tolerance, Fault Tolerance, NAND Multiplexing, Complexity Estimation.*

1. INTRODUCTION

Electronic gates exhibit a certain error rate due to several uncertainty sources such as fabrication defects, variations on the device parameters, internal noise (i.e., thermal noise and shot noise) or external noise sources (i.e., crosstalk, substrate noise, and cosmic rays). The shrinking of the electronic devices near to the atomic scale [1,2] increases the effect of these error sources. Therefore, as the electronic technology goes into the deep nanoscale, the device reliability decreases rapidly [2]. Predictions for nanoscale technologies indicate that the device reliability is expected to decrease with several orders of magnitude [3] and current implementations confirm those predictions [4].

In order to build reliable electronic systems using electronic nanotechnologies it is necessary to include fault and defect tolerant capabilities into the electronic systems. One of the most promising tolerant structure is NAND Multiplexing (NM) proposed by von Neumann [5] and considered to be one of the best fitted for highly unreliable gates [6,7]. This scheme uses redundant gates and wires, which, for the redundancy levels required by nanotechnology, results in highly complex circuits. Considering that building extremely small and complex patterns increases the probability of having defective parts, it is necessary to analyze how the circuit complexity affects the reliability of each circuit part and on overall of the redundant gate.

In this paper we compare two different layouts (CMOS-logic and diode-logic) for a basic NAND nanogate. To evaluate the effects of each layout on the gate reliability it is necessary to characterize the error probability of each gate part. Following this goal, we consider a technology where the interconnections are fabricated using metallic wires, with minimum feature size W (width and separation), following the standard mask-deposition method and the devices are implemented with either molecules or carbon nanotubes that are positioned somehow on specific contacts. We note here that, even though possible, such a technology is just a discussion vehicle that allows us to study the relationship between the manufacturing process resolution and quality and the gate reliability. We propose models to estimate the error probability for this technology and we compare the reliability of the two proposed layouts. Our results indicate that the CMOS-logic NAND has 20 to 100% higher error probability at an area cost which is 30 to 40% larger. Therefore, the utilization of diode-logic layouts permits the potential construction of tolerant gates with a reasonable amount of area overhead. The NM gates are capable to increase the gate reliability, but the manufacturing process resolution errors limit the practical redundancy factor.

The paper is organized as follow: Section 2 introduces the nanoscale oriented models for the reliability of nanodevices and interconnects. Section 3 presents the NM gate scheme and the proposed layouts for the basic NAND gate and for the randomizer. Section 4 presents the reliability study for the basic NAND gates, the interconnections, and the redundant gates as functions of the process quality. Finally, Section 5 draws some conclusions.

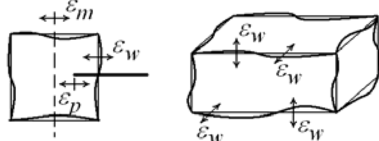

Fig. 1. Errors due to process resolution.

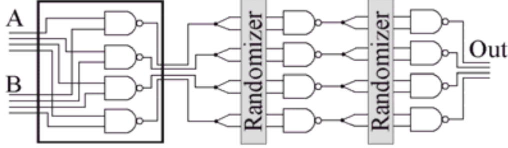

Fig. 2. Scheme of a NAND NM gate.

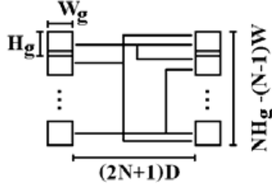

Fig. 3. Randomizer unit layout.

2. RELIABILITY MODELS

Circuits are built from metal lines, devices, and contacts. These elements are not perfect due to the limitations in the fabrication process. Fig. 1 illustrates some of the resolution errors caused by the manufacturing process. The thickness, height, and width of the metal lines vary (ε_w) and their position may differ (ε_m) from the nominal value. Besides, a small defect or transient fault may induce errors in the interconnection with a certain fault probability (P_w). In a similar way the positioning of the nanodevices is subject to errors (ε_p) and they may be defective, the contact may fail (even if the positioning was correct), or a transient fault may occur with a P_d probability. Moreover when three terminal devices are considered it is necessary to build the gate insulator. The width of the insulator may also vary (ε_g).

The resolution errors can be assumed to be normally distributed with a standard deviation covering 95% of the nominal error resolution (Δ). Using these errors it is possible to calculate the error probability for a contact due to the positioning errors as:

$$P_{ErrCont} = P\{\varepsilon_p - \varepsilon_m - \varepsilon_w < |W/2|\}, \qquad (1)$$

where $W/2$ is the maximum allowed deviation, which is actually the acceptable deviation for a minimum width wire.

An interconnection can be assumed to be defective if at some point it has a section that is lower than 60% of the nominal section or it has a defect or a fault. Then, the error probability for an interconnection is:

$$P_{ErrWire} = WL_w P_w P\{(W+\varepsilon_{wx})(W+\varepsilon_{wy}) < 0.6W^2\}^{L_w/L_p} \qquad (2)$$

where W and L_w are the wire width and length, respectively, and ε_{wx} and ε_{wy} are the accumulated error in each dimension per interconnection slide. The interconnection is divided in L_w/L_p slices according to the fabrication process resolution where $L_p=50\Delta_w$ reflects a certain correlation in the fluctuations along the interconnection. The gate error is calculated in a similar way but considering the gate parameters and a single slice.

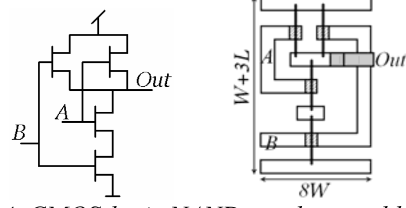

Fig. 4. CMOS-logic NAND topology and layout.

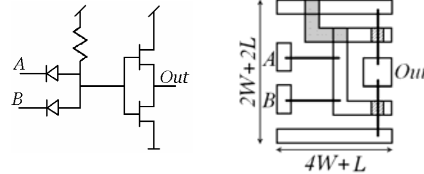

Fig. 5. Diode-logic NAND topology and layout.

3. GATE LAYOUTS

An NM gate (Fig. 2) is composed by three layers of gates and two randomizer blocks [5]. The first layer is composed by N logic gates implementing the desired logic function (the processing unit). The restitution unit is composed by two layers of N NAND gates and two layers of interconnections which uncorrelate the error positions. The randomizer units are built with metal wires. Their dimensions depend on the dimensions of the gates they connect. Fig. 3 shows the randomizer layout and dimensions for gates of height H_g and width W_g where the cells share one of the power supply lines. We assume that all the lines are of minimum width W and the routing follows the Manhattan style. Then, the average interconnection length for this element is

$$L_{ave} = (3(N+1)W + (N-1)H_g)/2\,. \qquad (3)$$

CMOS technology uses four 3-terminal devices to build the NAND gate. Our first layout uses this circuit for the NAND gate. Fig. 4 presents the circuit topology and the proposed layout with dimensions $H_g=W+3L$ and $W_g=8W$. The top and bottom metal lines are the power supply voltage

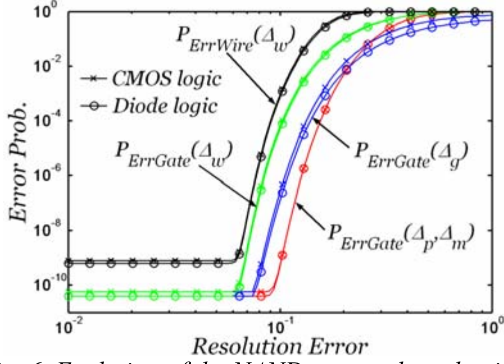

Fig. 6. Evolution of the NAND gate and randomizer wire error probability with the resolution errors.

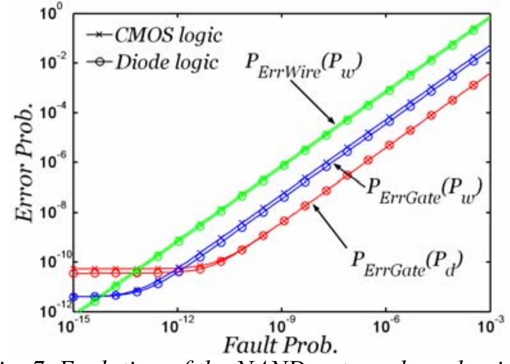

Fig. 7. Evolution of the NAND gate and randomizer wire error probability with P_d or P_w.

lines. The u-shaped lines define the gate connections and the small horizontal lines are an intermediate node and the output node. In grey we indicate the output wire using the second metal level and the line patterned regions point out the nanodevice gates.

An alternative to CMOS-logic is diode-logic gates. In this case we propose a mixed logic where the information processing is done using diode-logic and the inversion and buffering is implemented using CMOS-like inverters. Fig. 5 presents the topology and the proposed layout for such a gate. The layout uses nanodevices for the diode and transistor functions (thick black lines), but implements the resistor as a stripe line (such as an oxide layer), which has the same processing variations as a normal metal line (indicated in grey in the figure). The top and bottom lines are the power supply voltage lines and the u-shaped line the inverter input. Nanodevice gates are indicated by line patterned regions. The layout dimensions are smaller than for the CMOS logic gate, $H_g=2W+2L$ and $W_g=4W+L$.

The dimensions of the basic NAND gate affect the NM gate area cost and also the length of the randomizer interconnections. If we consider the minimum length for the nanodevices ($L\geq 4W$), the NM NAND, using CMOS-logic gates, area cost is $A_{NMCM}=W^2(48N^2+74N+5)$ and using diode logic it reduces to $A_{NMDI}=W^2(36N^2+49N+5)$. This indicates a 30 to 40% area increase for CMOS-like gates and a 20% connection length increase –from (3)– in the randomizers operating in conjunction with CMOS-logic gates.

4. RELIABILITY ANALYSIS

Using the reliability models introduced in Section 2 and the layouts presented in Section 3 it is possible to calculate the error probabilities for each element composing the basic NAND gate. Then, considering that all the parts of the gate must be functional to obtain a non-defective gate the error probability for each layout can be calculated as

$$P_{ErrGate} = 1 - \prod (1 - P_{ErrParts}) . \quad (4)$$

4.1. NON-REDUNDANT STRUCTURES

To better observe the effects of each parameter we use the following optimistic set-up: Δ_g=1%, Δ_m=1%, Δ_p=1%, and Δ_w=5%; fault probabilities P_d=10^{-12} and P_w=10^{-12} and N=100 as a base point for a parametric analysis to compare the two proposed layouts. Fig. 6 presents the evolution of the NAND gate ($P_{ErrGate}$) and the randomizer connection ($P_{ErrWire}$) error probabilities for both considered layouts as the different resolution errors increase. We can observe that, using this setup, the error probability is determined by the wire and device error probability for small resolution errors (Δ<5%). Above this value, Δ determines the gate and wire error probabilities. For Δ>30–40% it is not possible to build the gate at all ($P_{ErrGate}\approx 1$ and $P_{ErrWire}\approx 1$).

Fig. 7 plots the error probabilities for the NAND gates and the randomizer connections as the wire and device fault probabilities vary. For fault probabilities below 10^{-13}, the resulting error probability is determined by the resolution errors. However, for higher error probabilities there is a direct relation between the device and wire errors and the NAND and interconnection errors. As the plots in Fig. 6 and 7 are logarithmic it is not easy to observe the difference between the two layouts. Fig. 8 shows the CMOS to diode-logic error probability ratios for the curves in Fig. 6 (–o–) and 7 (–x–). From this plot we can observe that the CMOS-logic layout has higher error probabilities in all the cases. The error probability increases by a factor ranging from 1 to 2.

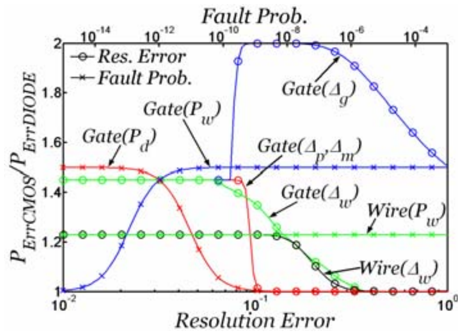

Fig. 8. Ratio between the error probabilities for the CMOS versus diode logic layouts.

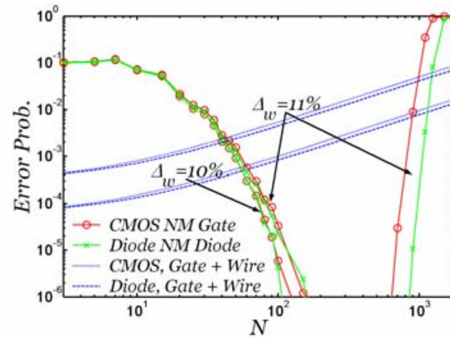

Fig. 9. Error probability for the NM gates.

4.2. NAND MULTIPLEXING GATES

Finally, we study the effects of the layouts on the reliability of the NM gates. The analysis of the NM gates is done by simulation. The simulation assigns a bit to each gate element (NAND gates and randomizer wires). This bit indicates whether the element is defective or functional and it is calculated according to the models proposed in Section 2. The output of each layer (NAND and randomizer blocks) is computed assuming non-defective elements. Then, the outputs corresponding to defective elements are inverted (von Neumann errors). This process is done layer by layer to emulate the error propagation inside the NM gate. The simulation uses two inputs at logic '1' coming from a similar gate. Then, if the gate output activation fraction is higher than 0.25 the gate is considered to be defective.

Fig. 9 plots the NM gate and the combined gate and wire error probabilities according to N. We use a realistic set of parameters for the resolution errors and fault probabilities [2,8]: Δ_g=2.5%, Δ_m=5%, Δ_p=5%, $P_d=10^{-6}$, and $P_w=10^{-10}$ with Δ_w=10%. We observe that the NM gate is able to improve the function reliability for N>70 with similar performance for both layouts. However, for a slightly worst Δ_w=11% the error probability of the implementation using CMOS-logic NANDs can be 50% larger than using diode-logic gates. Even more relevant to note is the fact that, due to the randomizer connection length increase (and, accordingly, the wire error probability), there is a maximum redundancy factor above which the NM gate reliability decreases with increasing N. For Δ_w=11%, the plot indicates that for N>1000 the NM gate is less reliable than the original NAND gate.

5. CONCLUSIONS

We have proposed models to estimate the error probability of the nanometric interconnections, contacts, and devices according to the fabrication process resolution errors. Using these models we have analyzed the reliability of two layouts for a NAND gate showing that a CMOS-like topology has 20 to 100% higher error probability at an area cost which is 30 to 40% larger when compared with a diode-logic topology. These NAND gates have been used to build NM gates. Our results indicate that for the expected fabrication resolution errors this technique is able to improve the gate reliability using N>70. However, due to randomizer interconnection complexity there is a maximum N above which the reliability decreases with the redundancy factor.

REFERENCES

[1] R. Chau *et al.*, "Silicon nano-transistors and breaking the 10 nm physical gate length barrier," *Device Research Conference*, pp. 123–126, 2003.

[2] Int. tech. roadmap for semiconductors, 2005, www.itrs.net/Common/2005ITRS/Home2005.htm.

[3] A. Kleinosowski *et al.*, "Exploring fine-grained fault tolerance for nanotechnology devices with the recursive nanobox processor grid," *Nanotechnology, IEEE Trans. on,* vol. 5, pp. 575–586, 2006.

[4] J.E. Green et al., "A 160-kilobit molecular electronic memory patterned at 10^{11} bits per square centimetre," *Nature*, vol. 445, pp. 414–417, 2007.

[5] J. von Neumann, "Probabilistic logics and the synthesis of reliable organisms from unreliable components," in *Automata Studies*, C. Shannon and J. McCarthy, Eds., Princeton University Press, Princeton N.J., pp. 43–98, 1955.

[6] K. Nikolic, A. Sadek, and M. Forshaw, "Fault-tolerant techniques for nanocomputers," *Nanotechnology*, vol. 13, pp. 357–362, 2002.

[7] G. Roelke, R. Baldwin, and D. Bulutoglu, "Analytical Models for the Performance of von Neumann Multiplexing", *Nanotechnology, IEEE Trans. on*, , vol. 6, pp. 75–89, 2007.

[8] A. Dehon *et al.*, "Nonphotolithographic Nanoscale Memory Density Prospects", *Nanotechnology, IEEE Trans. on*, vol. 4, pp. 215–228, 2005.