Trends in Tests and Failure Mechanisms in Deep Sub-Micron Technologies

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Abstract: *The increasing integration density of semiconductor devices and the usage of new materials and innovative manufacturing techniques result in introducing new and gradually changing the types of failure mechanisms and defects that take place in manufactured silicon. This is particularly true for current deep sub-micron manufacturing technologies. As we approach the nanoscale domain, new types of fault models and test methods are needed to cope with the increasing complexity of the observed faulty behavior. This paper discusses the latest trends in testing and failure mechanisms in all stages of IC production.*

1 Introduction

As silicon integration continues its relentless pace according to the premise of Moore's low, and as we get ever closer to the nanoscale fabrication domain, new and previously unknown failure mechanisms are being observed that need special analysis and modeling techniques. At the same time, the quality requirements on *integrated circuits (ICs)* has risen significantly in the past few decades to levels approaching zero *DPM (defect per million)* for special mission critical applications, such as those in the automotive industry. As a result, close attention should be given to follow the trends of new failure mechanisms in order to prevent them from becoming the bottlenecks in tomorrow's ICs.

This paper identifies some of the latest trends observed in the semiconductor industry in terms of testing and failure mechanisms as a result of sensitivities in the manufacturing process. The paper also analyzes these trends and proposes ways to deal with the them, along with proper methods to tackle the latest challenges.

The paper is organized as follows. Section 2 starts with a classification of the latest trends in testing and failure mechanisms, and discusses the testing trends developing in the IC production process as a whole. Section 3 identifies the testing and failure trends resulting from new directions in IC design. Then, Section 4 evaluates how testing is impacted and what new failure mechanisms are expected to result from the latest manufacturing techniques. Section 5 shows how the testing practice itself is changing as a result of recent IC developments and requirements. Finally, Section 6 ends with the conclusions.

2 Trends in IC production

In order to successfully bring an IC to the market, production has to go through a number of important stages that ensure the functionality and quality of the product. Figure 1 gives a simplified description of the typical production stages of an IC today.

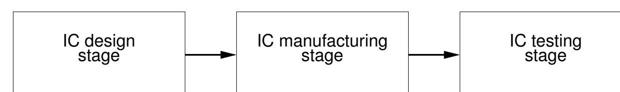

Figure 1. Simplified flow of IC production process

The figure shows three main stages: the IC design stage, the IC manufacturing stage and the IC testing stage. As scaling continues and new issues arise in the production process, the challenges for the stages in this figure change, both within each of the three individual blocks, and for the integrated IC production process as a whole. In the following, we describe a couple of trends that involve the production process in general.

2.1 Fragmentation of IC production

One of the trends observed for the integrated production process is the gradual fragmentation of the different stages across multiple companies, rather than being carried out by a single semiconductor giant. This makes it possible to have smaller, specialized and rather dynamic companies that closely focus on one aspect of the semiconductor industry or the other.

Many *fabless* design firms are being established, which sell their circuit designs in the form of *intellectual property (IP)* components to other parties, that would in turn

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integrate them into their designs. In addition, so-called *foundries* (such as the Taiwanese Semiconductor Manufacturing Company or TSMC) are replacing expensive company-owned manufacturing fabs. Also, test houses are fulfilling the task of ensuring the functionality and quality of manufactured ICs, thereby replacing in-house testing facilities.

This trend helps companies to overcome the huge investments needed to produce todays top-end semiconductor products. As the cost of the production process continues to increase, this trend is expected to accelerate in two different ways:

- New, more specialized IC production stages will be realized that handle every aspect of the industry from technology research to product specification, design, manufacturing, testing, marketing and sales [Vermeulen04].
- Bigger semiconductor companies will increasingly partner with others in specific fields (research, fabrication, etc.) to muster the heavy investments needed for future technologies [McGregor03].

This trend makes it necessary to have industry-wide standards in order for the different companies to exchange information. In term of testing, standardized test description languages and specialized test data management protocols are needed to facilitate upstream and downstream communication in the IC production flow.

2.2 Value-added testing

The second trend is the usage of testing information not only to screen defective products from reaching the customer, but also to provide feedback to the manufacturing process and/or design process to prevent the defects from occurring in the first place [see Figure 2]. This approach is called *value-added testing* since it provides a way to increase the value of the performed testing by improving manufacturing yield levels and increasing profitability. This, however, comes at an increased price for testing, since test feedback is only possible with the application of more complex diagnostic testing rather than the simpler detection testing.

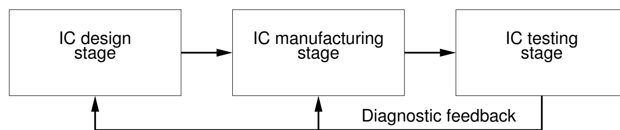

Figure 2. Using diagnostic feedback information from the test stage

Value-added testing techniques have been in use by leading silicon manufacturers for a long time [Al-Ars05], where cutting-edge fabrication processes start off with relatively low yields and with many systematic defects. These processes are gradually modified to increase yield (in a procedure referred to as *yield learning*) using diagnostic information from test application [Jahangiri05]. This yield learning process is expected to be increasingly used even in older, well-established manufacturing processes to push yield levels even higher.

In addition to the above mentioned trends that impact the IC production process as a whole, each of the three stages in Figure 1 has its own trends, as discussed next.

3 Trends in IC design

Market demands coupled with the extra amount of transistors available for designers today have tilted the design process to adopt new, challenging design techniques that increase the complexity of both the designs themselves as well as their testing process. In the following, a number of these new design-related trends are discussed and their impact on testing is identified. Figure 3 shows a classification of these trends.

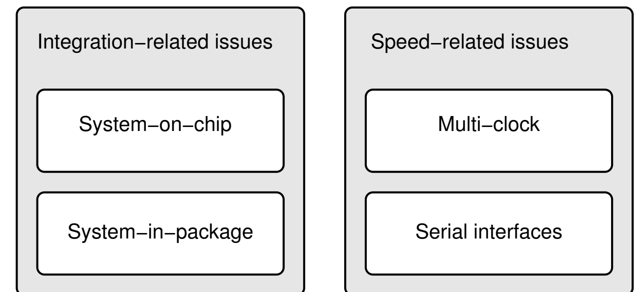

Figure 3. Classification of design-related trends

3.1 System-on-chip integration

The concept of *systems-on-chip (SOCs)* has developed as a result of the need for higher processing power and for hardware integration levels much greater than could be offered by integrating discrete components on a *printed circuit board (PCB)* [Bergamaschi02]. The SOC market is expected to grow significantly in the coming years fueled by the boom of various Internet applications in the home and office wireless environments. In general, three types of circuits can be distinguished on an SOC: logic (e.g., for control and data processing), memory (e.g., for data storage), and analog (e.g., for digital-analog conversions). Each of these components have their own testing requirements, and have dedicated types of *automated test equipment (ATE)* that cater for these requirements. This means

that SOCs cannot relay on using a specific kind of ATE optimized to test a particular type of circuits. There are two different possible solutions: either using *design-for-testability (DFT)* techniques to enable a single tester of testing different cores, or using multiple ATE benches to perform the necessary testing. The first solution costs on-chip silicon area, while the other needs investment in multiple specialized ATE. Depending on the relative cost of each solution and the expected device volume, the most cost effective alternative should be chosen. Besides the ATE issue, there is the problem of *electromagnetic compatibility (EMC)* where components should be used that do not electrically interfere with each other.

3.2 System-in-package integration

When the manufacturing technology of the different components to be integrated on an SOC are incompatible with each other, the concept of *systems-in-package (SIPs)* becomes a more attractive alternative. SIPs are made by stacking a number of different chips on top of each other and bonding them into one single package in a technique called *stacked-die packaging*. One famous application for SIPs is stacking a chip manufactured in a logic technology along with a chip manufactured in a memory (particularly DRAM) technology. These two technologies are incompatible, and manufacturing both devices on the same chip requires a tradeoff between performance and silicon area. These two technologies have been successfully integrated in SIPs for the cellphone handset market [Wilson03].

The main test challenges faced by SIPs are similar in nature to those faced by SOCs. The integration of components with different test requirements into a single package, means that a number of specialized test techniques have to be used. In addition, SIPs are especially sensitive to edge bonding problems, which require special testing of the behavior at the die interface that goes beyond the simple electrical continuity test. Apart from that, SIPs suffer from a number of unique problems, which require careful attention to power dissipation from multiple chips, capacitive coupling between adjacent chips and incompatible die sizes.

3.3 Using multi-clock

A number of complex ICs require using more than one clock signal for functional or performance reasons. Especially in the telecommunications field, applications often use many complex clock structures and clock domain transitions. In these cases, the internal circuitry of the IC are divided into a number of parts, each synchronized by a different clock, each of which are then handled asynchronously. Testing for such multi-clock circuits can be very challenging due to the asynchronous nature of the circuit. This also complicates designing DFT solutions, which are needed since these circuits usually use very high clock frequencies that go beyond the capabilities of the ATE. Special DFT solutions are needed to overcome the need for a large number of test vectors, which in turn lead to long pattern generation and application times [Schmid99].

3.4 Fast serial interfaces

There is a growing tendency today toward incorporating fast serial interfaces into many ICs, a trend that transcended the traditional application of serial interfaces to telecommunications applications. These interfaces implement a specialized bus protocol to increase the data communication bandwidth both within the chip and on the interface connecting different chips. Today, speeds for these serial interfaces range from 1.5 to 3.3 Gbps (giga bits per second), with an expected future increase in bandwidth that may reach 6.4 Gbps and beyond. Testing circuits with fast interfaces involves more than using a test pattern to validate functionality. For testing circuits that use wired interfaces, measurements should be made of both voltage and timing, while for testing those using wireless interfaces frequency and power measurements are needed. In addition, ATE-based testing has some limitations when it comes to fast serial interfaces, and therefore specialized DFT techniques need to be implemented as well [Abdennadher05].

4 Trends in manufacturing

The ever changing nature of the manufacturing process and the on-going research into advanced materials and manufacturing techniques, creates trends that have a significant impact on IC testing. Below, we discuss a number of those important trends [see Figure 4]

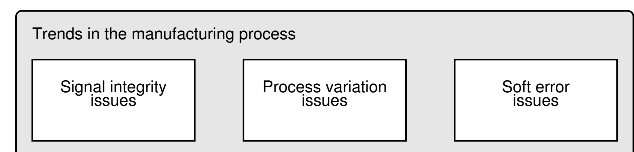

Figure 4. List of manufacturing-related trends

4.1 Signal integrity

Signal integrity refers to the general issue of ensuring that the analog voltage present on a given line correctly reflects the digital signal it represents. Several parasitic effects resulting from the continued scaling down of feature sizes

jeopardize the integrity of digital signals. Problems with signal integrity can be divided into three different types [Caignet01]:

- **Propagation delay**—this refers to the time needed for a signal to propagate through a signal line. This delay increases with shrinking line dimensions as a result of the increase in line resistances.
- **Signal interference (crosstalk)**—this refers to the noise introduced on a signal line as a result of a change in the voltage on a neighboring line. This noise increases with decreasing feature sizes as result of the increasing capacitance between adjacent lines.
- **Crosstalk delay**—this refers to the signal delay induced on a signal line as a result of the simultaneous switching of a neighboring line. This delay is positive when the two lines switch in the opposite direction, while it is negative when they switch in the same direction.

The first effect is inherent to the technology, and should be taken care of during the design stage. The other two effects are design related, and must be tested for to ensure proper functionality. A number of techniques have been proposed to deal with the signal integrity issues in current and future technologies. One of those is the generation of special test patterns that ensure the worst case crosstalk scenarios. This solution, however, requires using a large number of test vectors, which results in a large test application time. Another solution is to use on-chip noise detection circuitry that signals the development of high noise levels on specific critical signal lines [Nourani01].

4.2 Process variations

To keep the cost of the manufacturing process low, variations in a number of device parameters are tolerated. However, the continued technology scaling has introduced new variation sources and made process control more difficult. As a result, future technology nodes are expected to see increased process variations and decreased predictability of nanoscale circuit performance [ITRS03]. Process variations can be divided into two types [Cao02].

- **Intrinsic (or process) variations**—These variations are always present during circuit operation. They can either be *systematic variations* (i.e., due to known and predictable phenomena) such as changes in transistor channel length, or *random variations* (i.e., due to the inherent unpredictability of the manufacturing process) such as changes in channel doping and gate oxide thickness.
- **Dynamic (or environmental) variations**—These variations only develop temporarily during chip operation. Examples of these variations are temperature distribution or voltage levels on the chip.

These variations take effect between different chips (inter-die variations), and increasingly within a single chip (intra-die variations). Solutions to process variations include on-chip sensors that detect changes in chip behavior and compensate accordingly during chip operation. In addition, statistical timing analysis is becoming an important design tool to model and successfully design high speed circuits suffering from intra-chip process variations [Agrawal03].

4.3 Soft errors

Soft errors are intermittent faults that take place as a result of radiation particle strikes on silicon, which causes a temporary change in the voltage of the effected area. The impact of the soft error problem becomes increasingly significant with device scaling, as a result of the decreasing node capacitances and reduced voltages. *Soft error rate (SER)* values are typically expressed in *FIT (Failure in Time)*, which signifies one error in a billion hours. A FIT rate of 1000 is equivalent to a mean time to failure of 114 years. Currently, the FIT of an SRAM cell is estimated to be around 10^{-4}, while that of logic is estimated to be an order of magnitude lower at 10^{-5}. However, as shown in Figure 5, soft error rate models predict that, by 2011, the contribution of logic will surpass that of SRAMs [Shivakumar02].

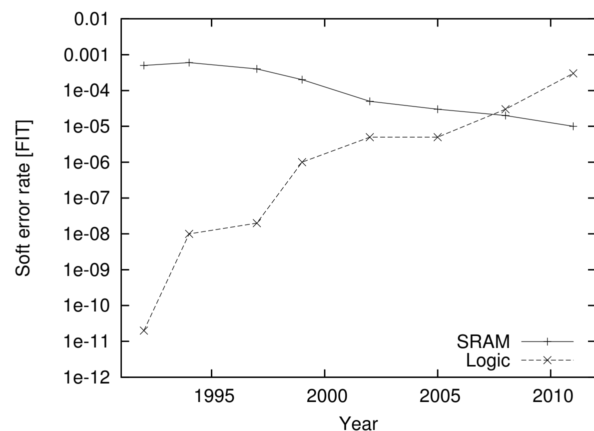

Figure 5. Trend in soft error rate for SRAMs and logic

There are a number of solutions suggested to reduce SER levels, which can be classified into three different approaches [Mukherjee05].

- **Process technology solutions**—*Silicon-on-insulator (SOI)* is a process technology that uses a much thinner

silicon layer than bulk CMOS. Therefore, SOI devices collect less charge from an alpha or neutron particle strike than bulk CMOS. IBM reports a 5x reduction in SER of SRAM devices from SOI technology. However, it is unclear whether we get similar reductions in SER from SOI logic.

- **Circuit Solutions**—It is possible to use design techniques to tune the device parameters and create radiation-hardened cells. Examples of such tuning could involve increasing the capacitance and/or supply voltage of a device. It is also possible to design circuits containing redundant states that can recover from a particle strike. However, these designs come with significant area and performance penalty.
- **Architectural Solutions**—These involve adding specialized components to analyze circuit behavior and identify potential failures. Using *error-correction-code (EEC)* circuits is one example. EEC circuits typically have lower overhead than radiation-hardened cells.[1] Today, EEC circuits are considered by the industry to be the most optimal solution for the soft error problem.

5 Trends in testing

As the complexity of the IC test process continues to increase, companies are hard at work to reduce the overall cost of manufacturing testing. In the following, we discuss the current trends in testing and the future challenges in nano-scale technologies.

5.1 Test generation

In order to generate the high-quality tests needed for todays circuits, a number of approaches are being explored and used in the industry.

- **Extending current fault models**—The fault models mainly used to generate tests are stuck-at faults, delay faults and IDDQ faults. Stuck-at faults are mainly caused by bridges as shown in Figure 6. In order to increase the effectiveness of stuck-at faults, multiple stuck-at faults are being considered, where many faults (rather than one) are considered to take place at the same time. Delay faults, on the other hand, are being refined in order to detect small timing deviations that may not always result in an actual failure. IDDQ faults are gradually becoming more analog, where not only a distinction is made between *failing* and *passing* devices, but also the exact value of the failing *current* should be measured [Vermeulen04]. New fault models are also being developed for analog and memory devices [Hmadioui04].
- **Augmenting the test set**—Test sets (i.e., sequence of test vectors) generated according to the fault coverage requirements of a given fault model are becoming gradually less effective in detecting the faulty behavior observed in modern ICs. One way to overcome this shortcoming of fault models is to augment the model-based test set with a number of hand-picked test vectors, known to detect specific types of faulty behavior. It is rather challenging to come up with a proper augmented test set, as such a set is based more on the understanding of the behavior rather than a specific fault modeling approach.
- **Using specialized tests**—Since SOCs contain memory and analog devices along with logic circuits, it is crucial to include not only logic oriented tests but also specialized tests for the memory as well as the analog parts. These specialized tests are based on their own set of fault models for each device. Here, there are two challenges to be reckoned with: first is to come up with effective specialized test sets, and second is to apply this test set properly to each device despite the restrictions one has with accessing the embedded devices [Kundu04].

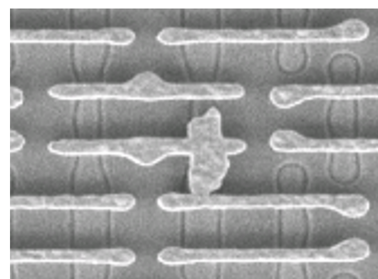

Figure 6. Example of a bridge causing stuck-at faults

5.2 Test application

In addition to the challenges that stem from generating an effective test set, there is a growing number of limitations on the way these tests are applied to the IC. Below are the main trends with this regard.

- **Tester related challenges**—As the complexity and speed of ICs increase, the complexity and speed of the testers required to test them increase accordingly.

[1]EEC circuits add an overhead of 8 bits per 64 bits of data (i.e., 13%), whereas radiation hardened-cells can have an area penalty of $30 - 100\%$ depending on the aggressiveness.

The main cause for concern is the overall tester timing accuracy, where rising and falling signal edges must be controlled with continuously decreasing time intervals. With tester accuracy levels as high as 10s of pico seconds, it is unclear how this could be further increased as ICs go to higher frequencies. An accompanying problem is the increasing cost of these specialized top-end testers. The cost aspect has gradually resulted in a move toward so-called *structural testers*, where high accuracy and speed are achieved by embedded DFT circuits, thereby reducing the demands on the external tester [Crouch04]. Apart from this, very effective tester-related test approaches such as using high voltage and high temperature (so-called *burn-in*) are becoming increasingly difficult to apply since they may easily cause a failure in the device under test.

- **Challenges with DFT**—As we use more and more on-chip DFT circuits to facilitate testing, the more hurdles we face in the implementation. Scan chains and *built-in self-test (BIST)* engines are becoming increasingly difficult to implement on modern ICs. Scan chains face a number of problems, ranging from managing heat emitted by dissipated power during test to increasing time needed to perform a scan test with the increasing number of scan flipflops. One solution to this problem is to increase the number of chains, thus decreasing the length of each chain. BIST engines face the problem of performing the correct test set on the device under test. The whole test set is too large to be stored on-chip, while externally loading the test set is difficult due to power, speed and storage related issues. One solution to this problem is using a hybrid of pseudo-random BIST vectors with externally-applied tester seeds. This way, internal tests are partly controlled by the tester and driven in the right direction. In this case, it is important to choose effective tester seeds to ensure a high-quality test set [Das2000].

6 Conclusions

This paper presented the trends and challenges of testing and failure mechanisms in deep sub-micron integrated circuits. A classification has been made, based on the flow of the production process of these devices, which results in four different classes of trends: those related to the production process as a whole, those related to design, those in manufacturing and finally those in testing. The general trend is toward reducing the cost of the test process by putting as much test circuitry on-chip as possible, rather than concentrating it in a specialized external tester. This brings around its own set of challenges that need to be dealt with in the next silicon generations.

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