Influence of Parasitic Memory Effect on Single-Cell Faults in SRAMs

Sandra Irobi Zaid Al-Ars Said Hamdioui
CE Laboratory, EEMCS faculty
Delft University of Technology, The Netherlands
Email: {I.S.Irobi, Z.Al-ars, S.Hamdioui}@tudelft.nl

Michel Renovell
LIRMM-UMR C5506 CNRS. 161,
Rue Ada 34392 Montpellier Cedex 5 France
Email: renovell@lirmm.fr

***Abstract*—Parasitic node capacitance and faulty node voltage of a defective node can induce serious parasitic effects on the electrical behavior of SRAMs. This paper evaluates the impact of parasitic memory effect on the detection of single-cell faults in SRAMs. It demonstrates that detection is significantly influenced by parasitic node components; something that is often not accounted for during memory testing. Finally, it shows the impact of parasitic node components on all possible opens in the SRAM memory cell array, using node voltages from GND to V_{DD}.**

***Index Terms*—Parasitic memory effect, static faults, SRAMs.**

I. Introduction

Smaller dimensions of memory devices can elicitate different types of defects, for example spot defects - opens, shorts and bridges during the manufacturing process. For resistive opens, complex faulty behavior can be induced by the presence of parasitic components associated with the defective node.

A lot of work has been done on investigating resistive defects [1], [9], [5], [10], [7] but without considering the presence of parasitic components of the defective node. Some work also has been done on establishing the presence of parasitic memory effect in CMOS logic and SRAMs [11], [6]. However, no work has been done on analyzing the impact of parasitic memory effect on faults in SRAMs, which is the main focus of this paper.

In this paper, all possible defect positions in the SRAM cell array has been analyzed. For each defective node, the parasitic node capacitance, defective node voltage and the defect resistance are considered. This is important in order to ensure proper faults detection in the presence of parasitic memory effects. The contributions of this paper are an analysis of the impact of parasitic memory effect on single-cell static faults detection, an identification of the different parasitic components that influence fault sensitization, and a characterization of the impact of variation of the floating node voltages on the faulty behavior.

This paper is structured as follows. Section II presents the background for parasitic memory effect in SRAMs, modeling of parasitic capacitance and the targeted fault models. Section III discusses the simulation model parameters, and presents the analysis. We conclude the paper in Section IV.

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II. Background

In this section, we present a discussion on parasitic memory effect, explain the SRAM failure mechanism considering the parasitic components of the defective node, and then show how parasitic node capacitance is modeled.

A. Parasitic memory effect in SRAMs

The presence of parasitic node capacitance (C_n) in the defective node has been shown to exacerbate the faulty behavior in SRAMs [11]. It can also induce the dependence of a successive faulty node's voltage on the voltage of previous cycle(s); an effect that is known as parasitic memory effect.

In general, both the values of R_{def} as well as the parasitic capacitance C_n influence the timing behavior of the circuit, and therefore decide the eventual output of the memory. These two parameters create a space of possible (C_n, R_{def}) values, dividing the entire space into two regions: pass and fail. In [11] it has been shown that as C_n increases, the fail region expands, while the pass region decreases. This underscores the importance of C_n, and the need to account for it as an important component of the defective node. To explain the failure mechanism, we consider that the defective node (N) in the SRAM device is characterized by three important components, namely, the resistive defect (R_{def}) of the defective node, the parasitic capacitance (C_n) of the defective node, and the voltage (V_n) on the defective node.

Figure 1 shows all 18 open defect positions injected into the SRAM cell, and an example of parasitic capacitance on the defective node, assuming an open defect position R2. In the SRAM cell array, opens can be present within the cell, at bit lines (BLs) or at word lines (WLs).

Resistive opens combined with parasitic capacitance on a defective node, can modify the timing behavior of the circuit, which can cause faults. Such modified behavior can result in different faults depending on the operating faulty node's voltage, which could be in the range GND $< V_n < V_{DD}$.

B. Modeling parasitic node capacitance

To model the total parasitic capacitance (C_n) of a defective node N, the actual position of the defect is considered. For example, for the open at R2, the defect is injected between the gate of the pass transistor and WL. Therefore, the total

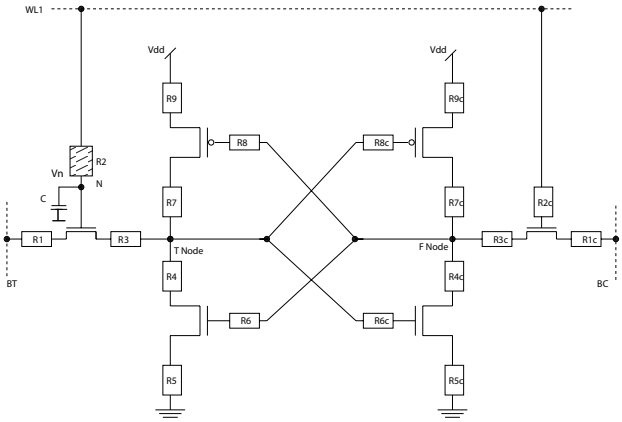

Fig. 1. SRAM cell showing R_{def} and C_n

parasitic capacitance of the defective node will comprise the *gate capacitance (C_G)* and the (wire) *line capacitance (C_L)* connecting the defect to the gate of the pass transistor. Thus, the total capacitance of the defective node is given by:

$$C_{\mathrm{n}} = C_{\mathrm{G}} + C_{\mathrm{L}} \tag{1}$$

The CMOS gate capacitance consists of the *gate-source capacitance (C_{gs})*, the *gate-drain capacitance (C_{gd})*, and the *gate-bulk capacitance (C_{gb})*, such that:

$$C_{\mathrm{G}} = C_{\mathrm{gs}} + C_{\mathrm{gd}} + C_{\mathrm{gb}} \tag{2}$$

On the other hand, the parasitic line (wire) capacitance (C_L) consists of three main components [3], as depicted in Figure 2, namely,

- *line-to-ground* capacitance (C_{lg}): This is the capacitance between a wire and ground (substrate).
- *line-to-line* capacitance (C_{ll}): This is the coupling capacitance between different wires on the same metal layer.
- *crossover* capacitance (C_{co}): This is the coupling capacitance between wires on different metal layers.

So, the total line capacitance across metal planes is the sum of these three components; that is,

$$C_{\mathrm{L}} = C_{\mathrm{lg}} + C_{\mathrm{ll}} + C_{\mathrm{co}} \tag{3}$$

C_L is a function of H, W, T and S. H is the thickness of the dielectric layer between metal layers, W is the width of the metal line, T is the thickness of the metal line and S is the spacing between the parallel lines [4], [8]. In advanced MOS technologies, the line-to-line capacitance is comparable to, or larger than the line-to-ground capacitance [3]. The exact values of the capacitances depend on the connecting wire and the manufacturing technology. C_L values used in this paper are in the range $0 < C_L < 10$fF [12], [13]. Note that other close values yield the same behavior shown in this paper.

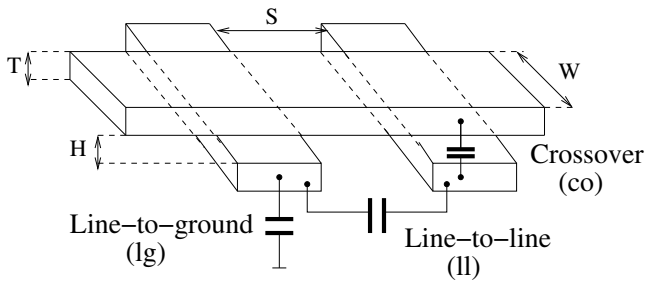

Fig. 2. Three components of line capacitance

C. Functional fault models

Functional fault models (FFMs) can be defined as a non-empty set of FPs. In this paper, single-cell static faults are targeted. Static faults are faults that are sensitized by at most one operation. These FFMs and their corresponding *fault primitives (FPs)* have been presented in [2] and are State Faults (SF), Transition Faults (TF), Word Destructive Faults (WDF), Read Destructive Faults (RDF), Deceptive Read Destructive Faults (DRDF) and Incorrect Read Faults (IRF).

III. Analysis of the Faulty Behavior

In this section, we present full analysis for one defect, and thereafter tabulate the results of the remaining defects.

A. Simulation model parameters

In this paper, an electrical Spice model of the SRAM cell (e.g., shown in Figure 1) array [11] is used for evalution. Each injected open within the cell creates a *floating node*, whose voltage varies between GND and V_{DD}, in this case 0V to 1.2V. A floating node is a memory node that is not properly controlled by a memory operation due to a defect, which leads to an improper voltage on the floating node at the end of the operation. The analysis of this behavior requires performing memory operations, while observing the impact on the cell at the true node and at the output.

R_{def} values of $0 < R_{def} < 10\mathrm{G}\Omega$ with logarithmic incremental steps of 1, 10, 100, 1000, etc., and C_L within the range $0 < C_L < 10$fF are used. Since V_n is floating, For each R_{def} value, the simulation is performed using 13 different values of V_n in the range $0.0\mathrm{V} < V_n < 1.2\mathrm{V}$, i.e., from GND to V_{DD} with incremental steps of 0.1V.

After injecting a defect, analysis has been performed by applying six operation sequences: seq = $\{1r1$ (i.e., apply read 1 to the defective cell initialized to 1), $0r0$, $1w1$, $1w0$, $0w1$ and $0w0\}$. Note that at most one operation is applied at a time; therefore the analysis is static. Only static faults can be sensitized with such analysis. Our analysis is based on observing the deviations in the electrical behavior at the output and the internal content of the cell through the true node.

B. Analysis for defect position R2c

The defect R2c is located between the WL and the gate of the pass transistor on the F-node side, with the floating node between the defect and WL. An open between WL and the gate

TABLE I
STATIC FAULTS FOR R2C F-NODE SIDE USING SEQ = $\{1r1\}$ AND SEQ = $\{0w1\}$

R2c	Defective node voltage (V_n) in Volts												
	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
10G	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	– TF_1	– TF_1	– TF_1	– TF_1	– –	– –	– –	– –	– –	– –
1G	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	– TF_1	– TF_1	– TF_1	– TF_1	– –	– –	– –	– –	– –	– –
100M	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	– TF_1	– TF_1	– TF_1	– TF_1	– –	– –	– –	– –	– –	– –
10M	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	– TF_1	– TF_1	– TF_1	– TF_1	– –	– –	– –	– –	– –	– –
1M	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	– TF_1	– TF_1	– TF_1	– TF_1	– –	– –	– –	– –	– –	– –
100k	–	–	–	–	–	–	–	–	–	–	–	–	–
10k	–	–	–	–	–	–	–	–	–	–	–	–	–
1k	–	–	–	–	–	–	–	–	–	–	–	–	–

TABLE II
STATIC FAULTS FOR DEFECTS ON T-NODE SIDE

Defect	Defective node voltage (V_n) in Volts												
	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
R1	–	–	–	–	–	–	–	–	–	–	–	–	–
R2	–	–	–	–	–	–	–	–	–	–	–	–	–
R3	–	–	–	–	–	–	–	–	–	–	–	–	–
R4	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0
R5	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0
R6	RDF_0 –	RDF_0 –	RDF_0 –	RDF_0 –	RDF_0 –	RDF_0 –	– $DRDF_1$	– RDF_1	– RDF_1	– RDF_1	– RDF_1	– RDF_1	– RDF_1
R7	–	–	–	–	–	–	–	–	–	–	–	–	–
R8	–	–	–	–	–	–	–	–	–	–	–	–	–
R9	–	–	–	–	–	–	–	–	–	–	–	–	–

of the pass transistor on F-node side will limit connectivity to the gate such that the pass transistor will not function properly. Results for this analysis are presented in Table I.

Using seq = $\{1r1\}$ in the presence of defect R2c, we observe that for C_n = 4.5fF and V_n values $0.0V < V_n < 0.2V$ the correct logic value is yielded by the sense amplifier at the output when R_{def} is in the range $1K\Omega < R_{def} < 100K\Omega$. For R_{def} = 1MΩ and above for the same V_n values, incorrect logic values are recorded at the output. However, the content of the true node shows correct logic values for all simulated R_{def} values from 1KΩ to 10GΩ. Thus, at $0.0V < V_n < 0.2V$ and for $1M\Omega < R_{def} < 10G\Omega$ at C_n = 4.5fF the cell exhibits an Incorrect Read fault IRF_1 ($< 1r1/1/0 >$). Consequently, an inspection of the BLs indicates a distortion such that the difference in potential between the true BL and the complementary BL is greatly reduced for the values where the fails occured, thereby making it hard for the sense amplifier to read the correct value from the cell.

Furthermore, at increased faulty node voltage of $0.3V < V_n < 1.2V$ we observe that no fail occurs. Again, this underscores the importance of taking into consideration the parasitic effects of the faulty node during fault detection.

Using seq = $\{0r0\}$ in the presence of R2c, we observe that this operation passes such that the sense amplifier output and the content of the true node both record correct logic 0 values for all simulated V_n values. The reason is that for a r0, only true BL is discharged while complementary BL is expected to remain approximately at V_{DD}. Thus the parasitic components of the faulty R1c node will have no significant impact on this operation.

In the same way, using seq = $\{0w1\}$, we evaluate the impact on the faulty behavior of the cell by observing the content of the true node. The results show that for V_n values in the range $0.0V < V_n < 0.6V$ when $1K\Omega < R_{def} < 100K\Omega$ the true node shows that the cell contains the expected correct logic 1 value indicating successful write transition. But, when $1M\Omega < R_{def} < 10G\Omega$, incorrect logic 0 value is observed at the true node. Thus, at $0.0V < V_n < 0.6V$, when $1M\Omega < R_{def} < 10G\Omega$ the cell exhibits the Transition Fault TF_1 ($< 0w1/0/- >$).

However, at $0.7V < V_n < 1.2V$ for all simulated values of R_{def} $1K\Omega < R_{def} < 10G\Omega$ the true node shows that the cell contains correct logic 1 and did not fail.

Using seq = $\{1w1\}$, the performed operation successfully passed and the true node shows that the cell contains the expected correct logic 1 value.

Likewise, using the operation sequences seq = $\{0w0\}$ and seq = $\{1w0\}$, both operations passed irrespective of the value of the parasitic components used. The reason is that for a write 0 despite the initial content of the cell, BT is expected to be discharged to GND, while BC is expected to remain at V_{DD}. Since R2c is positioned on the non-discharged path, its presence does not significantly influence the content of the cell to necessitate a fail.

TABLE III
STATIC FAULTS FOR DEFECTS ON F-NODE SIDE

Defect	Defective node voltage (V_n) in Volts												
	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
R1c	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1
R2c	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	– TF_1	– TF_1	– TF_1	– TF_1	– –	– –	– –	– –	– –	– –
R3c	– TF_1	– TF_1	– TF_1	– TF_1	– TF_1	– TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1
R4c	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1
R5c	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1
R6c	– RDF_1 – TF_0	– RDF_1 – TF_0	– RDF_1 – TF_0	– RDF_1 – TF_0	– – – TF_0	RDF_0 – WDF_1 TF_0	RDF_0 – WDF_1 TF_0	RDF_0 – WDF_1 TF_0	RDF_0 – WDF_1 TF_0	RDF_0 – WDF_1 TF_0	RDF_0 – WDF_1 TF_0	RDF_0 – WDF_1 TF_0	RDF_0 – WDF_1 TF_0
R7c	–	–	–	–	–	–	–	–	–	–	–	–	–
R8c	–	–	–	–	–	–	–	–	–	–	–	–	–
R9c	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	$DRDF_0$	–	–	–	–	–	–	–

C. Analysis for the other defect positions

This section summarizes the rest of the results of analyzing the faulty behavior of all open defects in the SRAM cell.

Table II lists the results for defects at the T-node side, while Table III lists results for defects at the F-node side. In both tables, the first column indicates the defect considered, while the first row lists the defective node voltages simulated. For all operation sequences performed, the detected faults are listed against the corresponding defective node voltage value at which the fault is detected. The entry '-' indicates the absence of a fault for the corresponding defect and/or defective node voltage listed.

The tables show that some faults are only observed for specific V_n and R_{def} values and not throughout the whole range of the parasitic node components. The fact that the faulty behavior depends on the different parameters of the parasitic node components underscores the importance of taking into consideration the presence of parasitic effects on the faulty node during fault detection.

IV. CONCLUSION

This paper evaluated the impact of parasitic memory effect on all single-cell static faults in SRAMs. It has demonstrated that the detection of these faults is significantly influenced by the parasitic components of the defective node and not only the resistance. Finally, it showed the impact of parasitic components for all possible opens in SRAMs memory cell array.

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