Automated Digital Circuits Design Based on Single-Grain Si TFTs Fabricated Through μ-Czochralski (Grain Filter) Process

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This paper describes a newly developed procedure to apply automated circuit design to single-grain Si TFTs fabricated through the μ-Czochralski (Grain Filter) Process. A standard cell library, which contains several basic logic cells, has been created. Every cell is designed and standardized in a full custom design style. Here a specific design rule is devised for special requirements in circuit designing based on the SG TFT technology. To automate digital circuit design, a synthesis library file describing the created cells has been generated for synthesis tools. Files for extraction and verification were also created. At the end, an 8 bit adder has been designed and the circuit behavior is demonstrated by simulation.

1. INTRODUCTION

2D location control of Si grains in excimer laser crystallization by for example, the μ-Czochralski (grain filter) process[1,2], enables formation of single-grain (SG) TFTs, which showed an average field effect mobility of more than 600 cm^2/Vs[3]. An inverter and ring-oscillator were fabricated using the SG-TFTs and showed a superior circuit performance[4]. We expect that in the future a large scale IC could be fabricated based on the SG-TFTs technology. Like any other circuits design based on traditional CMOS processes, when circuit complexities grow to a point beyond human capabilities to lay out manually, CAD tools are necessary to help designers to shorten product development time and manage the complexity of a chip having millions of logic gates or more.

In this paper, we describe a new approach to realize an automated digital circuit design based on SG-TFTs technology. A specific design rule check file was devised for special requirements in circuit design based on SG TFT technology. A standard cell library, which contains several basic logic cells, has been created in a full custom design style while taking into account several constrains in the SG-TFTs. Among them, parameterized versions of an inverter, a NAND gate and a NOR gate were designed. To automate digital circuit design a synthesis library file describing our existing cells has been generated for synthesis tools. At the end, an 8 bit adder has been designed and the circuit behavior is demonstrated by simulation based on empirical timing data.

2. DESIGN METHODOLOGY

Special features in SG-TFT Technology

The SG-TFT has a different fabrication process from the traditional MOS process, which results in some difference in circuit layout implementation. Here we will point out a few distinguished differences.

In the SG-TFT technology, the substrate surface is tiled with a grid of squared shaped single grains. Within the single grain, the silicon has single crystalline quality, in which transistors channels can be placed. The grain boundary has defects, so the transistor channel would suffer from a low mobility when the channel is on the boundary.

Secondly, in the bulk MOS or SOI technology, locations for N- and P-MOS are separated from each other using the well structures. The SG-TFTs, on the other hand, do not have such

well structure, hence, P/N channel transistors can be placed at any position, which gives more flexibility.
Another difference is that, like other TFTs, the device isolation of SG-TFTs is done by etching a way of the Si between the devices instead of the wells, the LOCOS or the trench isolation used in the bulk MOS FETs.

Approaches for automated design

Several design approaches exist in VLSI ranging from high-performance handcrafted design to fully programmable, medium-to-low performance designs. For the SG TFTs, we have chosen the standard-cells based design (CBD), since it allows one to reuse high quality cells using full custom design and also it offers a high level of automization. A detailed description of standard cell design flow is shown in Figure 1. After creating a behavior level design using a high level languages like VHDL and simulation taking into account a specification, synthesis tool will pick up proper logic cells to realize a circuit. Here we created an original cell library based on the SG-TFTs. The synthesis tool will then connect them to realize the intended function. Subsequently, placement and routing will be done automatically with specific CAD tools. Here we have created a special technology file for the SG-TFTs which is used to verify the layout.

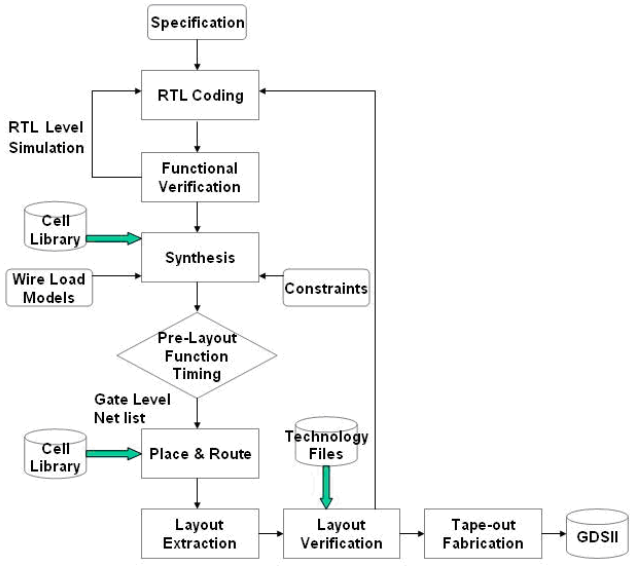

Fig. 1 Flow-chart of standard cell based design used for the SG-TFTs

After the verification of the layout, the final circuit layout would be taped out. We have used Cadence Design System for the whole procedure except Synopsys for the synthesis.

3. TECHNOLOGY DESCRIPTION

Technology files

Firstly, a technology file is created for the SG-TFTs. In the technology file, mask information is stored which defines materials and rules we use in the fabrication process. It contains the following: layer definitions; device definitions; layer, and physical- and electrical rules. For the layer definition we added two special layers into the standard CMOS technology description. Those are GF and SG, which defines the grain-filter and grain boundaries, respectively. Although the layer SG is not used for a mask in manufacturing, in the design phase it shows boundaries which limit a room within which channel should be placed. The SG layer can be designed by grow operation of the GF. For the physical rule, we have used 0.6 μm design rule with a minimum gate length of 1.5 μm and length of the single-grain of 5.9 μm. Figure 2 shows example of designed SG-TFTs inside single grain.

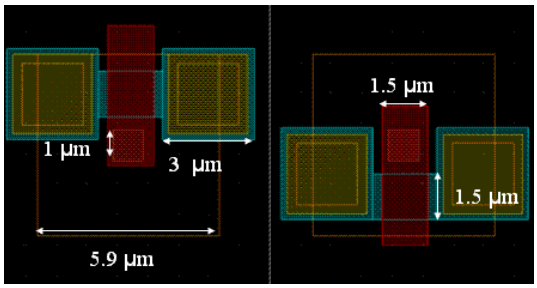

Fig. 2 Example of two isolated SG TFTs with the GF (two squares with 1μm length) and SG (two square with 5.9 μm length) layers.

Design rule checker (DRC)

The DRC checks for rules such as separation between same metal layers or a minimum width of a layer, etc. Besides those basic rules, for the SG-TFT process, a special rule was created, that is, the rule: a transistor channel must be located within the grain. an alarming is given when transistor channel fall over or out of the grain boundary.

4. STANDARD CELL DESIGN

Standard cell library

Every standard cell is designed in a full custom style and carefully characterized. We designed inverters, NANDs with 2 and 3 inputs, NORs with 2 and 3 inputs, XOR/XNOR and D flip flop. Here the ratio between channel length and width was kept at 1 while ratio of the length between the p- and n-channel SG-TFTs is kept at 2 according to the mobility difference between the two.

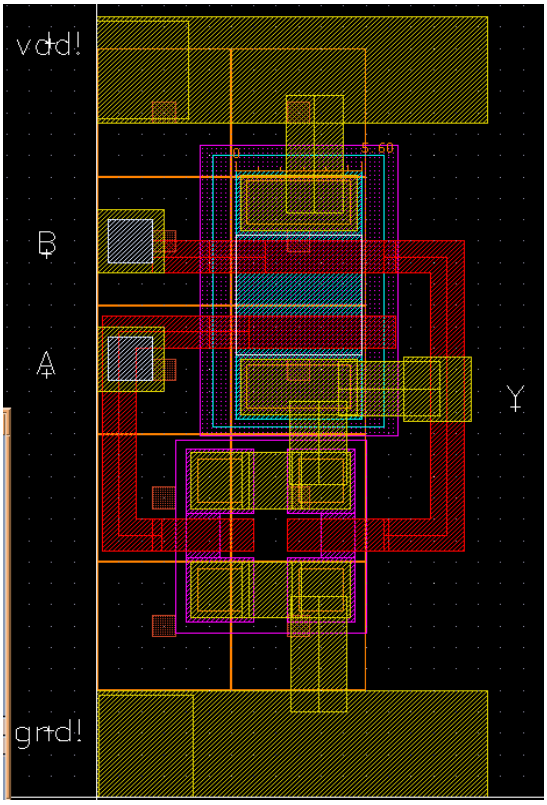

Fig. 3 Layout of 2 inputs NOR

We created also parameterized cells for 3 gates: the inverter, the 2 inputs NAND, and the 2 inputs NOR, to create all variety of sizes for a cell to realize multiple current driving strengths.

Cell verification

The created cells were verified by the aforementioned special DRC. The cells were extracted and Layout versus Schematic (LVS) check was also performed to compare the extracted netlist against the netlist described by the schematic view. Here we didn't perform Electrical Rule Checks (ERC), however basic short or open circuit problems can be alarmed during the LVS step. We used Spectre as simulator to do switch level functional check. Before simulation, a test bench and also a schematic view have to be created to provide input signals and power supply to the cell symbol. Figure 4 shows an example of the functional check simulation for the 2 inputs NOR. From the wave form, the NOR function could be verified.

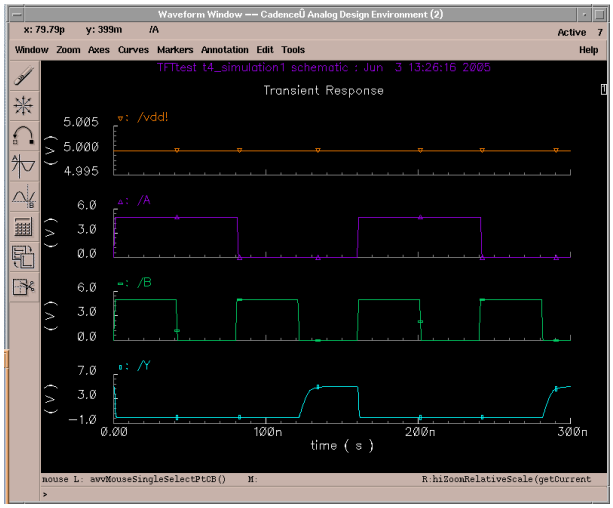

Fig.4. Simulation of the 2 inputs NOR

5. DEMONSTRATION

8-Bit Adder Design

Using the CBD with the modifications for the SG-TFTs, we demonstrated the automated design of a 8-bit adder with the flow shown in Fig. 1. First, the 8 bit adder is described in the VHDL at the RTL level. After verification, using a logic synthesis tool from Synopsys, the description was then translated into a netlist containing the logic elements of the created cell libraries.

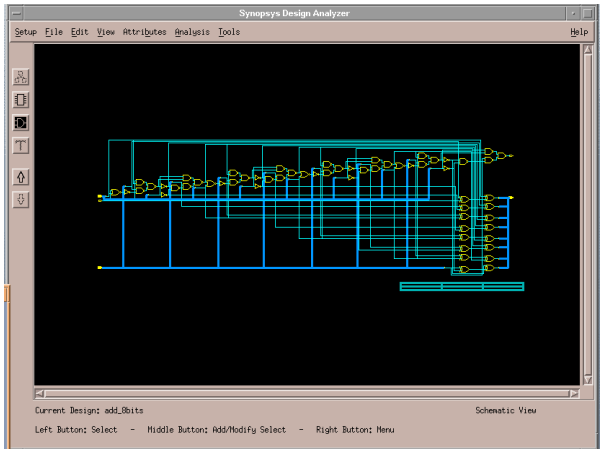

Fig. 5 Netlist of 8-bit adder

The created netlist is shown in Fig.5 with a graphical view. Then, this netlist was mapped to a layout description using placement and routing tools from Cadence. To prevent routing conflicts, We rearranged manually a few cells in over-crowed areas to make more room between them. The routing step is subdivided into 2 sub steps. Power routing aims at routing the V_{DD} and GND lines that connect all the cells. Signal routing is used to connect blocks and pins to realize the chip function. Then the layout is verified by the DRC specially made for the SG-TFTs. The LVS check was also performed. The extracted layout of the 8-bit adder is shown in Fig. 6.

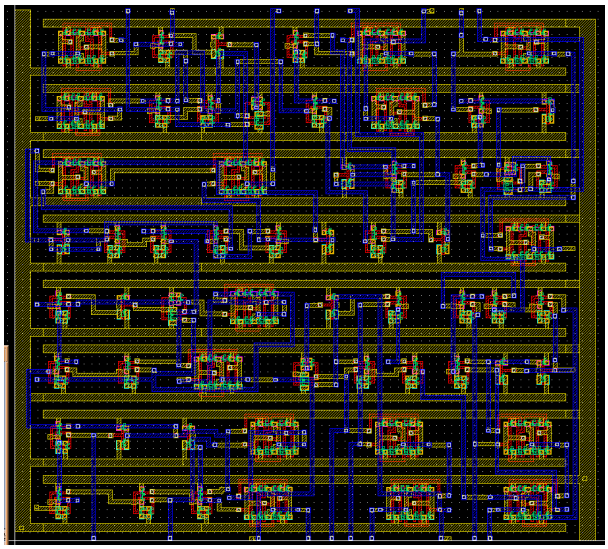

Fig. 6 The extracted layout of the 8-bit adder

We performed a functional simulation by a CMOS transistor model to verify the logic function using Spectre by Cadence. Table 1 is a truth table of the out signals of this 8 bit adder and simulated decimal value of each sum.

Table 1. Truth table of the 8 bit adder and the simulated decimal values

Index	Sum <7>	Sum <6>	Sum <5>	Sum <4>	Sum <3>	Sum <2>	Sum <1>	Sum <0>	Cout	SDeci Value
1	1	1	1	1	1	1	1	1	1	511
2	1	1	1	1	1	1	0	0	1	508
3	1	1	1	1	1	0	1	1	1	507
4	1	1	1	1	0	0	0	0	1	496
5	1	1	1	0	0	1	1	1	1	487
6	1	1	0	0	0	1	0	0	1	452
7	1	0	0	0	1	0	1	1	1	395
8	0	0	0	0	1	0	0	0	1	264

It shows that the layout of the 8 bit adder does function as described in the truth-table or, in other words, the cell does function as planned. Finally the layout was taped-out with GDSII format.

4. CONCLUSION

This paper describes a newly developed procedure to apply automated design to single-grain Si TFTs fabricated through μ-Czochralski (Grain Filter) process. An original standard cell library, which contains several basic logic cells with the SG-TFTs, has been created. Every cell is designed and standardized in a full custom design style. A specific design rule file was devised for special requirements in circuit design based on SG TFT technology. To automate digital circuit design a synthesis library file describing our existing cells has been generated for synthesis tools. Files for extraction and LVS were also created. We use some empirical timing data for a simulation. Finally, an 8 bit adder has been designed and the circuit behavior is demonstrated by the simulation. We have created an interface between design and fabrication for this new technology, so that designers need not worry about how to locate the grain filter when they design. The approach will be promising for a design of large scale ICs based on the SG-TFTs with μ-Czochralski process in future.

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