Bitline-Coupled Precharge Faults and Their Detection in Memory Devices

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Abstract: *The gradually increasing performance of memory devices increases the complexity of memory circuitry and causes new, previously unknown, failure mechanisms to take place. This paper describes a recently identified failure mechanism, observed during the design stage of a high speed DRAM. The failure mechanism is caused by the inability of the precharge circuits to set the proper voltages on memory bit lines at the end of each operation, a problem that is made even worse by the coupling effects bit lines have with each other. This paper gives a detailed analysis of this problem, and suggests effective tests to detect it. The paper also describes the results of an industrial study performed to validate the effectiveness of the new tests.*

Keywords: *DRAM testing, precharge faults, bit line coupling, defect simulation, test generation.*

1 Introduction

The processor-memory performance gap represents a major bottleneck in the overall performance of computer systems today [Mahapatra99]. This gap has led to the introduction of various DRAM I/O interfaces, each targeted to increase the access speeds for a specific type of application [Prince03]. The continuous pressure to increase the speed of memory devices puts significant demands on cutting-edge memory circuits and introduces new speed-related failure mechanisms, and redefines the importance of previously irrelevant and overlooked fails.

This paper describes a failure mechanism in high performance memory devices that stems from week precharge circuitry which, when combined with the high speed requirement, prevents setting bit lines (BLs) to proper precharge voltage at the end of every operation. This failure mechanism is made even more complex because of its sensitivity to BL coupling effects, thereby inducing failures not only on defective BLs but also in neighboring ones.

The paper is organized as follows. Section 2 starts with a description of the precharge failure mechanism, models it, and indicates how it is tested. Then, Section 3 identifies how BL coupling influences the faulty behavior induced by precharge fails. Section 4 validates the analysis using Spice simulation of the faulty behavior and suggests a test for it. This section also shows the results of including the proposed test into the manufacturing test flow of high speed DRAMs. Finally, Section 5 ends with the conclusions.

2 Description of the problem

The bitline-coupled precharge failure mechanism was first identified when a large mass of test results revealed a correlation between the failure of read operations performed with alternating logic values and the maximum BL voltage (V_{dd}). Figure 1 shows a plot of this correlation. The x-axes represents the maximum BL voltage (V_{dd}), while the y-axes represents the fail count of read operations performed along BLs (i.e., in the fast x direction) with alternating logic values in the cells (i.e., with a checkerboard of row stripes data backgrounds).

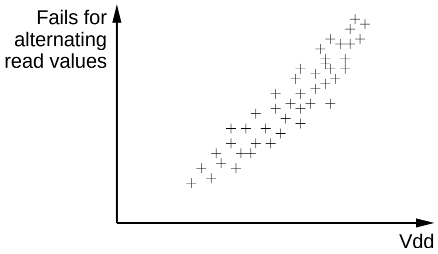
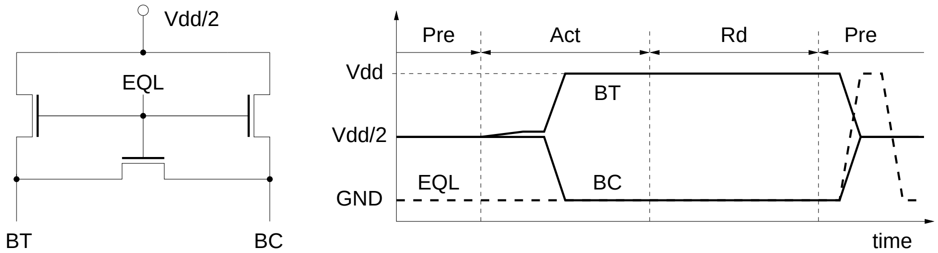


Figure 1. Experimental correlation showing precharge faults.

The correlation in the figure shows that the memory finds it difficult to read alternating values from memory



(a) Precharge circuits (b) Voltage signals

Figure 2. Precharge circuits and their functionality.

cells when these read are performed along the same BLs. This indicates that the memory suffers from a precharge problem that prevents the BLs from being fully equalized before the following operations are performed.

Figure 2(a) shows a typical electrical schematic of the precharge circuits, where the true bit line (BT) and the complementary bit line (BC) are connected to each other and to the voltage $\frac{V_{dd}}{2}$ through 3 transistors, controlled by the equalize signal (`EQL`). Figure 2(b) shows the different stages of a typical read operation, and the way the `EQL` signal is used to precharge and equalize the BLs. The read operation starts with an activation (Act) stage, where the cell is accessed and a small differential voltage develops between BT and BC. This differential voltage is amplified by the sense amplifier to the full cell voltage. Then the read (Rd) stage forwards the sensed voltage to the output, and finally the precharge (Pre) stage resets the voltages on BT and BC to $\frac{V_{dd}}{2}$.

A precharge problem can be modeled electrically by a weak equalization transistor in the precharge circuitry. Figure 3 shows the precharge circuits where the fault is modeled as an increased threshold voltage (V_t) in the equalization transistor. This increased V_t prevents the `EQL` signal from setting the proper BL equalization voltage on both BT and BC. This happens since precharging is mainly done through the equalization transistor by short-circuiting the high (low) voltage on BT with the low (high) voltage on BC. The other two precharge transistors are needed to ensure reaching the exact $\frac{V_{dd}}{2}$ voltage on both BLs, and to accelerate the precharge process.

In order to detect this kind of faulty behavior, it is important to perform a sequence of read operations on all memory cells in the fast x direction using an alternating data background (DB), such as row stripes DB or checkerboard DB. Such a test could have the following form $\{\Updownarrow_x(w0);\ \Updownarrow_x(r0);\ \Updownarrow_x(w1);\ \Updownarrow_x(r1)\}$ with the row stripes or checkerboard DB. This is simply a variant of the scan test which is usually performed at the beginning of almost any memory test flow.

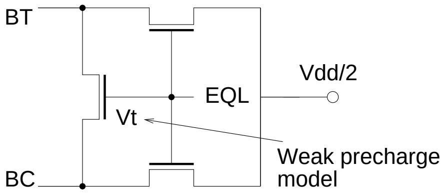


Figure 3. Electrical modeling of precharge faults.

3 Contribution of BL coupling

Due to the high speed of the memory product in question, simply applying the scan test variant described above does not succeed in detecting the DRAMs known to have faulty precharge circuits. The faulty behavior shows to be not only dependent on the value of the previous operation on the failing BL, but also on the value of the previous operation on neighboring BLs. This indicates that BL coupling plays a role in precharge failures. Previous published work in the literature indicates the importance of BL coupling in influencing the behavior of memory devices and as a case of memory fails [Konishi89, Redeker02].

Figure 4 shows how to model BL coupling effects using capacitances (C_{bb}) placed between different BLs [Al-Ars04]. The model contains three BL pairs, denoted as BLt for top (with true BTt and complement BCt lines), BLm for middle (with true BTm and complement BCm lines), and BLb for bottom (with true BTb and complement BCb lines). The BLm pair is considered the one with the faulty precharge circuitry, and the cells connected to it are inspected for faulty behavior. The model also has 6 cells connected to two WLs, three to WL0 and the other three to WL1. We consider the faulty behavior in the cell connected to BTm and WL1.

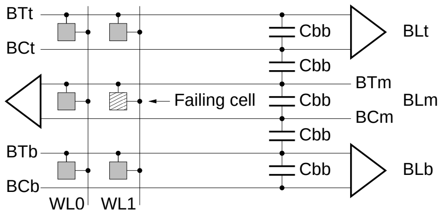


Figure 4. Three BL pairs used to model BL coupling.

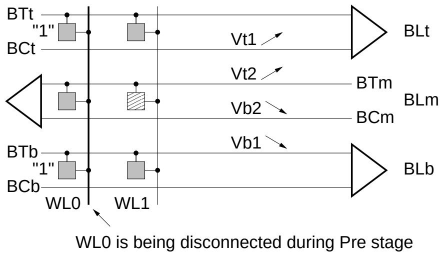


Figure 5. Effects of BL coupling on precharge faults.

BL coupling results in developing small coupling voltages on adjacent BLs, which influences proper sense amplifier operation. From a testing point of view, it is important to understand how previous operations and the currently accessed cells influence the voltage on the BLs connected to faulty precharge circuits. This way, the best test can be generated by writing the worst-case neighborhood voltages in neighboring cells.

With the faulty precharge circuits, BL coupling influencing sensing the proper cell voltage in the two operation stages before sensing takes place: the Pre stage of the previous operation, and the Act stage of the current operation [see Figure 2(b)]. We consider that the Pre stage is being performed on the cells connected to WL0, while the Act stage is being performed on cells connected to WL1. In the following, the influence in these two stages is discussed in detail.

3.1 BL coupling during Pre

Figure 5 gives a graphical representation of the coupling effects of the precharge history in the neighboring cells of a defective BL pair. We consider that the Pre stage is being performed on the cells connected to WL0. We assume that the cell accessed on BTt and WL0 contains a logic 1 and the cell accessed on BTb and WL0 contains a logic 1. As soon as WL0 is disabled, the precharge phase of the operation starts by enabling the `EQL` signal in the precharge circuitry [see Figure 3]. Since the accessed cell on BTt has a value 1, the precharge phase pulls the voltage on BCt high by an amount of V_{t1} to $\frac{V_{dd}}{2}$; this is indicated by the up-arrow next to V_{t1} in the figure. As a result of C_{bb}, the voltage on BTm is also pulled by an amount of V_{t2} to a higher level; this is indicated by the up-arrow next to V_{t2} in the figure. This voltage change promotes sensing a *logic 1* in the victim[1].

In the same way, since the accessed cell on BTb has a value 1, the precharge phase pulls the high voltage present on the BTb low by an amount of V_{b1} to $\frac{V_{dd}}{2}$; this is indicated by the down-arrow next to V_{b1} in the figure. This in turn pulls the voltage on BCm by an amount of V_{b2} lower, as indicated in the figure, which promotes sensing a *logic 1* in the victim cell.

In conclusion, if an accessed cell has a value c then the worst-case precharge background would be $\bar{c}$ in the both cells connected to the BLs above and below the failing cell. For the cell connected to the same faulty BL, the worst-case precharge value should also be $\bar{c}$. In other words, the best test conditions for testing BL-coupled precharge faults is achieved using the following worst-case precharge data background (DB): $\bar{c}_{a_t}\bar{c}_{a_m}\bar{c}_{a_b}$ (i.e., the aggressor cells on BTt, BTm and BTb should contain the value $\bar{c}$).

3.2 BL coupling during Act

During the activation stage (i.e., when WL gets activated), BL coupling causes two different coupling effects that influence the sensing of the cell voltage. These two different coupling effects are pre-sense coupling and post-sense coupling [Al-Ars04]. Figure 6 gives graphical representations for both cases. The figure assumes that WL1 is being accessed, which means that the cell connected WL1 and BLm is the failing cell, while the cells connected to WL1 and BTt and BTb the neighborhood of the failing cell. The cells are assumed to contain logic 1.

Pre-sensing effects

As soon as WL1 is accessed, the cell on BTt starts to pull the voltage on BTt by an amount of V_{t1} to a higher level; this is indicated by the up-arrow next to V_{t1} in the figure. As a result of BL coupling, the voltage on BCt is also pulled by an amount of V_{t2} to higher level; this is indicated by the up-arrow next to V_{t2} in the figure. Finally, as a result of BL coupling between BCt and BTm, the voltage on BTm is pulled higher by an amount of V_{t3}, which promotes sensing a logic 1 in the victim; this is indicated by the up-arrow next to V_{t3} in the figure. In the same way,

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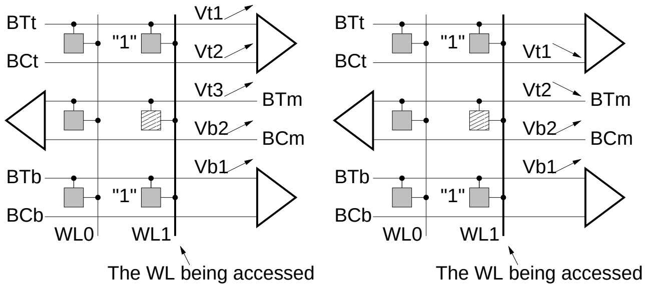
[1] The increase in the voltage on BTm further results in an increase in the voltage on BCm, but this effect is an order of magnitude less and is therefore negligible



(a) Pre−sensing (b) Post−sensing

Figure 6. Effects of (a) pre-sense and (b) post-sense coupling.

as soon as WL1 is accessed, the cell on BTb starts to pull the voltage on BTb by an amount of V_{b1} to a higher level, which in turn pulls the voltage on BCm by an amount of V_{b2} higher. This increase in the voltage on BCm promotes sensing a *logic 0* in the failing cell. In conclusion: the worst-case pre-sensing DB is either $1_{a_t}0_v0_{a_b}$ or $0_{a_t}1_v1_{a_b}$ (in short $\bar{c}_{a_t}c_vc_{a_b}$). This means that if the cell on WL1 and BTm contains the value c, then the worst case is when the cell on WL1 and BTt contains $\bar{c}$ and the cell on WL1 and BTb contains c.

Post-sensing effects

Once the sense amplifier is activated, and since the cell on WL1 and BTt contains 1, the sense amplifier pulls the voltage on BTt high while the voltage on BCt is pulled low by an amount of V_{t1} [see Figure 6(b)]. As a result of BL coupling, the voltage on BTm is pulled low by an amount of V_{t2}, which promotes sensing a logic 0 in the failing cell. In a similar way, once the sense amplifier is activated, and since the cell on WL1 and BTb contains a 1, the sense amplifier pulls the voltage on BTb high by an amount of V_{b1} as indicated in Figure 6. As a result of BL coupling, the voltage on BCm is also pulled high by an amount of V_{b2}, which promotes sensing a logic 0 in the victim cell. In conclusion: the worst-case post-sensing DB is either $0_{a_t}0_v0_{a_b}$ or $1_{a_t}1_v1_{a_b}$ (in short $c_{a_t}c_vc_{a_b}$). This means that if the cell on WL1 and BTm contains the value c, then the worst-case DB is when the cell on WL1 and BTt contains c and the cell on WL1 and BTb contains c as well.

Comparing the two results of pre and post-sensing, we find that each requires a different DB to ensure the worst-case sensing condition. It is possible to use a memory test that covers both DBs to ensure covering the worst-case condition. But to reduce test time, a single worst-case DB is needed, and therefore we should identify whether pre-sensing or post-sensing is more dominant.

4 Industrial evaluation

This section presents the results of a Spice-based evaluation of the BL-coupled precharge failure mechanism. A test is presented to detect this faulty behavior, and the results are discussed of implementing this test in the test flow of a recent memory in Infineon Technologies.

4.1 Modeling the defect

In order to simulate the faulty behavior of the memory, it is important to model the failure mechanism to be analyzed and the analysis objective. [see Figure 7].

1. **Failure mechanism**—The failure mechanism to be analyzed takes place in the precharge devices of a specific bit line pair (BL pair), resulting in weak precharge devices that fail to properly set the BLs to the correct precharge voltage, which leaves true and complement bit lines (BT and BC) unequalized with a small differential voltage between them ($\Delta V_{BL} = V_{BT} - V_{BC}$).

2. **Analysis objective**—The objective of the analysis is to identify the worst-case data background (DB) that should be used in the two BL pairs adjacent to the defective BL pair.

This failure mechanism is difficult to detect since it takes place in a rather fast memory design, which means that it is not possible to use the traditional approach of inducing a fail in defective memories by increasing the test stress (for example, by reducing the write time), since such a stress would result in failing all devices, both defective and functional. Therefore, to make the tests more selective in failing defective memories, other ways are needed to induce a fail that are more closely associated with the defect in the precharge devices. In this case, we choose to use the worst-case data in 3 different DB cells during the precharge stage of the previous operation, and 2 cells during the activate stage of the current operation.

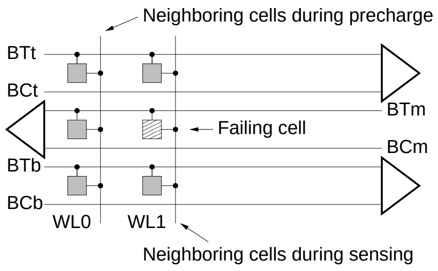


Figure 7. The defective BL pair and its DB.

Simulating this failure mechanism is done using a design validation model used during the design of memory circuits. Simulations performed on this model show that it takes 2 minutes to simulate 1 nanosecond of memory operation, which is relatively long. But since we are only interested in analyzing one failure mechanism (the weak precharge circuits problem), the investment in simulation model reduction is not justified. Therefore, the original design validation model is used for the simulations. The model contains a number of BL pairs, but for our analysis we take one BL pair as the defective one, and consider two other BL pairs (two above and two below) as the DB in the analysis. These relevant BL pairs are shown in Figure 7.

The following step in the fault analysis process is to electrically model the failure mechanism, and inject it into the memory model. This failure mechanism can be modeled by an increased threshold voltage (V_t) of the equalization device, as shown in Figure 8. The increase in V_t models the weakness in the equalization device.

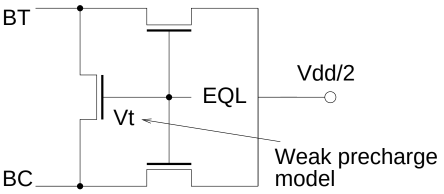


Figure 8. Modeling of the weak precharge circuits problem.

The next step in the fault analysis process is performing the simulations according to the guidelines of a fault analysis method suitable for the memory under analysis. Since we are dealing with a DRAM, the simulation employs the concept of the result planes and the V_{cs} curves previously used to analyze the faulty behavior of DRAMs [Al-Ars02].

4.2 Simulation results

Spice simulation has been effectively used in the past to evaluate the faulty behavior of memory devices [Naik93]. The Spice simulation of the faulty behavior in this paper is done in two steps: first, simulation of the worst-case precharge DB is simulated, then the worst-case DB during sensing is identified.

Precharge DB

Figure 9 shows the result plane associated with the faulty behavior of the weak precharge circuits for a range of V_t values. The x-axis of the result plane represents the value of the voltage within the cell (V_c), while the y-axis represents the change in the threshold voltage of the equalization device (ΔV_t). The result plane shows 8 different V_{cs} curves with 3 DB values, organized from left to right at the bottom of the figure with the same order listed in the legend. There is a ninth V_{cs} curve to the right of all other curves with 5 DB values. This curve will be discussed later. The V_{cs} curve is the *cell-sense threshold voltage*, which is the cell voltage at which the sense amplifier distinguishes a 0 from a 1. This means that if a read operation is performed when $V_c > V_{cs}$ then the sense amplifier detects a logic 1 in the failing cell, while $V_c < V_{cs}$ results in sensing a logic 0 in the failing cell. Therefore, the leftmost V_{cs} curve is associated with the worst-case DB for detecting a 0, while the rightmost V_{cs} curve is associated with the worst-case DB for detecting a 1.

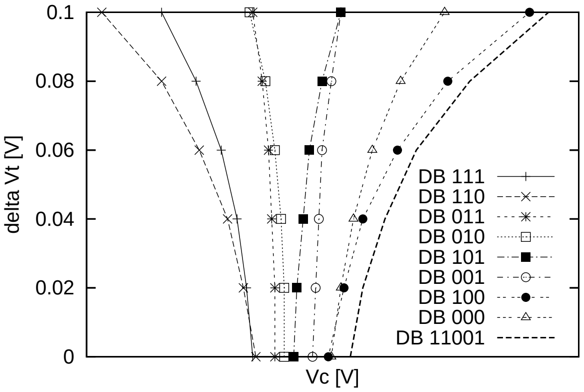


Figure 9. V_{cs} curves for all possible precharge DBs.

Figure 9 shows that the V_{cs} curves are clearly divided into two main groups, and as the threshold voltage of the equalization device increases, 4 curves with DB $x1y$ diverge to the left, while the other 4 curves with DB $x0y$ diverge to the right ($x, y \in \{0, 1\}$). This result can be explained by noting that if the cell in the precharge DB on the defective BL contains a 1, then a faulty equalization device would fail to fully equalize the BLs, leaving a slight bias against sensing a 0. As V_t increases, the equalization ability of the precharge device decreases, and the bias against sensing a 0 increases, which makes the V_{cs} curves diverge to the left. Using a similar argument, one can explain why the other 4 V_{cs} curves diverge to the right.

Inspecting the curves at bottom of the figure, shows that the worst-case precharge DB for sensing a 0 is 111, while the worst-case precharge DB for sensing a 1 is 000. This result validates the theoretical analysis performed in Section 3, where the same worst-case precharge DBs have been proposed. This situation changes as ΔV_t increases, as one moves to the top of the figure. The V_{cs} curves at top of the figure indicate that the worst-case DB for sensing a 0 is

110, while the worst-case precharge DB for sensing a 1 is 100. These results are not justified by the theoretical analysis in Section 3, which means that the simple model used in that section to derive the worst-case DBs is not always enough to identify the worst-case precharge DBs.

Since there is no single V_{cs} curve with 3 DB values that remains the worst-case throughout the range of simulated V_t, we attempted to simulate the coupling effect of more BLs in order to find out the worst-case DB. When 5 DBs were simulated, a clear worst-case V_{cs} curve appeared at the rightmost side of the figure with the DB 11001. This curve remains the worst-case condition for sensing a 1 throughout the range of simulated ΔV_t.

Sense DB

A similar simulation experiment has been carried out in order to identify the worst-case DB when sensing takes place. As discussed in Section 3, there are two different, partially opposing, coupling mechanisms taking place during sensing. Using a simulation-based analysis, the worst-case DB has been identified. The analysis shows that the worst-case DB for detecting a 0 in the failing cell is 0 in the cell on BTt and 0 in the cell on BTb (i.e., using the DB 000), while the worst-case DB for detecting a 1 in the failing cell is 111. In other words, a worst-case DB of ccc is needed, which means that the post-sense coupling effect is prevalent for the simulated memory model according to Section 3. Further analysis of the behavior using more DB cells indicates that the worst case DB should still be $ccccc$.

4.3 Implementation results

Based on the Spice simulation analysis, a test experiment has been applied to validate the findings of the analysis above. The experiment used 200 different memory component, with 180 of them assumed to have the weak precharge circuits problem, while the remaining 20 are known to be perfectly functional. On each one of these components, 16 different tests have been applied, each with a precharge DB from $xy0zw$ where $x, y, z, w \in \{0, 1\}$. The tests also attempted to sense a 1 from every cell with an all 1s sense DB after writing the precharge DB in the previously accessed cells, then precharging. In other words, the following tests have been applied $\{\Uparrow(w11111);\ \Uparrow(wxy0zw, r11111)\}$, where $x, y, z, w \in \{0, 1\}$.

The results show that out of the 180 known defective components, 178 components failed at least one applied test, while 2 components escaped all performed tests. It is possible that these 2 components have a different defect that is not related to the weak precharge circuits problem, which results in a different faulty behavior from the expected one. From the 20 known functional components, none failed any of the applied tests. The experiment showed that only the DB 11001 has been able to detect all the 178 failing components, which means that this DB is the most effective precharge DB to detect the faulty behavior. This is exactly the same precharge DB the simulation-based failure analysis predicted to be the most effective.

5 Conclusions

In this paper, a BL-coupled precharge failure mechanism is described, which has been observed during the design stage of a high speed DRAM. The failure mechanism is caused by weak precharge circuits, and is influenced by BL coupling effects. In order to detect this failure, two different worst-case data backgrounds (DBs) should be used: a precharge DB (during the precharge stage of the previous operation) and sense DB (during the sense stage of the failing read operation). A simulation-based analysis showed that the worst-case precharge DB to be 11001, while the worst-case sense DB to be 11111. A test to detect the weak precharge problem has been implemented, and the results indicate clearly that the DBs suggested by the simulation approach are the most effective possible DBs for this problem taking place in this specific memory design.

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