Short Papers

Influence of Bit-Line Coupling and Twisting on the Faulty Behavior of DRAMs

Zaid Al-Ars, Said Hamdioui, Ad J. van de Goor, and Sultan Al-Harbi

***Abstract*—With the continued advances in miniaturization, bit-line (BL) coupling is becoming ever more influential on the memory behavior. This paper discusses the effects of BL coupling on the faulty behavior of defective dynamic RAMs. It starts with an analytical evaluation of coupling effects, followed by a simulation-based fault analysis using a Spice simulation model. Two BL coupling mechanisms are identified (pre-sense and post-sense coupling), which are found to have a partly opposing effect on the faulty behavior. It is shown that BL coupling causes a special kind of coupling fault between adjacent memory cells. In addition, the influence of BL twisting on the faulty behavior of the memory is analyzed and simulated. The results indicate strong correspondence between theory and simulation and show the importance of Spice simulation as a vital tool for fault analysis.**

***Index Terms*—Bit-line (BL) coupling, BL twisting, defect simulation, dynamic RAM (DRAM), fault analysis, memory testing.**

I. Introduction

The long narrow bit-line (BL) structures running in parallel on the surface of a memory chip are particularly prone to relatively large amounts of "capacitive coupling" (or "crosstalk") noise from adjacent BLs. As the integration density of memory devices increases, the problems associated with BL coupling noise become more significant because of the weak cell signals that must be sensed reliably on these lines [12]. To reduce the impact of crosstalk on BL functionality, a number of BL twisting techniques can be implemented, so that noise cancellation can take place [5].

The issue of crosstalk in logic circuits has received much attention and was investigated in depth in the literature [6], [7]. There is also some research on BL coupling in memory devices that investigate its effect on memory operations in current and future fabrication technologies [10], [12]. However, there is not much published work on the impact of BL coupling noise on memory faults, nor of the way neighboring cells influence the faulty behavior of a victim cell.

This paper discusses the concept of BL coupling and investigates its impact on the faulty behavior of dynamic RAM (DRAMs) [3]. In addition, BL twisting techniques are analyzed to identify the way they influence this faulty behavior [4]. We start with a theoretical analysis and then use Spice simulation to analyze the faulty behavior of a defective memory. Two BL coupling effects are identified, and the way a neighborhood of cells influences BL coupling is investigated.

This paper begins with a discussion of the general concept of BL coupling in Section II, where a theoretical analysis of BL coupling is given. Section III evaluates the effects of BL coupling on the faulty behavior. Section IV introduces the simulation-based fault analysis method used in Section V to validate the theoretical analysis of BL coupling. Then, Section VI analyzes the impact of BL twisting on coupling effects and on the faulty behavior of defective memories. Section VII validates the theoretical analysis of BL twisting using Spice simulation. Finally, Section VIII ends with the conclusions.

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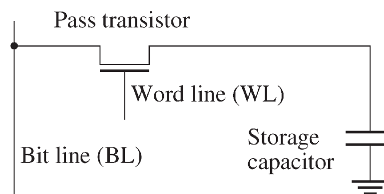

Fig. 1. Electrical schematic of a DRAM cell.

II. Concept of BL Coupling

This section introduces BL coupling using a Spice memory model, which is later used in this paper to perform the memory simulation. Fig. 1 shows a simple electrical schematic of a DRAM cell, which consists of a storage capacitor and a transistor (called "pass transistor") that acts as a switch connecting (or disconnecting) the capacitor to the BL. The word line (WL) controls the pass transistor in such a way that, during a read (r) or a write (w) operation, the cell gets connected to BL to transfer data to or from the cell. Between operations, WL keeps the cell disconnected from BL to ensure that the cell retains its data and that other cells connected to BL can transfer their data.

To limit the needed simulation time, the used simulation model has been reduced in complexity while electrically compensating removed components. Fig. 2 shows a close-up block diagram of a single folded BL pair of the three pairs to be simulated in the model. This simplified simulation model contains a 2×2 cell array with nMOS access transistors, in addition to a sense amplifier and precharge devices. The removed memory cells are compensated for by load cells and parasitic components of different values distributed along the BLs. External to the BL pair, the simulation model contains one data output buffer needed to examine data on the output and a write driver needed to perform write operations. The memory model employs Spice BSIM3v3 device parameters for the simulations.

The model contains three BL pairs, denoted as: 1) BLt for top; 2) BLm for middle; and 3) BLb for bottom, as shown in Fig. 3. Fig. 2 shows both the true (BTm) and complementary (BCm) BLs of BLm, the complementary (BCt) BL of BLt only, and the true (BTb) BL of BLb only.

The different BLs influence each other by a number of distributed coupling capacitances $(C_{bb1} + C_{bb2} + C_{bb3} = C_{bb})$. Note that BL coupling capacitances are the same whether coupling takes place within a given BL pair or between different BL pairs. This is true since all BLs on a chip are manufactured in the same way, using the same materials having the same dimensions and at the same distances from each other. Identifying a given BL as BT or BC depends solely on the way that BL is connected to the sense amplifier and not on the way it is manufactured.

The total BL capacitance C_b is made up of the sum of the BL coupling capacitance C_{bb} and the remaining capacitance C_{br}, which is not related to BL coupling but to WL coupling, substrate coupling,

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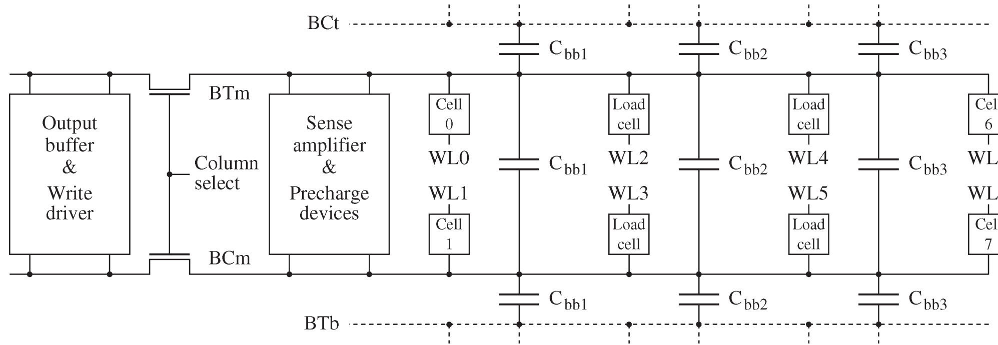

Fig. 2. Close-up block diagram of one BL pair of the three pairs used for simulation.

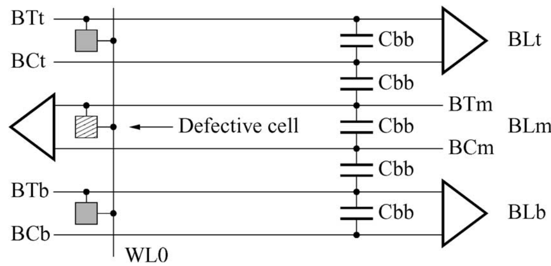

Fig. 3. Three BL pairs implemented in the simulation model.

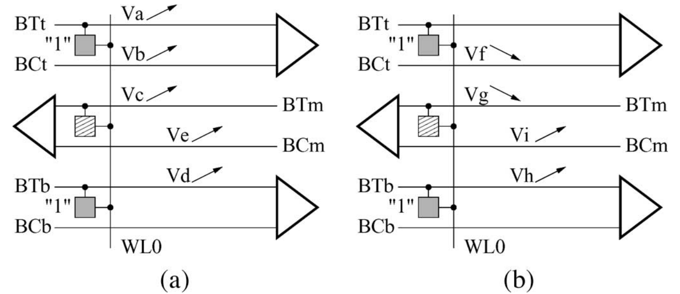

Fig. 4. Effects of (a) pre-sense and (b) post-sense coupling.

etc. In the simulation model of Fig. 2, these capacitances are related as follows:

$$C_b = C_{bb} + C_{br} = 10 \times C_{bb}. \tag{1}$$

These are typical cell array capacitances in megabit DRAMs with a folded BL pair arrangement [9], [10]. As a result of C_{bb}, two different kinds of coupling effects may take place: 1) pre-sense coupling and 2) post-sense coupling [5].

Pre-sense coupling (ΔV_1) is generated after the WL is activated and the cells are accessed, but before the sense amplifier is activated. The noise on a given floating BL results from coupling to two BLs, above and below the victim BL, on which cells are accessed. The amount of worst-case ΔV_1 developing on the floating BL relative to the full voltage V_1 developing on neighboring BLs can be approximated as [8]

$$\frac{\Delta V_1}{V_1} \approx \frac{1}{2 + (C_{br}/C_{bb})}. \tag{2}$$

This relation indicates that the amount of pre-sense coupling noise increases with increasing C_{bb} from 0 V (for $C_{bb} = 0$) to 1/2 V (as C_{bb} approaches ∞). For the used simulation parameters in (1), the worst case $\Delta V_1/V_1 \approx 1/11$.

Post-sense coupling (ΔV_2) is generated after the sense amplifier is activated and the BLs are pulled either to 0 or 1 according to the logic value sensed by the sense amplifier. The main reason for this type of noise is the time difference between sense amplifier activation and the instant the sense amplifier decides to sense a 1 or 0 (Δt). The amount of ΔV_2 can be approximated according to the following relation [5]:

$$\Delta V_2 \approx \alpha \frac{C_{bb}}{C_b^2} (\Delta t)^3 \tag{3}$$

where α is a constant that depends on a number of sense amplifier related parameters and has a value in the order of $10^{12} - 10^{13}$ FV/s^3. The relation shows the strong dependence of ΔV_2 on the time delay until the sense amplifier pulls the BLs either up or down. This means that even small delays in the sense amplifier operation can cause a relatively large amount of post-sense coupling noise.

The total amount of BL coupling noise ΔV is equal to the sum of pre-sense and post-sense coupling $(\Delta V_1 + \Delta V_2)$. Whether ΔV_1 or ΔV_2 constitutes the dominant factor in ΔV depends heavily on design-specific parameters that generally cannot be evaluated analytically, which leaves circuit simulation as the only analysis option [9].

III. Effects of Coupling

BL coupling results in developing small coupling voltages on adjacent BLs, which influences proper sense amplifier operation. From a testing point of view, it is important to understand how a specific initialization of a neighborhood of cells affects the sensing of a given victim, so that the worst case values can be written in the neighboring cells.

The model considered here (see Fig. 3) consists of three BL pairs, each with 2×2 cells, which means that the defective cell (Cell 0 on BLm) has a neighborhood of $3 \times 2 \times 2 = 12$ cells with a possible influence on the behavior. However, since the precharge operation functions properly (because we assume that the defective cell suffers from an open within the cell, which does not influence the precharge voltage on the BLs), the history of operations performed on any cell other than the defective cell does not influence the faulty behavior of the memory.[1] Therefore, the only cells able to influence the faulty behavior are those sharing the same WL with the defective cell. This means that the neighborhood consists of two cells, each containing either 0 or 1, which results in $2^2 = 4$ different data backgrounds (BGs).

The effects of BL coupling on the faulty behavior can be divided into pre-sensing effects and post-sensing effects. Fig. 4 gives graphical representations for both cases, when Cell 0 on BTt contains a logic 1 and Cell 0 on BTb contains a logic 1.

[1]On the other hand, a defective precharge circuitry would mean that the read/write history affects the faulty behavior and should be simulated.

A. Pre-Sensing Effects

As soon as WL0 is accessed, Cell 0 on BTt starts to pull the voltage on BTt by an amount of V_a to a higher level; this is indicated by the up-arrow next to V_a in the figure. As a result of C_{bb}, the voltage on BCt is also pulled by an amount of V_b to higher level; this is indicated by the up-arrow next to V_b in the figure. Finally, as a result of C_{bb} between BCt and BTm, the voltage on BTm is pulled higher by an amount of V_c, which promotes sensing a logic 1 in the victim; this is indicated by the up-arrow next to V_c in the figure.[2] From (1) and (2), the amount V_c is related to V_a by the relation $V_c/V_a = (V_b/V_a)(V_c/V_b) \approx 1/11^2$. In the same way, as soon as WL0 is accessed, Cell 0 on BTb starts to pull the voltage on BTb by an amount of V_d to a higher level, which in turn pulls the voltage on BCm by an amount of V_e higher. This increase in the voltage on BCm promotes sensing a logic 0 in the victim cell. The values of V_d and V_e are related by $V_e/V_d \approx 1/11$, which means that the cell on BTb has a much higher influence on the faulty behavior than the cell on BTt. The following conclusions are derived.

1) The worst case pre-sensing BG is either $1_{a_t}0_v0_{a_b}$ or $0_{at}1_v1_{a_b}$ (in short $\bar{x}_{a_t}x_vx_{a_b}$). This means that if Cell 0 on BTm contains the value x, then the worst case is when Cell 0 on BTt contains $\bar{x}$ and Cell 0 on BTb contains x.
2) Cell 0 on BTb has a much higher pre-sensing influence on the faulty behavior than Cell 0 on BTt.

These results indicate that the cells on BTt and BTb cause a special kind of coupling fault with the cell on BTm, although there is no direct coupling between these cells. For example, a read 0 operation $(r0)$ on Cell 0 on BTm might fail only when the state of Cell 0 on BTb is 0, but not when it is 1. This coupling effect has important implications on memory testing since it requires testing for coupling faults with two aggressors rather than only one. Almost all memory tests today are based on the assumption that only one aggressor should be taken into consideration.

B. Post-Sensing Effects

Once the sense amplifier is activated, and since Cell 0 on BTt contains a 1, the sense amplifier pulls the voltage on BTt high while the voltage on BCt is pulled low by an amount of V_f [see Fig. 4(b)]. As a result of C_{bb}, the voltage on BTm is pulled low by an amount of V_g, which promotes sensing a logic 0 in the victim cell. In a similar way, once the sense amplifier is activated, and since Cell 0 on BTb contains a 1, the sense amplifier pulls the voltage on BTb high by an amount of V_h as indicated in Fig. 4. As a result of C_{bb}, the voltage on BCm is also pulled high by an amount of V_i, which promotes sensing a logic 0 in the victim cell. Both neighboring cells have a first-order effect on the victim. The following conclusions are derived.

1) The worst case post-sensing BG is either $0_{a_t}0_v0_{a_b}$ or $1_{a_t}1_v1_{a_b}$ (in short $x_{a_t}x_vx_{a_b}$). This means that if Cell 0 on BTm contains the value x, then the worst-case BG is when Cell 0 on BTt contains x and Cell 0 on BTb contains x as well.
2) Both cells have a comparable first-order effect on the faulty behavior.

These results again indicate that the cells on BTt and BTb cause a special kind of coupling fault with the cell on BTm, which implies that tests for coupling faults should be derived where two aggressors are taken into consideration instead of one.

Comparing the two results of pre- and post-sensing, we find that each requires a different BG to ensure the worst case sensing condition.

[2]The increase in the voltage on BTm further results in an increase in the voltage on BCm, but this effect is an order of magnitude less and is, therefore, negligible.

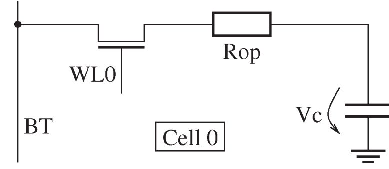

Fig. 5. Open injected into Cell 0.

It is possible to use a memory test that covers both BGs to ensure covering the worst-case condition. However, to reduce test time, a single worst-case BG is needed, and therefore, we should identify whether pre-sensing or post-sensing is more dominant.

IV. Simulation-Based Fault Analysis

This section presents the way to use Spice simulation to evaluate the faulty behavior of a defective DRAM. The analysis performed here corresponds to BLs with no coupling. This means that the coupling capacitances shown in Fig. 2 are all set to zero: $C_{bb1} = C_{bb2} = C_{bb3} = 0$.

Consider the defective DRAM cell shown in Fig. 5, where a resistive open (R_{op}) between BT (true BL) and the access transistor limits the ability to control and observe the voltage across the cell capacitor (V_c). The open is injected into Cell 0 and simulated as part of the reduced memory model shown in Fig. 2. The reasons for choosing this specific cell defect to analyze BL coupling include the following.

1) This defect models a strap connection between the drain of the pass transistor and the cell capacitor that is difficult to manufacture and may have resistive values that are higher than normal [1].
2) Gradually increasing the resistive value of this defect results in the gradual reduction of the differential BL signal needed for proper sensing. Therefore, this defect is ideal for analyzing the impact of BL coupling on the faulty behavior.
3) The relative simplicity of the defect model and the required fault analysis.

The analysis takes a range of possible open resistances ($10\ \text{k}\Omega \leq R_{op} \leq 10\ \text{M}\Omega$) and a range of possible floating cell voltages ($\text{GND} \leq V_c \leq V_{dd}$) into consideration.

Two different (V_c, R_{op}) result planes are generated: one for the write "zero" $(w0)$ operation on a cell initialized to one $(1w0)$ and one for the write "one" $(w1)$ operation on a cell initialized to 0 $(0w1)$. These result planes describe the impact of successive $w0$ and successive $w1$ operations on V_c (denoted as $(n)w0$ and $(n)w1$, respectively) for a given value of R_{op}. Write operations described here refer to single-cycle operations, where a cell is accessed, written, then disconnected, and followed by a memory precharge. Fig. 6 shows an automatically generated result plane corresponding to $(n)w0$ operations, whereas Fig. 7 shows the result plane corresponding to $(n)w1$ operations for the open R_{op} shown in Fig. 5.

A. Plane of $w0$

This result plane is shown in Fig. 6 [2]. To generate this figure, the floating cell voltage V_c is initialized to V_{dd} (because a $w0$ operation is performed), and then, the operation sequence $1w0w0 \ldots w0$ is applied to the cell (i.e., a sequence of $w0$ operations to a cell initialized to 1). The net result of this sequence is the gradual decrease (depending on the value of R_{op}) of V_c toward GND. The voltage level after each $w0$ operation is recorded on the result plane, resulting in a number of curves. The curves are numbered as $(n)w0$, where n is the number of $w0$ operations needed to get to the curve. For example, the arrows in the figure indicate that, for $R_{op} = 1000$ kΩ, a single $w0$ operation represented by $(1)w0$ pulls V_c from V_{dd} to about 1.2 V, whereas four

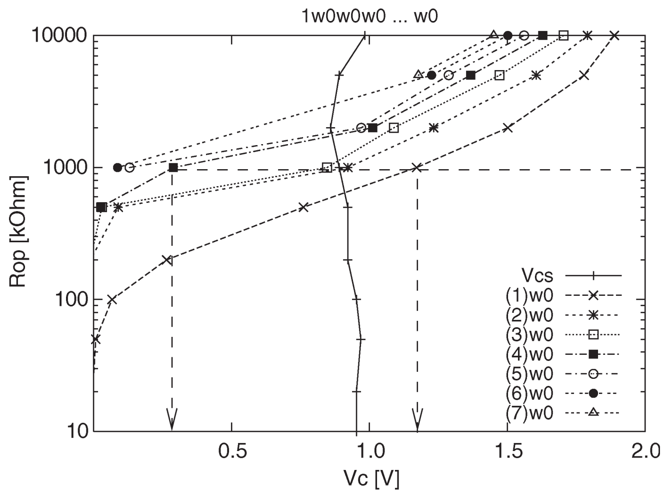

Fig. 6. Result plane corresponding to $w0$.

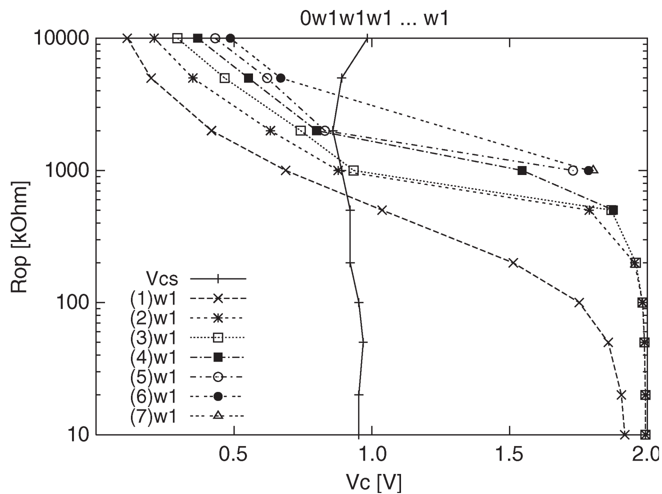

Fig. 7. Result plane corresponding to $w1$.

$w0$ operations represented by $(4)w0$ pull V_c to about 0.3 V. We stop performing the $w0$ sequence when the voltage change ΔV_c, as a result of $w0$ operations, becomes $\Delta V_c \leq 0.05$ V, which results in identifying up to seven different $w0$ curves in the plane. Initially, an arbitrary small value for ΔV_c is selected, which can be reduced afterward if it turns out that more than seven $w0$ operations are needed to describe the faulty behavior. The "sense threshold cell voltage" (V_{cs}), shown as a solid line that runs across the center of the figure, is the cell voltage "above" which the sense amplifier reads a 1 and "below" which the sense amplifier reads a 0. This curve is generated by performing a read operation for a number of V_c values and iteratively identifying the V_c border that distinguishes a 1 and a 0 on the output. V_{cs} is almost independent of R_{op} here because there is no BL coupling considered in this simulation since all BL coupling capacitances are set to zero ($C_{bb1} = C_{bb2} = C_{bb3} = 0$). The small deviation V_{cs} has from the center of the figure is due to sense amplifier imbalance and other types of coupling, such as WL–BL coupling.

B. Plane of $w1$

This result plane is shown in Fig. 7 [2]. This result plane is generated in the same way as the result plane of $w0$. First, V_c is initialized to GND, and then, the operation sequence $0w1w1\ldots w1$ is applied to the cell. The result is a gradual increase of V_c toward V_{dd}. The voltage level after each $w1$ operation is recorded on the result plane, which gives a number of curves in the plane. We stop the $w1$ sequence when ΔV_c becomes small enough (0.05 V in this example). V_{cs} is also shown in the figure as a solid line.

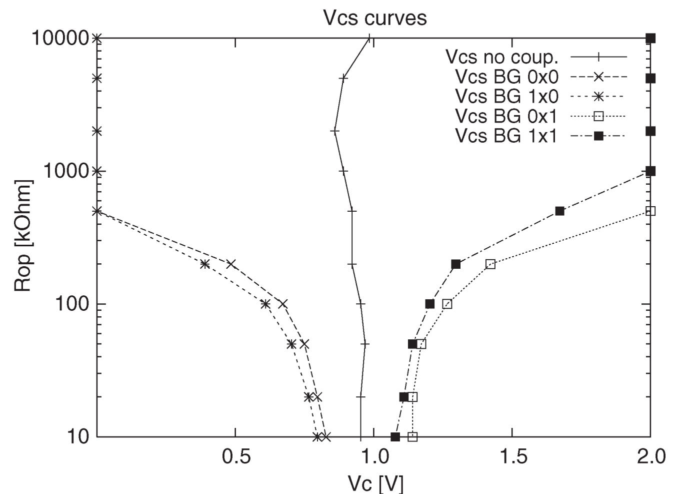

Fig. 8. Different V_{cs} curves showing effects of BL coupling.

It is possible to use the result planes to analyze a number of important aspects of the faulty behavior such as 1) the resistive value of the defect where the memory starts to fail and 2) the test needed to detect the faulty behavior resulting from the open defect [2].

V. Validation of BL Coupling

This section presents the simulation results of the effects of BL coupling on the faulty behavior of the memory model shown in Fig. 2, having the cell open shown in Fig. 5 [3]. The device parameters used in the simulation model correspond to a memory manufactured in 0.20-μm technology. The analysis method used here is the same as that outlined in Section IV. Four different simulations are performed, one for each data BG: BG $0x0$ (both aggressors on BTt and BTb are 0, while the stored voltage in the victim is floating), BG $0x1$ (cell on BTt is 0 and on BTb is 1), BG $1x0$ (cell on BTt is 1 and on BTb is 0), and BG $1x1$ (both cells are 1).

The analysis results show that the write curves are very similar in all BGs and are also similar to the $(n)w0$ curves shown in Fig. 6 and the $(n)w1$ curves shown in Fig. 7. Therefore, they are not significantly influenced by BL coupling and are not discussed further.

The effects of BL coupling on the faulty behavior are evident in the way the V_{cs} curve is influenced. This is expected since the V_{cs} curve is closely associated with the amount of differential voltage developing on a given BL pair. Fig. 8 shows four different V_{cs} curves for the simulated BGs, plus the one resulting in the case of zero coupling (no coupling) (see Fig. 6).

The figure shows that for a victim with a stored 0, the worst-case coupling is generated with BG $1x0$, then with BG $0x0$, followed by the case with no coupling, then BG $1x1$, and finally BG $0x1$. For a victim with a stored 1, the worst-case coupling is generated with BG $0x1$, then BG $1x1$, no coupling, BG $0x0$, and finally BG $1x0$. This means that the worst-case condition for a victim containing the value x corresponds to BG $\bar{x}xx$. Comparing these results with the theoretical analysis of Section III indicates that the dominant BL coupling effect in the simulations of Fig. 8 is a pre-sense coupling.

The figure also shows that the most influential cell on the behavior is the one on BTb. This is expected since the pre-sense and post-sense coupling effects induced by the cell both pull the voltage on BCm in the same direction. The cell on BTt has a limited impact on the

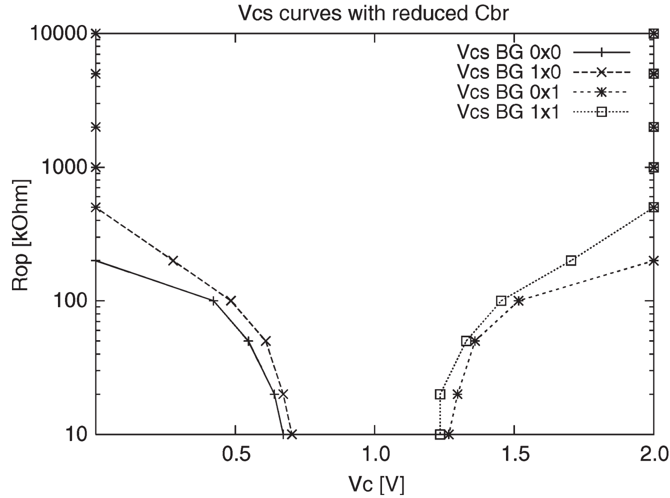

Fig. 9. V_{cs} curves showing coupling with reduced C_{br}.

behavior since it induces opposing pre-sense and post-sense coupling voltages on BTm. It is interesting to note that, for a given victim value, some BGs actually help the faulty behavior to produce the correct read output, which indicates the importance of selecting the worst-case BG values.

To check the correct correspondence between the simulation results and the theoretical analysis of Section III, one could ask the question: Is it possible to modify the simulation model in such a way that would make post-sensing more dominant than pre-sensing?

Referring to (2) and (3), ΔV_1 and ΔV_2 are related as follows:

$$\frac{\Delta V_1}{\Delta V_2} \sim \frac{(C_{br} + C_{bb})^2}{C_{br} + 2C_{bb}} \qquad (4)$$

where we consider Δt as a constant. This relationship indicates that to increase the relative impact of ΔV_2 compared to ΔV_1, the ratio in (4) should be reduced, which in turn can be done by reducing C_{br}. Fig. 9 shows four new V_{cs} curves corresponding to a modified simulation model with $C_{br2} = C_{br}/2$. The figure shows that for a victim containing a 0, the worst-case condition is ensured by BG $0x0$, then BG $1x0$, BG $1x1$, and finally BG $0x1$. On the other hand, the worst-case condition for a cell containing a 1 is ensured with BG $0x1$, then BG $1x1$, BG $1x0$, and finally BG $0x0$. This represents a mixed behavior where the post-sensing effects are dominant when sensing a 0 in the victim, while pre-sensing effects are dominant when sensing a 1 in the victim (see Section III). Reducing C_{br} further does not change this mixed behavior.

It is worth noting that post-sensing effects are also able to dominate both sensing a 0 and a 1 in the victim. In conclusion, depending on the specific memory design and fabrication technology, either pre-sensing or post-sensing effects (or both) may dominate the resulting faulty behavior. This, in turn, means that unless an analysis is done to identify the exact coupling effects for a specific memory, then all possible worst-case data BGs have to be considered during testing.

VI. Impact of BL Twisting

Previous research on crosstalk reduction on BLs in memory devices investigates the effectiveness of BL twisting techniques in eliminating BL noise in current and future fabrication technologies [11]. In addition, there is some published qualitative analysis of the possible impact of BL twisting on the faulty behavior of memories [13]. This section gives a quantitative theoretical investigation of the influence of BL twisting on the faulty behavior of DRAMs. A number of BL twisting techniques are evaluated, and the way a neighborhood of cells influences the behavior is shown [4].

BL twisting is used to reduce the influence of BL coupling on the behavior of the memory by shielding parts of a BL from neighboring BLs. There are many types of BL twisting schemes used in the industry. Fig. 10 compares the untwisted BL scheme with other important twisted BL organizations [5]. These BL organizations are known to be effective at reducing crosstalk between adjacent BLs, and they have all been used in commercially produced memory components [12]. In Section III, we analyzed the impact of solid BLs on the behavior, and in this section, we discuss the impact of single and triple twisting on the behavior.

A. Single Twist

Close consideration of the impact of the single twist on memory behavior shows that the single twist fails in completely eliminating pre-sense BL coupling but succeeds in eliminating post-sense coupling. The net effect is that the single twist results in making pre-sense coupling more significant than post-sense coupling on the faulty behavior of the memory. In the following, a more detailed discussion of this point is given.

For pre-sense coupling, Fig. 11 shows the pre-sense voltage development on BTm and BCm as a result of a logic 1 stored in both neighboring cells. Since the accessed cell on BCt has a logic 1, a small upward voltage differential of V_a develops on BCt during pre-sensing, which in turn results in pulling BTm up by V_b. As a result of BL twisting, the amount of V_b developing on BTm is almost one-half of that in the case of solid BLs.[3] The same situation takes place with BCb, where an up voltage differential of V_c induces an up voltage differential of V_d on BCm. In conclusion, the single twist cuts the amount of pre-sense BL coupling by almost one half and requires a worst-case BG of $\bar{x}_{a_t} x_v x_{a_b}$ (i.e., Cell 0 on BCt contains $\bar{x}$ and Cell 0 on BCb contains x).

For post-sense coupling, Fig. 12 shows the voltage development on BTm and BCm as a result of a logic 1 stored in both neighboring cells. During post-sensing, and since the accessed cell on BCt has a logic 1, the top sense amplifier pulls the voltage on BCt up by an amount of V_{a1}, which induces an up differential voltage of V_{a2} on BTm. At the same time, the top sense amplifier pulls the voltage on BTt down by an amount of V_{b1}, resulting in a down voltage of V_{b2} on BTm. Since V_{a2} and V_{b2} are equal and opposite to each other, they nullify each other, leaving a zero net coupling voltage on BTm. The same situation takes place with the bottom sense amplifier, which pulls BCb down by V_{c1}, inducing V_{c2} on BCm, and pulls BTb up by V_{d1}, inducing V_{d2} on BCm. V_{c2} and V_{d2} nullify each other, leaving a zero net coupling voltage on BCm. In conclusion, the single BL twist totally eliminates post-sense coupling effects.

B. Triple Twist

Close consideration of the impact of the triple twist on the memory behavior reveals that the triple twist succeeds in completely eliminating the influence of BL coupling, both pre-sense and post-sense coupling. As a result, only indirect (or second-order) BL coupling effects remain present between memory cells, which are complex to analyze theoretically. This means that one cannot evaluate the impact of the triple twist on the faulty behavior of the memory by theoretically analyzing the effect of BL coupling, and therefore, electrical simulation here becomes necessary to evaluate the faulty behavior.

[3] It is actually slightly higher than one-half as a result of second-order coupling, which is not considered in this discussion.

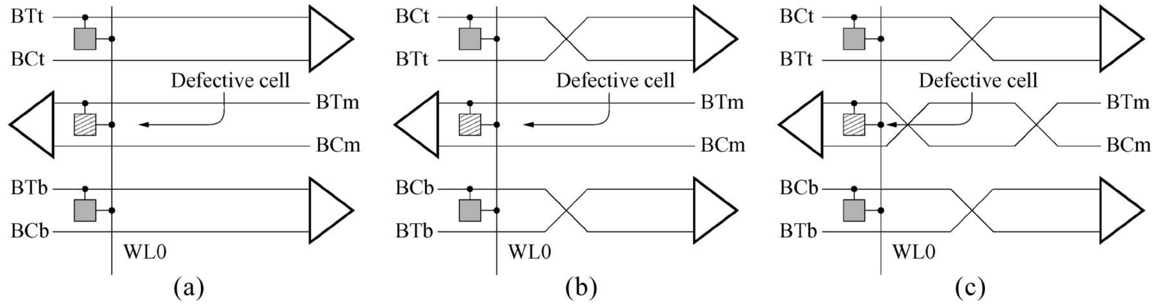

Fig. 10. Analyzed BL organization. (a) Solid BLs (no twist). (b) Single BL twist. (c) Triple BL twist.

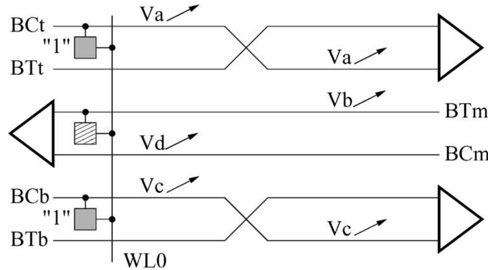

Fig. 11. Pre-sense voltage development for a single twist.

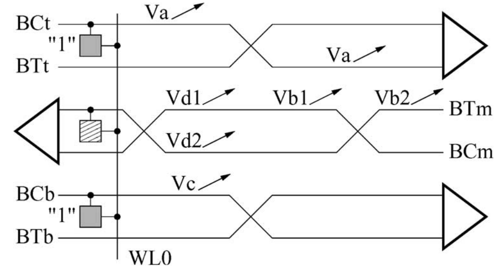

Fig. 13. Pre-sense voltage development for a triple twist.

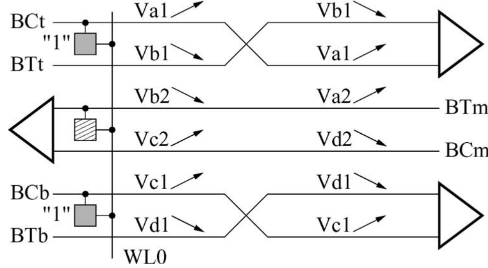

Fig. 12. Post-sense voltage development for a single twist.

This can be understood by noticing that the triple twist splits the BL into four equal parts, such that one half of any coupling effect is induced onto BTm while the other half is induced onto BCm. Since only a voltage "differential" between BTm and BCm is able to influence the behavior of the memory, then a common change (whether increasing or decreasing) in the voltage of BTm and BCm has no impact on the behavior. In other words, the triple twist transforms the differential-mode noise into common mode noise for which the sense amplifier is insensitive.

As an example, Fig. 13 shows the pre-sense coupling voltage development on BTm and BCm as a result of a logic 1 stored in both neighboring cells. During pre-sensing, and since the accessed cell on BCt has a logic 1, an up voltage of V_a develops on BCt, which in turn results in pulling BCm up by V_{b1} and in pulling BTm up by V_{b2} at the same time. Both V_{b1} and V_{b2} are equal and therefore do not result in a differential voltage developing between BTm and BCm. The same situation takes place with BCb, where an up voltage V_c induces an up voltage of V_{d1} on BCm and an up voltage of V_{d2} on BTm. Since both V_{d1} and V_{d2} are equal, they do not result in a differential voltage developing between BTm and BCm.

VII. Validation of BL Twisting

This section presents the results of the simulation analysis of the three different BL organizations shown in Fig. 10 and discusses their impact on the faulty behavior [4]. The memory simulation model employed for the analysis is the same as the one shown in Fig. 2, whereas the device parameters used in the simulation model correspond to a memory manufactured in 0.14-μm technology. These device parameters are chosen to be different from those used in Section V to get a new and independent set of results to test the theory. The simulation is based on the concepts of result planes and the cell sense voltage (V_{cs}) curves previously used to analyze the faulty behavior of DRAMs in general [2] and to evaluate the impact of BL coupling in particular [3].

Consider the defective DRAM cell shown in Fig. 5, where a resistive open (R_{op}) between BT (true BL) and pass transistor limits the ability to control and observe the voltage across the cell capacitor (V_c). The open is injected into Cell 0 and simulated as part of the reduced memory model shown in Fig. 2. The simulation results are represented in Fig. 14, which shows three result planes for the three BL organizations discussed in this paper [4]. The information represented in these result planes can be interpreted in the same way as in Figs. 8 and 9.

Fig. 14(a) presents the four BGs associated with the solid BL organization, where no twisting is used. The figure shows that the worst case BG for detecting a 0 in the defective cell is $0x0$, whereas the worst case BG for detecting a 1 in the cell is $1x1$. In other words, a worst case BG of xxx is needed, which means that the post-sense coupling effect is prevalent for the simulated memory model according to Section III.

Fig. 14(b) shows the four BGs associated with the single twist BL organization, which according to the analytical evaluation presented in Section VI should only be affected by pre-sense BL coupling. The figure shows that the worst case BG for detecting a 0 in the cell is $1x0$, whereas the worst case BG for detecting a 1 in the cell is $0x1$. In other words, a worst case BG of $\bar{x}xx$ is needed, which indeed matches that of a pre-sense coupling effect. This means that by introducing the single twist into the model, post-sense coupling effects [prevalent before introducing the twist, as indicated in Fig. 14(a)] have been neutralized, which makes pre-sense coupling effects become the more prevalent sort of BL coupling.

Fig. 14(c) shows the four BGs associated with the triple twist BL organization, which according to the analytical evaluation presented in Section VI should totally eliminate pre-sense and post-sense BL coupling effects. The figure shows that the worst-case BG for detecting

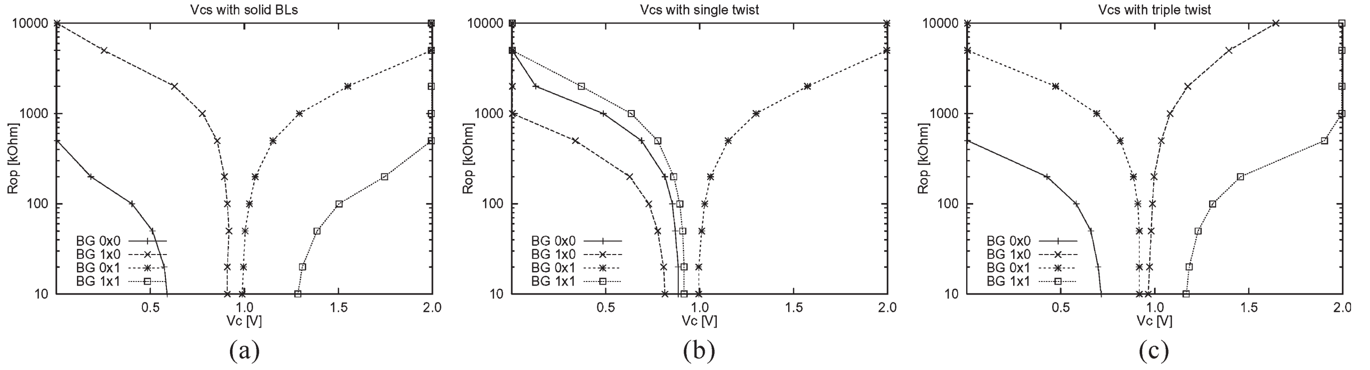

Fig. 14. V_{cs} curves with different BGs for (a) solid BL organization, (b) single twist, and (c) triple twist.

a 0 in the cell is $0x0$, whereas the worst-case BG for detecting a 1 is $1x1$, which indicates an existing post-sense coupling effect on the defective cell. Although this may seem to be contradictory with the analytical evaluation of Section VI, it can actually be explained by the fact that Section VI only took into consideration first-order BL coupling effects caused by BL to BL coupling capacitances. It is important to note, however, that second-order BL coupling exists in the form of BL to "line" to BL coupling (BL to WL to BL, for example), which is negligible when compared to the direct first-order BL to BL coupling. However, in the absence of first-order coupling, second-order coupling becomes the major factor in the faulty behavior. This is also indicated by the fact that the V_{cs} curves of Fig. 14(c) are located closer together than those of Fig. 14(a), which means that the post-sense coupling effect with the triple twist represents a fraction of the full post-sense coupling effect without any twists.

This can be mathematically illustrated as follows: It is possible to represent the coupling voltage in the case of solid BLs as V_{0t} (for 0 twists), i.e.,

$$V_{0t} = \Delta V' + \Delta V'' \tag{5}$$

$$= \Delta V' + f \cdot \Delta V' \tag{6}$$

$$= \Delta V_2 - \Delta V_1 + f \cdot \Delta V_2 - f \cdot \Delta V_1 \tag{7}$$

where V' and V'' stand for first-order and second-order coupling effects, respectively, and f represents the "factor" that relates V' to V''. Since second-order effects are supposed to be a fraction of first-order effects, f should satisfy $0 < f < 1$. V_1 and V_2 stand for pre- and post-sense coupling voltages [see (2) and (3)]. The "$-$" sign between V_2 and V_1 indicates that these voltage coupling effects are opposite to each other.

The coupling voltages in the case of the single BL twist (V_{1t}) and the triple BL twist (V_{3t}) can be represented as follows:

$$V_{1t} = \frac{1}{2}\Delta V_1 + f \cdot \Delta V_1 - f \cdot \Delta V_2 \tag{8}$$

$$V_{3t} = f \cdot \Delta V_2 - f \cdot \Delta V_1. \tag{9}$$

The fact that the impact of the triple twist coupling voltage seems to be bigger than the impact of the single twist coupling voltage can be represented as follows:

$$V_{3t} > V_{1t} \Longrightarrow f \cdot (\Delta V_2 - \Delta V_1) > \left(f + \frac{1}{2}\right)\Delta V_1 - f \cdot \Delta V_2$$

$$\Longrightarrow f > \frac{\Delta V_1}{4(\Delta V_2 - \Delta V_1)}. \tag{10}$$

Applying the condition $0 < f < 1$ to (10) results in the following condition that relates pre- and post-sense coupling voltages:

$$\Delta V_2 > \frac{5}{4}\Delta V_1. \tag{11}$$

Equation (11) states that, although second-order effects are a fraction f of first-order effects, it is possible for V_{3t} to be bigger than V_{1t} as long as post-sense effects (ΔV_2) remain large enough (relative to ΔV_1).

In the case of the triple twist, analytical evaluation of second-order BL coupling effects on the behavior is overly complex, and electrical simulation can provide considerable insight into the faulty behavior of a defective memory.

VIII. Conclusion

This paper analyzed the effects of BL coupling on the faulty behavior of DRAMs. Two different coupling mechanisms were identified, i.e., pre-sense and post-sense coupling, which have a partly opposing effect on the faulty behavior, something that is important to take into consideration when designing DRAM tests. The effects of both mechanisms were analyzed, first analytically and then using a Spice memory simulation model. This paper also analyzed the effects of BL twisting on the behavior of defective DRAMs. Three well-known BL organizations have been taken into consideration: 1) solid BLs; 2) single BL twists; and 3) triple BL twists. The single twist eliminates post-sense coupling, which makes pre-sense coupling the more prominent factor, whereas the triple twist eliminates pre-sense and post-sense first-order coupling, which makes second-order coupling become prominent. The analysis indicates that it is not always possible to know the worst-case BL coupling pattern needed to test the memory. Fault analysis based on electrical Spice simulation can provide great insights into the faulty behavior and is able to reduce the complexity of analyzing the second-order coupling promoted by the triple twist.

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Floorplanning With Wire Pipelining in Adaptive Communication Channels

Mario R. Casu and Luca Macchiarulo

***Abstract*—The recent shift toward wire pipelining (WP) mandated by technological factors has attracted attention toward latency-controlled floorplanning. However, no systematic study has been published so far that takes into account block and logic-delay limitations. This paper aims at filling the gap by showing that block delay can limit and possibly prevent any real gain WP might promise. In this paper, the authors also show how a modified adaptive WP scheme, on the other hand, allows relevant gains. They built a SoC floorplanner based on the use of adaptive and nonadaptive WP, which optimizes the data rate, taking block delay into account. The results of new and old WP techniques applied on benchmarks and on an MPEG decoder are compared to the optimal results obtained when no WP is employed.**

***Index Terms*—Floorplanning, systems-on-chip, wire pipelining (WP).**

I. Introduction

The different scalability of logic and local interconnects on the one hand, and global wires on the other hand, is a serious concern that might jeopardize the advantage of CMOS technology scaling [1]. Wire pipelining (WP) helps facing this problem. In addition to buffer insertion, wires may be segmented by intermediate flip-flops or latches. The throughput of the connection increases as well as the latency of the connections, thus possibly jeopardizing the frequency increase.

This new technique has attracted attention toward latency-controlled floorplanning (see [2]–[6], or the latest [7], for example). However, to the authors' knowledge, no systematic study has been published so far that takes into account block and logic-delay limitations. In this paper, based on the work we presented at the International Symposium on Physical Design [8], we aim at partially filling the gap. We show that block delay can limit and possibly prevent any real performance gain the WP technique, if implemented in a too conservative way, might promise. We also show how a different WP technique exploiting the locality of computation of some blocks, which from time to time do not read data from inputs with added wire latency, can be the key to fulfill the promise of high data rate of WP. To this aim, we adopted a floorplan strategy that optimizes the data rate of systems (DR) based on standard and modified WP using suitable cost functions. We took into account various models of block delay and compared them to the optimal results obtained when no WP is employed.

In Section II, we briefly recall the characteristics of a standard WP technique. Its limits are highlighted in Section III through a mathematical derivation that takes into account the effect of intellectual property (IP) block delays. In Section IV, the performance results obtained with our new floorplanning strategy employing standard WP, with and without limitations imposed by the blocks delays, are reported. The foundations of the alternative WP methodology are described in Section V, while the results of its application using a modified floorplanner are outlined in Section VI. The effectiveness of the new technique is highlighted by means of a realistic case study, an MPEG decoder. Finally, conclusions are drawn in Section VII.

II. Promise of WP

The increased bandwidth of wires guaranteed by WP comes at the cost of increased wire latency. Such change of paradigm not only opens way to a number of new opportunities (see, for example, [9] and [10]) but also gives rise to relevant issues that range from functional and architectural to physical-design aspects (see for a review [3], [11], and references therein).

Even if from an abstract point of view, it might be possible to run wires at any desired frequency by simply increasing the number of pipeline stages, we need to investigate when this is in fact beneficial to the overall performance of the system. We restrict our analysis to the case (as that of systems-on-chip) in which designers connect IP taken from libraries and are not allowed to modify their internal structure, and no architectural features are present to render their IP independently "latency-tolerant." A class of communication protocols that allow transparent insertion of arbitrary latency is the so-called Latency Insensitive Protocols (LIP), which, by means of special wrappers around the blocks and pipeline elements along the wires, make a system with added latency functionally equivalent to a zero-latency system [9]. The equivalence is obtained by making the blocks "patient," i.e., suspending their operation by suitably gating their clock—if at least one of their inputs is not ready to be processed because of the latency.

Latency insensitiveness guarantees a strong form of equivalence between the original and the pipelined system: all the execution traces differ in "non-valid" time slots where no computation is allowed. This means that a one-to-one mapping between the traces is enforced. This is different from usual functional-level pipelining where there is no concept of nonvalid slots, and two traces might depend substantially on the pipelining depth.

To introduce performance measures in such cases, we first give some definitions.

1) A block is a computational logic element. In our analysis, a block behaves as a synchronous element.
2) A system is a collection of interconnected blocks. Formally, it can be represented with a directed graph $G = \{V, E\}$ whose vertices V are the blocks, and connections are edges E. The system is synchronous to a clock frequency F.

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