A New Digital Architecture For Reliable, Ultra-Low-Power Systems

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Abstract— **We are working towards the specification and design of a new system-level architecture serving as the digital control/processing core of ultra-low-power ($< 100\ \mu W$) and reliable systems along with a suitable, new compiler. Our primary area of focus is implantable microelectronic devices. While respecting the traditional design constraints of biomedical-implant design for low power consumption and miniature device size, the architecture shall be generic in nature, i.e. allowing for different peripheral blocks (sensors, actuators etc.) to be ported for building various application-specific implantable systems. Also importantly, the proposed architecture shall employ various fault-tolerance techniques for building highly reliable devices. Our approach is bottom-up one, starting from the architectural level and being complemented by a suitable, new compiler. The compiler shall provide the means to exploiting this architecture for different application setups and, by design, shall further underpin the reliability and low-power issues.**

Keywords—**Implantable biomedical devices, computer architecture, computer reliability**

I. Introduction

During the last two decades or so, an unprecedented market turn towards portable, embedded systems has been witnessed. Mobile telephony, ubiquitous computing (e.g. multimedia applications) and other fields have created a need for building portable devices of low power consumption. Moreover, the fields of wireless sensor networks [19] and biomedical implants - such as pacemakers [7] - have tightened the power budget further and have added extra requirements for dependable design. Anticipated is also the need for systems which can be built in part or in whole from reusable components, say I.P. (Intellectual-Property) cores. The realization of portable, high-performance and at the same time low-power consuming systems has been greatly facilitated by the recent, phenomenal advances in CMOS technology [8], featuring ultra-low-power transistors of miniature size, which has redefined what is "feasible" and what is not. Thus, new design approaches can now be investigated for developing new generations of low-power, embedded devices.

Our research is primarily focused on biomedical, microelectronic implants which impose ultra-low-power and high-reliability requirements. Moreover, their extremely high design cost calls for a generic design approach. In this way, different implantable systems can be developed based on an initial, modular design, effectively diminishing recurring development costs and reducing time-to-market.

We work on developing a digital architecture for such systems which will take into consideration all above requirements. The architecture will be *generic* in nature so that it can be (re)used for a wide range of different biomedical applications (e.g. glucose-sensing, temperature/intracranial pressure monitoring etc.) and potentially for wireless-sensor-network applications. It will do so by allowing a large gamut of different sensors and/or actuators to be interfaced and controlled by it.

Moreover, the architecture will be actively designed for *reliability* by inherently supporting dynamic error detection, fault isolation and correction. Lastly, the architecture will be *minimalistic* in nature (low bit count, small instruction set) so as to implement all above features while at the same time adhering to a strict *ultra-low-power consumption* requirement ($< 100\ \mu W$).

II. Related work

The area of biomedical implants implicitly demands design for low power and, thus, substantial work has been done so far in this area. Devices with an average power consumption in the range of a few hundred milliwatts have been proposed by many a researcher. For instance, Au-Yeung et al. [1] have come up with an implantable cardiac telemetry system for studying atrial fibrillation which consumes about $115.3\ mW$ when active. Prämaßing et al. [13], [14], [5], [3], [4], [15] have designed and implemented an implantable system for repairing blindness due to blurred cornea utilizing about $395\ mW$ in active state.

There have been presented other instances of implantable devices with even lower power needs. Such systems are typically minimalistic implementations designed to perform highly specialized tasks. To exemplify, Park H.J. et al., [10], [11], [9] have developed a swallowable, telemetry capsule for wireless endoscopy, consuming a

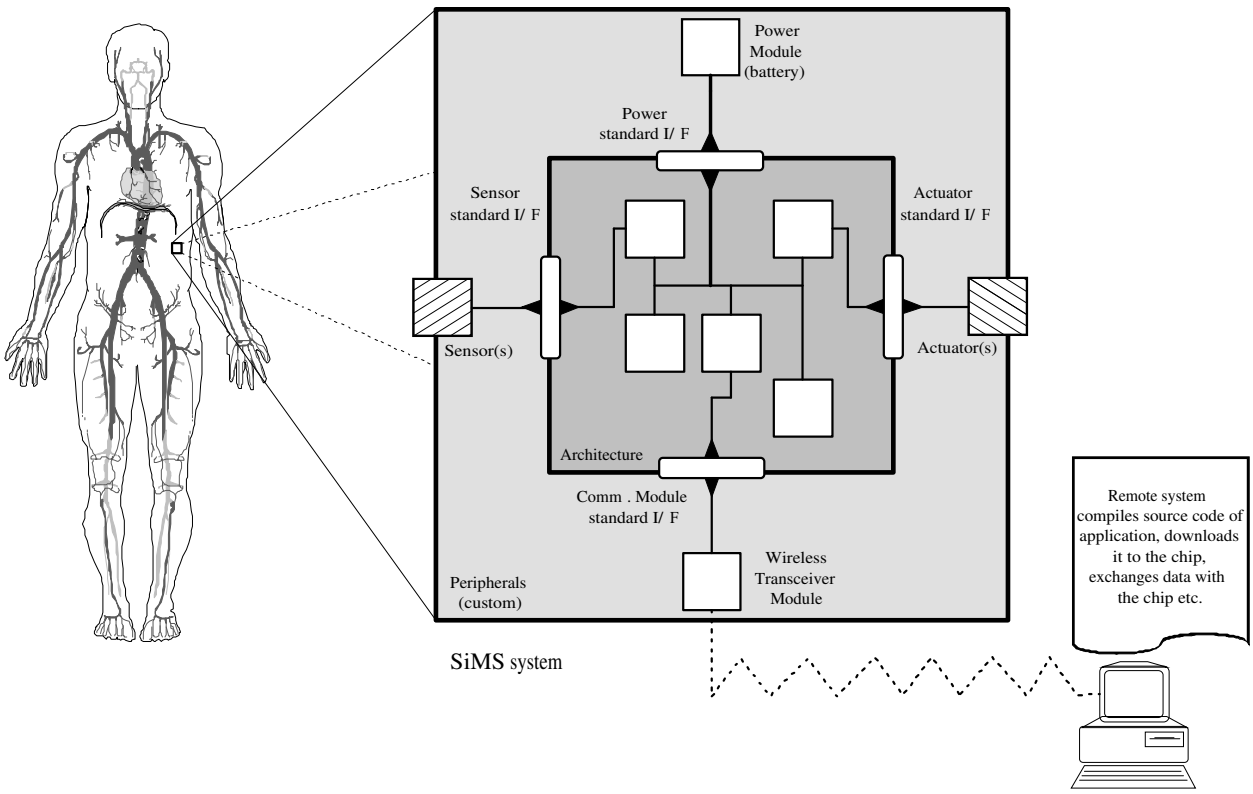

Fig. 1. Overview of SiMS.

mere 29.7 mW. Also, Salmons et al. [16] have come up with an ASIC-based microstimulator device for restoring functionality to paralyzed muscles which consumes a mere 90 μW when on.

As far as generic use is concerned, a few researchers have attempted to build systems with some degree of modularity for making them capable of adapting to different application scenarios. Fernald et al. [6] have come up with a modular microprocessor architecture which accepts various peripheral modules such as sensors and actuators. Smith et al. [18] have attacked the problem from a slightly different angle. They have designed an implantable stimulator device with provisions for a large set of peripherals. Given a specific application, unutilized components of the initial, "baseline" design are removed, resulting in a reduced system, sewn to the application needs and with lower power/area requirements than those of the base design.

Finally, reliability has been addressed to some extent by a limited number of researchers. Various approaches have been encountered ranging from duplication of circuits and structures (e.g. Pauley et al. [12]), to self-test/diagnostic circuitry (Berkman and Prak [2], [17]), to structural testability (Salmons et al. [16]) and other.

III. Contents of our research

The incentive for this work is the fact that, to the best of our knowledge, there does not exist a single implementation of a low-power digital architecture which also inherently addresses issues of modularity and reliability, all in one. In this context, we are proposing **Smart implantable Medical Systems** (**SiMS**, hereforth); that is, small implantable devices able to measure and/or regulate multiple biomedical parameters simultaneously and communicate with external (out-of-body) computing equipment wirelessly. Given that such devices are directly related to human life, they will be characterized by very high reliability, some degree of autonomy and self-awareness (within extremely demanding low power and size constraints). Our goal is to target silicon, multi-sensor (actuator), single chip, wireless medical systems. Such systems will be produced using fully integrated CMOS processes. In addition, they will be capable of context sensitive behaviour (smart), due to their multi-parameter awareness and communication abilities.

Our research is divided in two integral parts, namely i) a **digital architecture & compiler**, and ii) **peripherals**. The digital architecture and compiler are the underlying processing/controlling unit and system software - respectively - of a SiMS device. The peripherals of SiMS are all remaining (peripheral to the central unit) components

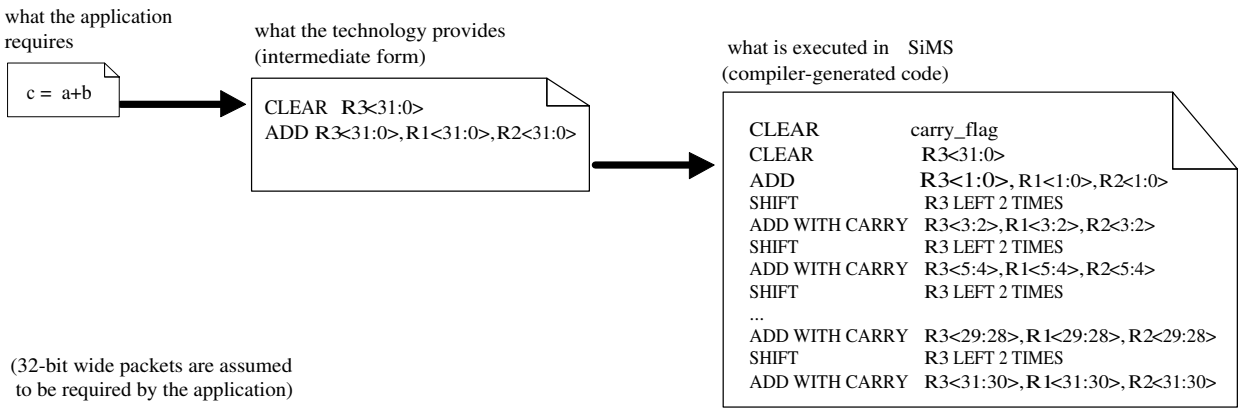

Fig. 2. Compiler role to application translation from high to low level code.

that make an implantable device interface with its environment, namely: i) microsensors and microactuators, ii) wireless communication module for contacting the out-of-body computing equipment, and iii) power module. A typical SiMS system as outlined above is shown in Fig.1.

IV. SiMS-PLATFORM SPECIFICS

A. The digital architecture

The digital architecture will be designed to be the *processing/controlling* core of the implantable device. It is termed as "processing" since it will perform all required data calculations of the device and as "controlling" because all peripheral modules of the device will be under its direct or indirect control. This architecture will be complemented by a new, specialized compiler which will handle *software generation* and *optimization*. For every new application scenario the implantable device model needs to behave in a specific fashion. This "behavior" will be inputted into the system in the form of a program source code which will be externally compiled and properly transmitted to the implantable device. It falls well within the goals of this work that the implantable device shall be able to be reprogrammed more than once and - more importantly - at run time, hence the demand on high reliability.

As previously mentioned, implantable devices are liable to a set of strict (often extreme) specifications due to the sensitive and demanding nature of their living "environment" and SiMS have to conform to them. In more detail, the architecture will be crucial in delivering highly reliable implantable devices. In principle, it will achieve this by displaying attributes of *error detection* and *error correction* as well as *self-testing* and *self-repairing* properties. Such features will be achieved by redundant hardware structures that will continuously check, correct and/or isolate faulty modules. To this end, reconfigurable standard cells may be used as well. Towards device safety and unhindered operation, further studies will be performed so as to effectively handle (on the architectural level) additional environmental aspects such as EMC and device heat dissipation.

The architecture of the platform will be extremely minute (1-bit / 2-bit architecture) featuring only a few hundred transistor devices at a maximum. The obvious reasons for this choice are the small-size and the low-power constraints ($100 - \mu W$ order of magnitude or lower) that implantable devices have to obey. A slightly larger size may deem a device unusable in the case of e.g. intracortical implantation whereas high power consumption: a) drains the battery of an implantable device rapidly, and b) causes potential damage (e.g. burns) to its surrounding tissue due to heat dissipation. A less obvious reason for a tiny architecture is that it allows for achieving and maintaining the reliability of the system more easily. Finally, the architecture will define specific interfaces to all peripheral modules and will, thus, standardize and simplify the way different modules are selected for different applications.

B. The compiler

The compiler will be responsible for generating the machine code to be executed by the SiMS architecture. Application design will be straightforward: a desired application behavior, defined by e.g. a doctor, will be properly encoded in a high-level language which will, then, be compiled to machine code and directly mapped to the Instruction-Set Architecture (ISA) defined during the first work package of this project. Like all standard compilers, the compiler tied to the SiMS platform will be able to perform code optimizations. In so doing, the instruction count (and, thus, execution time) of specific applications may be reduced allowing for lower power consumption and, therefore, for prolonged implantable device lifetime (i.e. autonomy). Nonetheless, other advanced compiler issues like

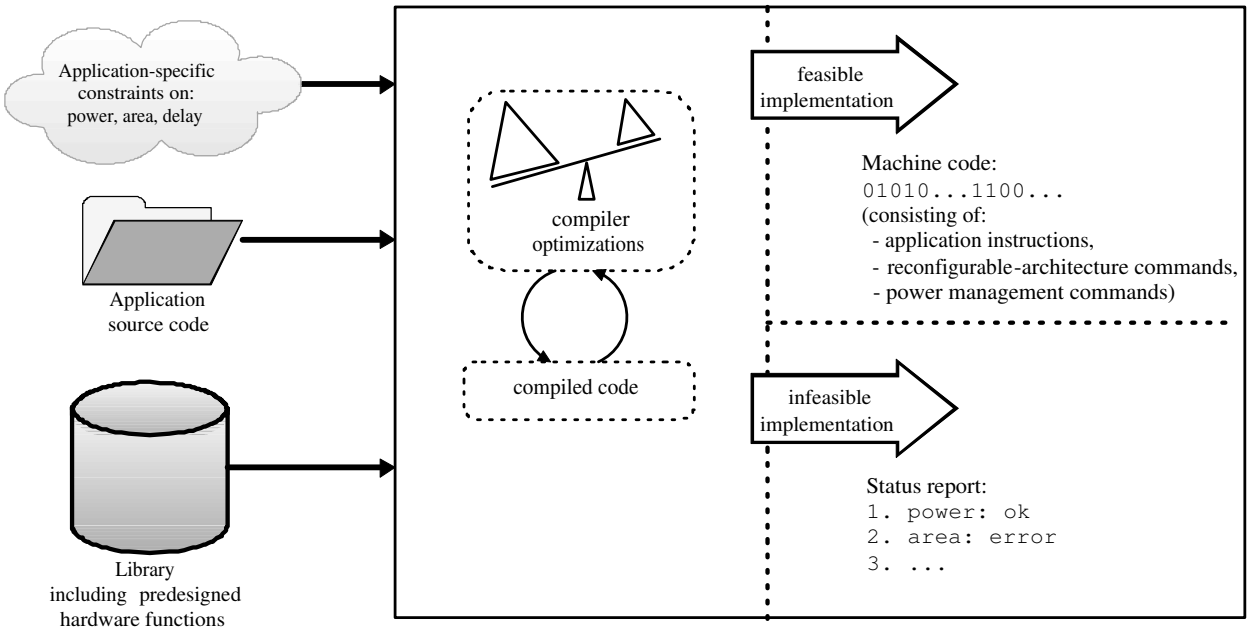

Fig. 3. Compiler model and data flow.

resource and data scheduling will not be addressed at all in this project due to the simplistic architectural approach selected (as described previously), which effectively renders all such enhancements useless.

On the other hand, the consideration of a tiny architecture necessitates a kind of abstraction functionality on the side of the compiler. To make this clear, imagine - for instance - that a specific medical application needs to receive (and properly handle) 32-bit data packets from an implantable device (say, an intra-cortical electrode array performing EEG measurements). Since the SiMS platform resides on a tiny-bit-count architecture (say, 2 bits), it is obvious that the high-level programmer has to program the device to transmit 2-bit sensor read-outs times 16, to acquire a simple data packet. Obviously, this is least convenient and - while the application developer may be allowed to manipulate larger data bundles (following the high-level needs of modern applications) - it will be the responsibility of the compiler to decompose them to the actual, elementary quantities (see Fig.2).

The ever crucial issue of reliability is treated at the compiler level, too. The compiler actively handles this aspect by also accepting application-specific constraint files along with the main application source code. Such a file will include application-specific information regarding, for instance, the nominal and maximal power consumption allowed, the area utilization and the processing speed of the targeted application. This set of constraints will - per case - reflect general specifications of the application. For example, similar code transformation may lead to different results in relation to the context (where - inside the human body - the targeted system will be implanted), e.g. same power dissipation found prohibitively large for usage inside the brain may be normal in some other cases. Given the source code and the set of constraints, the compiler will then determine if a realistic solution on the SiMS platform exists. It is an extra safety precaution that if there is no such solution, the compiler will generate an error report and will not output any machine code for the device. The compiler data flow is illustrated in Fig.3.

C. The peripheral modules

The architecture will also encompass well-defined interfaces to the ”outside world”, the *peripheral* part of the platform. That part is outlined in Fig.1 as a larger box enveloping the architecture box and, as its name suggests, encompasses all other (peripheral to the central unit) components that make an implantable device functional. Such peripherals may be: i) microsensors and microactuators (i.e. the interaction of the implantable device to the living tissue), ii) a wireless communication module for contacting the out-of-body environment, and iii) a power module (e.g. a rechargeable battery).

In order to make the SiMS platform a real ”scaffold” for diverse new implantable devices and not just a hard-wired solution to a specific problem, the platform design needs to be modular. This means the peripherals need to be exactly that; i.e. peripheral modules that can be exchangeable with other modules - depending on the application requirements at hand. For instance, the sensory module(s)

might be a glucose-level detector, a miniature CCD camera, a flow sensor, a pressure sensor, a humidity sensor, a temperature sensor etc.. Likewise, the actuating element(s) might be a blood pump, a drug-delivery system (drug infusion pump), a neurostimulator etc.. Seamless integration of the peripherals with the underlying architecture shall be ensured through well-defined interfaces, mentioned above. Of course, it may be the case that, in specific applications, some of the modules except - of course - for the power module, are not required and, thus, will not be included in the end-user device.

In this case, research effort will be focused on investigating only new (bio)sensors and (bio)actuators or on improving mature ones (the following subsection *"Further points of concern"* will clarify the reasons for this limitation). A typical improvement paradigm to be undertaken is, as introduced earlier, an implantable glucose detector. Such modules have commonly been based on biosensing elements that unfortunately age (i.e. their performance deteriorates with time). The suggested approach investigates a glucose detector based on optical technology, so as to avoid chemical interaction with the living medium and, thus, performance degradation. For the purposes of this work, a small set of microsensor and microactuator devices will be developed for various test applications. The endmost goal is proving, by example, the modularity benefits of the SiMS-platform approach.

Much effort will be put on the *transducing system* of those sensory and actuating elements in an attempt to boost sensitivity and performance. By improving peripheral modules, reliability as well as size and power consumption will directly benefit. To a further extent, built-in self-test will be supported by these modules offering increased reliability and safety, in conjunction with the provisions made on the architecture part, mentioned above.

On another level, the micromachining implementation method to be used will mainly affect size issues (micron and submicron technology) but also power issues. Furthermore, environmental constraints such as EMC apply to these modules and will be considered in this project. Lastly, an important topic is that, unlike the architecture which is isolated from the environment, sensors and actuators may be in direct physical contact with the living tissue (see also Fig.1). Therefore, additional issues of biocompatibility of the materials used are raised and will be resolved in this part. Nonetheless, it should be stressed out that such issues are heavily application-dependent; the surrounding tissue of an implant greatly affects the kind of materials the implanted device needs to be built from. Thus, peripheral biocompatibility study within the project scope will focus mainly on the applications instances that will be developed.

D. *Further points of concern*

Having discussed the architecture, compiler and sensing/actuation peripherals, we are well aware that there is a significant list of items not addressed in the framework. These items concisely are:

- Power module
- Wireless communication module
- Dedicated ADCs/DACs for the sensors & actuators
- SiMS packaging (biocompatibility)
- Security & privacy of biological data
- System electromagnetic compliance (EMC)
- System heat dissipation

The above items are rather essential in the SiMS framework as we have defined it. Nonetheless, they are currently not addressed in our work due to financial and time constraints. What is more, engineering aside, some of these items require a full medical certification cycle (e.g. testing on animals, humans, standardization etc.) which adds a prohibitive cost/time penalty to the current work. They are, thus, left as future work.

V. Conclusions

By proposing the SiMS concept, we attempt to build a framework which will be a reference for future applications in the medical as well as other fields where ultra-low power consumption, flexibility of design and reliable operation are key requirements to one degree or another. Benefits of this approach are envisioned to be a family of systems with smaller time-to-market costs and robust, guaranteed functionality. At the very least, we expect this work to give an original, fresh viewpoint to be adopted by future art.

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