A generic digital architecture & compiler for implantable devices

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ABSTRACT

A new system-level architecture serving as the digital control/processing core of biomedical, microelectronic implants along with a suitable, new compiler is being proposed. While respecting the traditional design constraints of biomedical-implant design for low power consumption and miniature device size, the architecture shall be generic in nature, i.e. allowing for different peripheral blocks (sensors, actuators etc.) to be ported for building various application-specific implantable systems. Also importantly, the proposed architecture shall employ various fault-tolerance techniques for building highly dependable devices. The edge over the extra cost (in power and size) paid for designing a generic - as opposed to a dedicated - architecture will be given by the recent, rapid advances in CMOS semiconductor technology (small transistor size and low power consumption) - a fact now making specific design choices viable. The new compiler shall provide the means to exploiting this architecture for different application setups and, by design, shall further underpin the dependability and low-power issues.

KEYWORDS: medical implants, generic design, platform, microelectronic, computer architecture

1 Introduction

Biomedical engineering has seen rapid and astounding technological achievements thusfar with highlights in laboratory instrumentation, medical imaging, pacemakers, artificial limbs and computer analysis of the human genome, to name a few [Nebe02]. *Biomedical implants* have attracted particular scientific interest in the last two decades for their promising applications. The first and most typical example of such devices is the implantable pacemaker which has saved (or improved the quality of life of) about 4.3 million patients worldwide. A plethora of biomedical implants has been proposed over the years and new devices are

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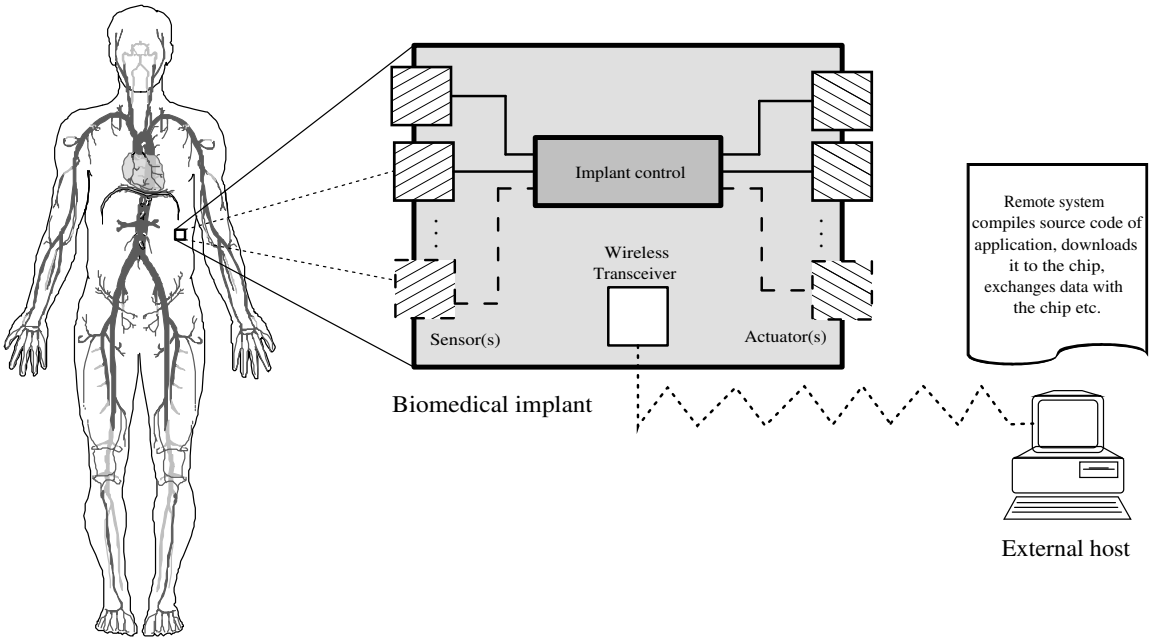

Figure 1: Overview of proposed implantable system.

continually added. Many medical problems are being addressed by these devices, namely functional electrical stimulation of patients for limb control, for suppression of chronic pain, for partial restoration of eye sight, for bladder control etc.. Also, measurement of physiological parameters such as temperature, pH and blood glucose concentration is achieved or monitoring of in-body strains caused by installed prosthetic limbs and so many more. Most of those implants feature bidirectional, wireless (percutaneous) communication with the out-of-body environment for accepting commands and/or transmitting physiological data from inside the body. Acquisition of physiological data on the part of the implants is usually achieved through appropriate *sensors* whereas intervention to the human body (such as insulin administration or the above mentioned electrical stimulation) is effectuated through *actuators*. In this context, sensory and actuating components (or wireless transceiver modules, for that matter) will be collectively called "peripherals". The design and implementation of any implantable device has been subject to strict low-power and small-form-factor considerations as well as tight (inter)national medical regulations. It is these reasons that have traditionally driven most designers to synthesize highly customized designs. In an attempt to provide robust implants with reliable operation and long functional time while keeping power and size figures small, most commercial vendors deliver devices with low flexibility and adaptability, usually aiming at a very narrow application area. Outright results of this situation are the long development times and the (resultant) high cost. Also importantly, minimal reuse of existing designs and/or IP cores and design from scratch for each new application are almost always the case nowadays.

2 Research focus

In this context, our research actively targets the design and development of a *system platform* for implantable devices, that is, a generic, system-level architecture for performing digital control and/or processing duties in the core of implantable devices (see Fig.1), accompanied

by a suitable compiler. This architecture shall be able to inherently support various design goals of biomedical nature (e.g. physiological-signal sampling rate and digital processing, feedback-loop control etc.) in order to replace many existing designs with just one. Needless to say, the proposed architecture shall be designed to also provide for small-size and low-power features as met in existing designs by devising a minimalistic scheme (low-bit-count architecture) of a few hundred transistor devices. The obvious reasons for this choice are the small-size and the low-power constraints ($10 - \mu W$ order of magnitude or lower) that implantable devices have to obey. Secondarily, tiny system architecture will allow for achieving and maintaining the required level of system reliability more easily. Additional important features to be supported will be: a) *flexibility* and *modularity*, for allowing the architecture to seamlessly cope with different combinations and numbers of peripheral modules, depending on the application scenario at hand. Modularity means that a large (as possible) subset of biomedical peripherals shall be able to connect to and be supported by the proposed architecture without any design change. Flexibility means that the architecture shall be versatile enough to support varied peripheral requirements such as sampling rate, amplifier gain, filter bandwidth, stimulating-pulse amplitude and so on. Obviously, for the architecture to achieve the above traits, a well-defined peripheral interface with the potential peripheral modules needs to be specified. This task falls also within the goals of our research. b) *High dependability*, i.e. the architecture-level measures (as opposed to mechanical or packaging measures) for error-free operation of an implant in the presence of hardware faults or stochastic faults induced by the ambient, e.g. EMI, mechanical strain, bodily fluids etc.. To this end, the researched architecture shall be *fault-tolerant*: error detection and isolation, error correction and retry as well as self-testing and self-repairing are considered as main attributes of the design. Such features will be implemented using, for example, redundant hardware structures and reconfiguration that will continuously check and retry when necessary, correct and/or isolate faulty modules.

The compiler will be responsible for generating the machine code to be executed by the above discussed generic architecture. Application design will be straightforward: a desired application behavior, defined by e.g. a doctor, will be properly encoded in a high-level language which will, then, be compiled to machine code and directly mapped to the Instruction-Set Architecture (ISA). Like all standard compilers, the compiler tied to the generic architecture shall be able to perform code optimizations. In so doing, the instruction count (and, thus, execution time) of specific applications may be reduced allowing for lower power consumption and, therefore, for prolonged implantable device lifetime (i.e. autonomy). Furthermore, the consideration of a tiny architecture necessitates a kind of abstraction functionality on the side of the compiler. To make this clear, imagine - for instance - that a specific medical application needs to receive (and properly handle) 32-bit data packets from an implantable device (say, an intra-cortical electrode array performing EEG measurements). Since the targeted architecture shall reside on a tiny-bit-count architecture (say, 2 bits), it is obvious that the high-level programmer has to program the device to transmit 2-bit sensor read-outs times 16, to acquire a simple data packet. Obviously, this is least convenient and - while the application developer may be allowed to manipulate larger data bundles (following the needs of high-level applications) - it will be the responsibility of the compiler to decompose them to the actual, elementary quantities. The ever crucial issue of dependability will treated in the compiler level as well. The compiler shall actively handle this aspect by also accepting application-specific constraint files along with the main application source code. Such a file will include application-specific information regarding, for instance, the

nominal and maximal power consumption allowed, the area utilization and the processing speed of the targeted application. This set of constraints will - per case - reflect particular specifications of the different applications. For example, similar code transformations may lead to different results depending on the context (i.e. in which part of the body the implant will be placed), e.g. the same power dissipation found prohibitively large for usage inside the brain may be normal in case of hip-joint implantation. Given the source code and the set of constraints, the compiler will be able to determine if a realistic solution exists for the implant platform to implement.

3 Conclusions

In the past, various researchers have also attempted to give a mild "generic flavor" to implant design (see, for instance, [Fern91, Smit98, Vald04]). Our research is unique in attempting to develop a truly generic but also highly dependable (through fault tolerance) system architecture while at the same time providing the performance needed by current applications in the field. Our optimism and timing hinges on the fact that microelectronics technology is ever shrinking and becoming ever lower power-demanding. Further miniaturization of the CMOS devices and improvement of their characteristics allows for new approaches to the issue, previously unrealistic. This technology boost now enables the conception and implementation of an architecture with features like the ones discussed above at a size/power cost which is upper bounded and quite feasible (see ITRS roadmap [Inte]). Long-term goal of the research is a well-documented and well-defined design framework for a large variety of new implantable systems by maximizing the reuse of existing IP cores.

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