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Buffer Design Trade-Offs for Single Electron Logic Gates

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***Abstract*— Networks of buffered Threshold Logic Gates (TLG) implemented in Single Electron Tunneling technology have previously been demonstrated to operate correctly for a wide range of logic circuits. Given the complexity of the buffered TLG design, the TLG and the buffer are typically designed and optimized separately. In this paper we propose a method to design the TLG and the buffer separately while optimizing the compound design. First, we analyze the impact of the buffer on the TLG switching behavior. Second, we introduce a general buffer design methodology. Third, we presents a set of buffer implementations and demonstrate their impact on an example TLG.**

***Index Terms*— Single electron tunneling (SET), single electron logic, buffers, SET networks.**

I. Introduction

Single Electron Tunneling (SET) [1] based circuits allow for encoding the Boolean logic values '0' and '1' as a charge of 0 or 1 electrons [2], realizing Single Electron Encoded Logic (SEEL) circuits. A SEEL Threshold Logic Gate (TLG) that can be used as a basis for implementing linear threshold gates with both positive and negative weights, as well as conventional Boolean gates, were proposed earlier in [3]. The feedback problems that occur in networks of such TLGs [4] were overcome by augmenting each gate in the network with an output buffer and networks of buffered TLGs were demonstrated to operate correctly for a range of logic circuits [5], [6].

Thus far, when designing a buffered TLG the TLG and the buffer were optimized independent of each other in order to reduce the complexity of the design process. While this is a pragmatic approach as optimizing the compound design is more difficult due the larger number of circuit parameters one has to consider for this purpose, it cannot take the interaction between the TLG and the buffer into consideration. Thus even though the parts are optimized the compound design might not be. This paper proposes a method to design the TLG and the buffer separately while considering the implications of combining them later into a buffered TLG. First, we analyze the dynamic feedback originating from the buffer and its impact on the switching behavior of the TLG. Second, we proposes a set of buffer implementations suitable for various TLG implementations. Third, we demonstrate the impact of the buffer on the TLG switching behavior through an example.

The remainder of the paper is organized as follows. Section II briefly describes the electron tunneling phenomenon in SET circuits and introduces the SEEL threshold gate and buffer. Section III examines trade-offs in the buffer design and demonstrates the impact of the buffer on the TLG switching behavior. Section IV concludes the paper.

II. Background

SET circuits are centered around tunnel junctions which consist of an ultra-thin insulating layer in a conducting material. In classical physics no charge transport is possible through an insulator. However, when the insulating layer is thin enough the transport or *tunneling* of charge can be controlled in a discrete and accurate manner, i.e., one electron at a time, if it reduces the amount of energy in the system. Tunneling through a junction becomes possible when the junction's current voltage V_j exceeds the junction's critical voltage $V_c = \frac{q_e}{2(C_e+C_j)}$ [7], where $q_e = 1.602 \cdot 10^{-19}C$, C_j is the capacitance of the junctions and C_e is the capacitive value of the remainder of the circuit as seen from the junction. In other words, tunneling can occur if and only if $|V_j| \geq V_c$. Electron tunneling is stochastic in nature and as such delay cannot be analyzed in the traditional sense. Instead, for each transported electron one can describe the switching delay as

$$t_d = \frac{-ln(P_{error})q_eR_t}{|V_j| - V_c}, \tag{1}$$

where R_t is the junction's resistance and P_{error} is the chance that the desired charge transport has not occurred after t_d seconds (this paper assumes $R_t = 10^5\Omega$ and $P_{error} = 10^{-8}$). Each transported electron reduces the system energy by $\Delta E = q_e(|V_j| - V_c)$ from which the energy consumption can be calculated.

A Threshold Logic Gate (TLG) is a device that is able to compute any linearly separable Boolean function given by:

$$F(X) \quad = \quad sgn\{\mathcal{F}(X)\} = \begin{cases} 0 & \text{if } \mathcal{F}(X) < 0 \\ 1 & \text{if } \mathcal{F}(X) \geq 0 \end{cases} \tag{2}$$

where $\mathcal{F}(X) = \sum_{i=1}^{n} \omega_i x_i - \psi$, x_i are the n Boolean inputs and w_i are the corresponding n integer weights. The TLG performs a comparison between the weighted sum of the inputs $\Sigma_{i=1}^{n}\omega_i x_i$ and the threshold value ψ. If the weighted sum of inputs is *greater than or equal to* the threshold, the gate produces a logic '1'. Otherwise, the output is a logic '0'.

A generic SEEL TLG structure has been proposed in [3] and is depicted in Figure 1(a). In order to reduce the feedback effects that occur in networks of such gates a

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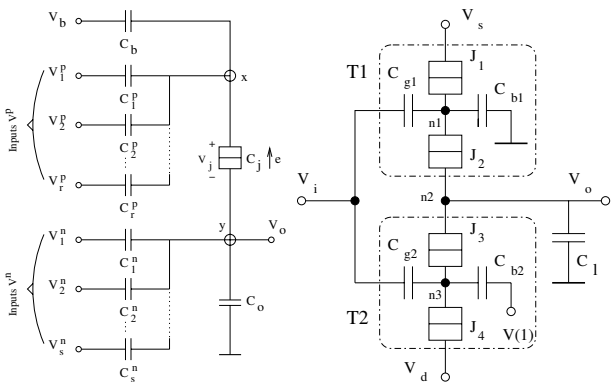

(a) n-input LTG. (b) Static inverting buffer

Fig. 1. Threshold Logic Gate (TLG) and buffer.

static inverting buffer, as depicted in Figure 1(b), was subsequently proposed in [4]. While the static buffer alleviates the feedback effects that may appear in TLG networks it also has an influence on the switching behavior of the gate it buffers. The next section explores the design space of the inverting buffer, focusing primarily on the trade-off between minimizing the buffer delay and minimizing the dynamic feedback from the inverting buffer to the threshold logic gate it shields.

III. Static Inverting Buffer Design Trade-Offs

Let us first assume the followings for the inverting buffer circuit, as depicted in Figure 1(b): logic '0' = V_d = 0 mV, logic '1' = V_b = $V_s \approx q_e/C_l$, and circuit parameters as utilized in [6] and listed on the last row of Table I. The inverting buffer is composed of 2 SET transistors, where the upper transistor $T1$ consists of the circuit elements J_1, J_2, C_{g1}, C_{b1} and the lower transistor $T2$ consists of the circuit elements J_3, J_4, C_{g2}, C_{b2}. When the buffer's output value changes, a charge transport of $1q_e$ occurs through one of these two transistors. The initial tunnel event occurs in either junction J_1 (followed by a tunnel event in junction J_2), or in junction J_4 (followed by a tunnel event in junction J_3). In each of these two cases, the delay associated with the initial tunnel event is approximately one order of magnitude larger than the delay of the second tunnel event, which can be explained as follows. The total capacitive load attached to a transistor island (nodes $n1$ and $n3$) is assumed to be approximately $\frac{1}{2}C_l$. As a result, the critical voltage V_c of each tunnel junction is approximately V_s. Focusing on $T1$, and assuming that the input V_i is logic '0' and that the charges on nodes $n1$ and $n2$ are both 0, the initial tunnel event occurs through J_1. Afterwards, the charge on node $n1$ is q_e while the charge on node $n2$ remains 0. Consequently, the voltage across junction J_2 resulting from the initial tunnel event is approximately $2V_s$, which implies for J_2 that $|V_j| - V_c$ is approximately V_s. In contrast, the initial tunnel event in J_1 is triggered when the input V_i switches between logic '0' and '1'. Given the ratio of the input capacitor C_{g1} to the total capacitive load attached to node n_1, the contribution of V_i to the voltage across junction J_1 is at most $V_s/10$. Consequently, for junction J_1, $|V_j| - V_c$ is an order of magnitude smaller than for J_2 and thus the delay is an order of magnitude larger. We can thus estimate the delay of the inverting buffer by focusing on the initial tunnel event only.

The inverting buffer ideally calculates the following threshold function: $V_o = sgn\{-V_i + V_s/2\}$. In other words, switching equilibrium occurs when the input voltage V_i is equal to the threshold value $1/2V_s$. This situation corresponds with $|V_j| - V_c = 0$, where V_j is the voltage across the junction in which the initial tunnel event occurs and V_c the critical voltage required to enable charge transport. Thus, if the input V_i switches between logic '0' and '1', $|V_j| - V_c$ becomes equal to V_j(V_i = $1/2$ V_s), i.e., the contribution of $V_i = 1/2V_s$ to V_j. The delay of the inverting buffer is inversely proportional to this voltage.

In order to estimate the delay we next assume that charge transport occurs through the upper SET transistor. Note that the same argument applies to charge transport through the lower transistor. Let $C_{\Sigma T1}$ and $C_{\Sigma T2}$ be the total capacitive load attached to the islands of SET transistor T1 and T2 (nodes $n1$ and $n3$), respectively. The input voltage $V_i = 1/2V_s$ thus contributes to the voltage across junction J_1 with an amount $\frac{1}{2}V_sC_{g1}/C_{\Sigma T1}$. Given that the delay is inversely proportional to this voltage contribution, the delay of the inverting buffer can be reduced by increasing V_s and/or increasing C_{g1} and/or reducing $C_{\Sigma T1}$. We consider V_s to be a fixed value that cannot be changed for optimizations because it is a global parameter. Changing it implies that the threshold gate must also be redesigned. Instead, we focus on the effects of changing the other two parameters.

We remind that the inverting buffer shields the threshold gate from the dynamic feedback effects due to switching in other threshold gates driven by the threshold gate under discussion. However, as switching also occurs in the inverting buffer itself, any dynamic feedback effects resulting from this switching must also remain within certain limits. When the buffer output V_o switches between logic '0' and '1', the voltages on nodes n_1 and n_3 changes by $\delta V_{n1} = V_sC_2/C_{\Sigma T1}$ and $\delta V_{n3} = V_sC_3/C_{\Sigma T2}$, respectively. As these nodes are capacitively attached to the threshold gate (by C_{g1} and C_{g2}), they act as virtual (negatively weighted) inputs to the threshold gate. This implies that they become (an undesired) part of the threshold equation calculated by the threshold gate. In the worst case, this can result in the threshold gate calculating an erroneous output value.

C_g	C_1	C_2	C_{b1}	C_3	C_4	C_{b2}
0.5 aF	0.75 aF	0.25 aF	4.5 aF	0.35 aF	0.65 aF	4.4 aF
0.4 aF	0.1 aF	0.2 aF	4.6 aF	0.3 aF	0.1 aF	4.5 aF
0.3 aF	0.1 aF	0.15 aF	4.7 aF	0.25 aF	0.1 aF	4.6 aF
0.2 aF	0.1 aF	0.1 aF	4.8 aF	0.2 aF	0.1 aF	4.7 aF
0.1 aF	0.1 aF	0.15 aF	4.8 aF	0.15 aF	0.1 aF	4.8 aF
0.5 aF (*)	0.1 aF	0.5 aF	4.25 aF	0.1 aF	0.5 aF	4.25 aF

TABLE I

CIRCUIT PARAMETERS FOR INVERTING BUFFER IMPLEMENTATIONS.

Assuming that this does not occur, the contributions of δV_{n1} and δV_{n3} to the voltage across the threshold gate's tunnel junction can significantly reduce $|V_j|-V_c$, resulting in *an increased delay in the TLG part* of the compound gate. Focusing on the upper SET transistor, we observe that the amount of dynamic feedback can be reduced by reducing C_{g1} and C_2, and/or increasing $C_{\Sigma T1}$, but this also results in *an increased delay in the buffer part* of the compound gate. Given that the buffer is the faster of the two components, we propose to reduce the dynamic feedback such that its effect on the delay of the TLG part can be ignored.

The dynamic feedback effects of the voltages δV_{n1} and δV_{n3} are evaluated as follows. Each threshold gate input contributes to the voltage V_j across the threshold gate's tunnel junction. The contribution of δV_{n1} and δV_{n3} should be significantly smaller than the smallest contribution of an input, which can be evaluated by calculating their ratio r. Assume that ω_s is the threshold gate weight with the smallest absolute value. If the sign of ω_s is negative and C^n is the capacitor implementing this weight (thus resulting in the smallest input contribution to V_j) the ratio r is calculated as:

$$r = \frac{C_2 C_{g1}}{C_{\Sigma T1} C^n} + \frac{C_3 C_{g2}}{C_{\Sigma T2} C^n} \tag{3}$$

If the sign of ω_s is positive and C^p is the capacitor implementing this weight (thus resulting in the smallest input contribution to V_j) the ratio r is calculated as:

$$r = \frac{C_2 C_{g1} C^p_\Sigma}{C_{\Sigma T1} C^p C^n_\Sigma} + \frac{C_3 C_{g2} C^p_\Sigma}{C_{\Sigma T2} C^p C^n_\Sigma} \tag{4}$$

where C^p_Σ and C^n_Σ are the sum of all the capacitors attached to nodes x and y of the threshold gate, respectively (see Figure 1(a)). Given that in general $C^p_\Sigma > C^n_\Sigma$ [3], a threshold gate whose smallest weight has a positive sign is more susceptible to dynamic feedback from its buffer.

Given that the dynamic feedback from the buffer to the threshold gate varies within a range of values (between 0 and $\delta V_{n1} + \delta V_{n3}$), the threshold gate can be biased such that it compensates for the median value. This compensation limits the dynamic feedback effect by a factor of 2. If, for example, we design a buffered threshold gate with $r = 0.2$, this results in the worst case in a 10% reduction of $|V_j| - V_c$ of the threshold gate, which in turn implies an increase in the threshold gate's delay of approximately 10%.

We next propose a set of inverting buffer implementations with varying equal sized input capacitors C_g (where $C_{g1} = C_{g2} = C_g$). Each of these designs is based on the following assumptions. We assume that the smallest weight of the threshold gate has a negative sign and that the capacitor implementing this weight is equal to the buffer's input capacitor ($C^n = C_g$). We next assume a maximum ratio $r = 0.1$, which implies that the threshold gate's delay may increase with at most 5%. In order to simplify the delay calculations we can ignore this added delay. Resulting, each inverting buffer design should satisfy the following:

$$\frac{C_2}{C_{\Sigma T1}} + \frac{C_3}{C_{\Sigma T2}} < 0.1 \tag{5}$$

C_g	Feedback Ratio	Delay	Energy
0.5 aF	0.1	0.44 ns	8.8 meV
0.4 aF	0.1	0.49 ns	7.5 meV
0.3 aF	0.08	0.65 ns	7.5 meV
0.2 aF	0.06	0.96 ns	7.4 meV
0.1 aF	0.06	1.90 ns	7.6 meV
0.5 aF (*)	0.19	0.39 ns	10.9 meV

TABLE II

FEEDBACK RATIO AND DELAY FOR VARIOUS BUFFERS.

A set of five inverting buffers that each satisfy the above constraints has been designed and tested. The input capacitor C_g was varied from $0.1aF$ to $0.5aF$ with increments of $0.1aF$. The circuit parameters for the resulting five inverting buffer implementations are summarized in Table I. Note that each design has an output capacitor $C_l = 9.5aF$ and that the supply voltage is $V_s = 16mV$. We also added the inverting buffer design (marked by a '*') utilized earlier in [6]. For each design we calculated the ratio of dynamic feedback to the regular input signal, the delay and the energy consumption. The results of these calculations are summarized in Table II.

Each of the inverting buffer designs was verified by means of simulation using the SET simulation package SIMON [8] and the simulation results are depicted in Figure 2. The top bar represents the input signal V_i, which is the same for all the designs. Although during normal operation the input signal of the inverting buffer is a Boolean value as described above, we have represented V_i

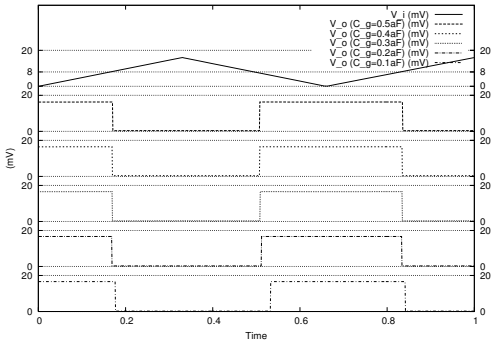

Fig. 2. Simulation results for the 5 inverting buffer implementations.

as a continuous signal. This demonstrates that the output of each of the inverting buffers switches when the input is approximately $1/2V_s$ or $8mV$. Notice that a slight amount of hysteresis can be observed (less then 5% of V_s), which can be ignored for our calculations.

In order to demonstrate the effect of using various inverting buffers in conjunction with a threshold gate we implemented a buffered threshold gate that calculates the following threshold equation: $Y = sgn\{4a + 2b + 2c + d + e - 4\}$. Given that the buffer inverts the threshold gate's output, the above threshold equation is implemented with a threshold gate calculating $\overline{Y}$. Inverted threshold equations can be derived by inverting the sign of each weight, and by subtracting one from the threshold value and inverting the result. Consequently, the threshold gate calculates $\overline{Y} = sgn\{-4a-2b-2c-d-e+3\}$. For this gate the following circuit parameters were assumed: $C_1^n(\omega = -4) = 0.8aF$, $C_2^n(\omega = -2) = C_3^n(\omega = -2) = 0.4aF$, $C_4^n(\omega = -1) = C_5^n(\omega = -1) = 0.2aF$, $C_o = 7.8aF$, $C_j = 0.1aF$. The voltage levels for logic signals and the supply voltages remain as stated above. During the experiments we maintained $a = b = 0$ and $c = d = 1$, while e was varied from 0 to 1 and back to 0.

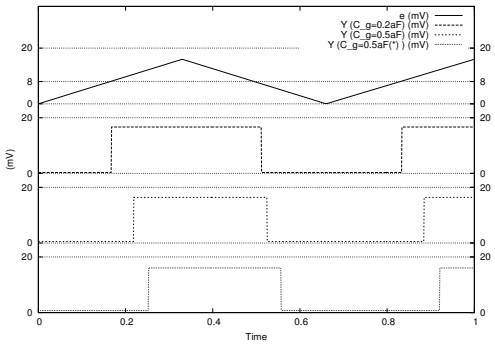

Fig. 3. Buffered threshold gate simulation results (3 different buffers.)

We implemented the threshold gate using three different buffers from Table I, i.e., $C_g = 0.2aF$, $C_g = 0.5aF$, and the initial buffer $C_g = 0.5aF(*)$, which resulted in $C_b = 12.4aF$, $C_b = 12.3aF$ and $C_b = 12.3aF$, respectively. The simulation results are depicted in Figure 3. Utilizing Equation (3), we calculated that the feedback ratios resulting from the three buffers are $r = 0.06$, $r = 0.25$, and $r = 0.48$, respectively. The increasing feedback ratio results in increasing amounts of hysteresis in the transfer function, as observed from the simulation results. Ideally, the threshold gate outputs should switch when the input e is exactly $1/2V_s$ $(8mV)$. Focusing on the bottom bar in the figure, which has the largest feedback ratio, one can observe that in this case the output switches from '0' to '1' when the input is approximately $3/4V_s$, while the output switches from '1' to '0' when the input is approximately $1/4V_s$.

IV. Conclusions

This paper proposed a method to design optimized buffered Threshold Logic Gates (TLGs). First, we analyzed the impact of the buffer on the TLG switching behavior. Second, we proposed a general buffer design methodology. Third, we derived a set of buffers and demonstrated their impact on a TLG through an example. We observed that the amount of dynamic feedback originating from the inverting buffer depends on the inverting buffer itself and on the size of the input capacitors of the threshold gates. Our experiments suggested that one should generally select a buffer whose input capacitors are similar in size to those of the threshold gate. The amount of dynamic feedback that can be accepted depends on various parameters, such as the number of threshold gate inputs and their signal quality. For threshold gates with low fanin, e.g., 2-input Boolean gates, larger feedback ratios can be tolerated. For threshold gates with high fanin one has to be more careful when selecting the buffer.

References

[1] K. Likharev, "Single-Electron Devices and Their Applications," *Proceeding of the IEEE*, vol. 87, no. 4, pp. 606–632, April 1999.

[2] Y. Nazarov and S. Vyshenskii, "SET Circuits for Digital Applications," in *Single-Electron Tunneling and Mesoscopic Devices*, ser. Springer Series in Electronics and Photonics. Springer-verlag, 1992, vol. 31, pp. 61–66.

[3] C. Lageweg, S. Cotofana, and S. Vassiliadis, "A Linear Threshold Gate Implementation in Single Electron Technology," in *IEEE Computer Society Workshop on VLSI*, April 2001, pp. 93–98.

[4] ——, "Static Buffered SET Based Logic Gates," in *2nd IEEE Conference on Nanotechnology (NANO)*, August 2002, pp. 491–494.

[5] ——, "Binary Addition based on Single Electron Tunneling Devices," in *4th IEEE Conference on Nanotechnology (NANO)*, August 2004.

[6] ——, "Single Electron Encoded Latches and Flip-Flops," *IEEE Transactions on Nanotechnology*, vol. 3, no. 2, pp. 237–248, June 2004.

[7] C. Wasshuber, "About single-electron devices and circuits," Ph.D. dissertation, TU Vienna, 1998.

[8] C. Wasshuber, H. Kosina, and S. Selberherr, "SIMON - A Simulator for Single-Electron Tunnel Devices and Circuits," *IEEE Transactions on Computer-Aided Design*, vol. 16, no. 9, pp. 937–944, September 1997.