Design Methodology for Single Electron Based Building Blocks

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***Abstract*— This paper investigates the design process of Single Electron Tunneling (SET) based building blocks in which logic values are represented by single or few electrons. A design methodology is proposed that, given a circuit topology and the corresponding targeted behavior, assists the circuit designer in deriving the circuit parameters in an analytical way. The methodology, based on the mathematical description of the tunnel junctions in the circuit, allows for a time effective design of SET based building blocks. Moreover the method allows for the adaptation of such blocks for the utilization in larger SET circuits. During the presentation we use a Move k electron ($MVke$) block as a discussion vehicle but the approach we propose is general and can be utilized for any SET topology.**

***Index Terms*— single electron tunneling, design methodology.**

I. Introduction

It is generally expected that current semiconductor technologies, i.e., CMOS, cannot be pushed beyond a certain limit because of problems arising in the area of power consumption and scalability. A promising alternative is Single Electron Tunneling (SET) technology [1], which has the potential of performing computation with lower power consumption than CMOS and is scalable to the nanometer region and beyond.

Several proposals have been made to implement computational operations using SET technology and these implementations are mainly categorized in two types (see for example [1], [2]). The first type of implementation represents logic values by voltage (see [2] for an overview) while the second type of implementation represents bits by single electrons. Single Electron Encoded Logic (SEEL) [3], [4] and the Electron Counting (EC) circuits [5], [6] are examples of the latter.

Although the principles of electron tunneling have been known since the twenties, it has only been in the last decade that a few circuits using SET technology have been designed. Since SET technology is different from MOS technology, existing design methodologies are not applicable. Additionally, CAD tools are not available and only a small number of simulators exist [7], [8]. Therefor the design of SET circuits is generally done by hand. This paper provides a design methodology, focussed on SEEL and EC implementations, for deriving the circuit parameters of SET based building blocks. A SET building block is a small circuit consisting of a few (typically between one and four) tunnel junctions and some other circuit elements (like capacitor's, voltage sources, etc.) which performs an elementary operation and can be connected to other building blocks to perform more complex operations. The proposed design methodology allows for a time effective design of SET based building blocks. Additionally, blocks that have been designed according to the methodology can easily be adapted for utilization in different circuits.

The remainder of this paper is organized as follows. Section II briefly describes the SET phenomenon and describes a SET building block, which is used as example throughout this paper. In Section III the six steps of the design methodology are presented. Section IV concludes the paper.

II. Background

SET circuits are based on tunnel junctions which consist of an ultra-thin insulating layer in a conducting material. In classical physics no charge transport is possible through an insulator. However, when the insulating layer is thin enough the transport or *tunneling* of charge can happen in a discrete and accurate manner, i.e., one electron at a time, if it reduces the amount of energy in the system. Tunneling through a junction becomes possible when the junction's current voltage V_j exceeds the junction's critical voltage $V_c = \frac{q_e}{2(C_e+C_j)}$ [9], where $q_e = 1.602 \cdot 10^{-19}C$, C_j is the capacitance of the tunnel junction and C_e is the capacitive value of the remainder of the circuit as seen from the junction. In other words, tunneling can occur if and only if $|V_j| \geq V_c$, in which case the junction is called unstable.

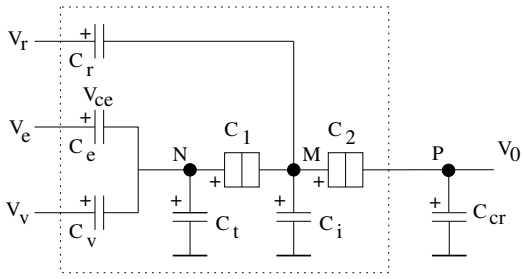

Fig. 1. $MVke$ block implementation.

The design methodology is explained using the Move k electron ($MVke$) building block [10] depicted in Figure 1 as example circuit. The $MVke$ building block operates as follows. The enable signal V_e is used to set the voltage over junction 1 (C1) close to its critical voltage while the voltage over junction 2 (C2) stays below its critical

voltage. If input V_v is zero no tunnel event will occur, but if V_v is larger than zero the voltage over junction 1 exceeds its critical voltage and k electrons tunnel from node P to node N. The value of k is proportional to the magnitude of V_v. If V_r ='1' while the other inputs are zero, all the transported electrons return to node P and thus the circuit is reset to its charge neutral state.

III. The Design Methodology

When designing SET based building blocks one starts with a targeted behavior for which an appropriate circuit topology has to be sought. After such a topology was proposed the designer has to find the appropriate circuit parameters that allow the topology to deliver the targeted behavior under certain boundary conditions imposed by the context where the block will be utilized. The methodology we propose assists the designer in finding these circuits parameters in a systematic way. It consists of the following steps:

1) **Derive the characteristic equations** for all junctions in the circuit.
2) **Derive the operation modes**, given the targeted behavior and the circuit topology.
3) **Solve the characteristic equations** for each operation mode, in order to obtain the parameter relations that have to be satisfied in to obtain the corresponding behavior.
4) **Derive the circuit parameters**, given a set of boundary conditions.
5) **Determine the upper bounds** for correct operation.
6) **Verify the design**.

In the remainder of this section the steps of the methodology are explained in detail using the $MVke$ building block as a discussion vehicle.

A. Deriving the Characteristic Equations

The behavior of a SET circuit is mainly determined by the behavior of the tunnel junctions. Thus the behavior can be described by a set of equations describing the voltages across the junctions. For each and every junction one equation can be derived and we call these equations the *characteristic equations* of the building block.

The characteristic equations can be derived by performing the following steps:

- Derive the basic equations describing the charges on the capacitors, tunnel junctions and the circuit nodes.
- For each junction, choose a voltage relation to start the derivation.
- Specify which parameters are known and which are the unknown parameters that are relevant for the design of the circuit.
- Starting from the chosen voltage relation, eliminate all the non-relevant parameters.

The basic equations for the $MVke$ building block are:

$$\begin{aligned} q_1 &= C_1 V_1 \quad & q_r &= C_r[V_r - V_2 - V_0] \\ q_2 &= C_2 V_2 \quad & q_i &= C_i V_i = C_i[V_2 + V_0] \\ q_v &= C_v[V_v - V_t] & q_{ce} &= C_e V_{ce} \\ q_t &= C_t V_t & q_{cr} &= C_{cr} V_0, \end{aligned} \tag{1}$$

where V_1, V_2, V_t, V_i are the voltages across capacitors C_1, C_2, C_t, C_i, respectively. The charges in the circuit nodes are described by:

$$q_m = q_2 - q_1 + q_i - q_r = -mq_e + q_{0m} \tag{2}$$

$$q_n = q_1 + q_t - q_v - q_{ce} = -nq_e + q_{0n} \tag{3}$$

$$q_p = q_{cr} - q_2 = -pq_e + q_{0p}, \tag{4}$$

where m, n, p are the number of electrons and q_{0m}, q_{0n}, q_{0p} are the background charges present at nodes M, N, P, respectively. The background charge is a random offset charge induced by stray capacitances and impurities located near the circuit nodes [2]. They are stated here for correctness, but are omitted in the remainder of this paper for studying the effects of random background charge is beyond the scope of this paper.

A good voltage relation to start the derivation of the junction 1 characteristic equation should at least contain an important input voltage, the voltage across the investigated junction, and as many other voltages across junctions as possible. Thus for the topology of the $MVke$ block we chose the following voltage relation for the derivation of both characteristic equations: $V_e = V_{ce} + V_1 + V_2 + V_0$.

The next step is to specify which parameters are known and wether parameters are relevant or not. In general all input voltages, capacitances and charges on nodes, and the voltage across the investigated junction are relevant. All other parameters, including output voltages, are non-relevant in this context as they can be eliminated from the characteristic equation(s). In order to illustrate the above, Table I lists the parameters that may be considered for the characteristic equation of junction 1 and their status.

known	*unknown*	
	relevant	*non-relevant*
V_v, V_e, V_r, C_{cr}	C_1, C_2, C_r, C_v, C_e, C_t, C_i, q_m, q_n, q_p, V_1	q_1, q_2, q_r, q_v, q_{ce}, q_t, q_i, q_{cr}, V_{ce}, V_t, V_i, V_0, V_2

TABLE I

Categorization of the parameters of the $MVke$ block.

The last step of the derivation of the characteristic equations is to eliminate all non-relevant parameters from the voltage relation, which is demonstrated for junctions 1 and 2 as follows.

Junction 1: The elimination of the non-relevant parameters from the start point voltage relation is done by subsequent substitution with the basic equations. It implies mathematical manipulation and can be done in different

ways, using the following procedure. First substitute the non-relevant voltages from the start point voltage relation for capacitances and charges, using the basic equations stated in Equation (1). Second, eliminate the resulting non-relevant charges using Equations (2) - (4).

In order to improve readability the following notations are introduced:

$$C_{\Sigma n} = C_v + C_e + C_t \tag{5}$$

$$C_{\Sigma m} = C_1 + C_2 + C_r + C_i \tag{6}$$

$$r_\alpha = \frac{C_2 + C_{cr}}{C_2 C_{cr}}[C_i + C_r] + 1 \tag{7}$$

$$r_\beta = \frac{C_2 + C_{cr}}{C_2 C_{cr}}[C_i + C_r + C_1] + 1. \tag{8}$$

The characteristic equation for junction 1 can thus be expressed as:

$$V_1 = \frac{r_\alpha \frac{C_e}{C_{\Sigma n}} V_e - \frac{C_2+C_{cr}}{C_2 C_{cr}} C_r V_r + \frac{r_\alpha}{C_{\Sigma n}} C_v V_v - \frac{q_p}{C_{cr}}}{r_\beta + \frac{r_\alpha C_1}{C_{\Sigma n}}} + \frac{-\frac{C_2+C_{cr}}{C_2 C_{cr}} q_m + \frac{r_\alpha}{C_{\Sigma n}} q_n}{r_\beta + \frac{r_\alpha C_1}{C_{\Sigma n}}} \tag{9}$$

Junction 2: The categorization of the parameters for junction 2 is similar to that presented in Table I, except that V_1 is non-relevant while V_2 is relevant. The characteristic equation for junction 2 can thus be expressed as:

$$V_2 = \frac{[C_e V_e + C_v V_v + q_n] C_1 + [C_{\Sigma n} + C_1][q_m + C_r V_r]}{[C_{\Sigma n} + C_1]\left\{[C_{\Sigma m} - C_1] + \frac{C_2}{C_{cr}}[C_i + C_r]\right\}} \frac{-\{[C_{\Sigma n} + C_1][C_i + C_r] + C_{\Sigma n} C_1\}\frac{q_p}{C_{cr}}}{+ C_{\Sigma n} C_1\left[1 + \frac{C_2}{C_{cr}}\right]} \tag{10}$$

B. Deriving the Operation Modes

For every building block several modes can be distinguished which determine the basic operations performed by the circuit. The operation modes can be derived in a straightforward manner based on the targeted behavior and the circuit topology. For each mode the targeted behavior of the circuit (i.e., which tunnel events should occur) should be described. For our example, the $MVke$ building block, four modes of operation are possible as described below.

Enabled-mode: In the enabled-mode, the input V_e is $'high'$, the other inputs V_v and V_r are $'low'$ while no electrons have tunnelled yet, i.e., all internal nodes are in a neutral state ($q_n = q_m = q_p = 0$). When the circuit is in the enabled-mode, no tunnel events should take place, but the voltage over junction 1 should be very close to its critical voltage. Therefor the voltage across junction 1 is its critical voltage minus a small value ϵ.

Move-mode: In the move-mode inputs V_e and V_v are $'high'$ and input V_r is $'low'$. The critical voltage of junction 1 should be exceeded so that an amount of electrons will tunnel from node P to node N. We denote the number of electrons we want to transport, for a value of V_v, by k and the actual amount of tunnelled electrons by n. The targeted behavior can now be described as instability for $n < k$ and stability for $n = k$ ($n > k$ should not be allowed).

Hold-mode: The third mode of operation of the $MVke$ block is the hold-mode, in which the input V_e is $'high'$ and the other inputs V_v and V_r are $'low'$, like in the enabled-mode. The difference between the hold-mode and the enabled-mode is that k electrons have tunnelled from node P to node N. These electrons should remain in their position in node N, therefor the targeted behavior can be described as stability for $n = k$ and $p = -k$.

Reset-mode: The last mode is the reset-mode, in which only the reset input V_r is $'high'$ while all other inputs are $'low'$. The objective of this mode is that all tunnelled electrons return to their original position, as a result of which the charges on nodes N, M and P will all become zero. The targeted behavior can be described as instability for $n > 0$ and stability for $n = 0$.

C. Solving the Characteristic Equations

The next step of the methodology is to derive the relations that have to be satisfied in order to obtain the targeted behavior in each mode. To do this for each mode the input values, the inner state of the circuit and the specified targeted behavior are substituted in the characteristic equations. This process produces the relations we are looking for. The move-mode of the example circuit is discussed in detail. For the other three modes the derivation can done in a similar way [11].

Move-mode: For the move-mode the targeted behavior is described as instability for $n < k$ and stability for $n = k$. Substitution of these conditions together with the input values in Equation (9) results in two equations:

$$\frac{[C_{\Sigma m} - C_1]}{C_{\Sigma n}}[C_e V_e + C_v V_v - n q_e] - \frac{C_2}{C_{cr}} n q_e > V_{c1} C_{\Sigma m} \text{ for } n < k \tag{11}$$

$$\frac{[C_{\Sigma m} - C_1]}{C_{\Sigma n}}[C_e V_e + C_v V_v - n q_e] - \frac{C_2}{C_{cr}} n q_e < V_{c1} C_{\Sigma m} \text{ for } n = k. \tag{12}$$

While performing this step of the methodology for the enabled-mode, an expression for C_e was derived [11] and its substitution in the equations above results in:

$$\frac{[C_{\Sigma m} - C_1]}{C_{\Sigma n}}[C_v V_v - n q_e] - \frac{C_2}{C_{cr}} n q_e > \epsilon \text{ for } n < k \tag{13}$$

$$\frac{[C_{\Sigma m} - C_1]}{C_{\Sigma n}}[C_v V_v - n q_e] - \frac{C_2}{C_{cr}} n q_e < \epsilon \text{ for } n = k. \tag{14}$$

From these equations and from the description of the targeted behavior, it can be observed that stability occurs if the n transported electrons have compensated for the contribution of the input V_v to the voltage over junction 1. This condition can be stated as follows:

$$\frac{[C_{\Sigma m} - C_1]}{C_{\Sigma n}}[C_v V_v - n q_e] - \frac{C_2}{C_{cr}} n q_e = 0 \tag{15}$$

Rewriting this equation and substituting k for n we obtain:

$$C_v V_v = \left[\frac{C_2}{C_{cr}} \frac{C_{\Sigma n}}{[C_{\Sigma m} - C_1]} + 1 \right] k q_e \quad (16)$$

from which we can derive the value for C_v.

The threshold between stability and instability should be between the last but one and the last tunneling electron. The value ϵ acts as a threshold and should therefor be set to half the contribution of one electron.

$$\epsilon = \frac{1}{2} q_e \left[\frac{C_2}{C_{cr}} + \frac{[C_{\Sigma m} - C_1]}{C_{\Sigma n}} \right] \quad (17)$$

In the move-mode, the equation for junction 2 is of no importance, although due to tunnel events on junction 1, k electrons tunnel from node P through junction 2 towards node N. Note that after the transport of k electrons the charge distribution is $-k$, 0, k for nodes N, M, P, respectively.

D. Deriving the Circuit Parameters

The fourth step of the methodology is to derive the circuit parameters given a set of boundary conditions. This is done by substituting the values of the boundary conditions into the equations derived in the previous step.

For the $MVke$ example we assume that the block has to move 16 electrons when $V_v = 16$ mV and we assume that $V_e('high') = V_e('high') = 16$ mV and $C_{cr} = 10^{-14}$ F. In compliance with previous research, specifically [6], [10], we utilize the following parameter values: $C_1 = C_2 = 0.5$ aF, $C_{\Sigma m} = 10$ aF, $C_{\Sigma n} = 1000$ aF. Substitution of these values in the equations derived in step three resulted in the following parameter values: $C_e = 527$ aF, $C_v = 161$ aF, $C_t = 312$ aF, $C_r = 5.00$ aF, $\epsilon = 7.65 \cdot 10^{-22}$ C.

E. Determining the Upper Bounds

In Section III-C it was explained how to derive the relations that have to be satisfied in order to obtain the targeted behavior. In general this process also delivers some equations describing a limit to the operation. To prevent the circuit from incorrect behavior, these limits should be evaluated. How this is done depends on the nature of the limit. In general it is a matter of manipulating the equations into an useful and comprehensible equation.

While performing step three of the methodology for the $MVke$ block the following expression was derived, which gives an upper limit for k, the number of electron that can be moved by the block.

$$k q_e \left[\frac{C_1}{C_{\Sigma n}} + \frac{C_i + C_r + C_1}{C_{cr}} \right] < V_{c2} C_{\Sigma m} + C_e V_e \frac{C_1}{C_{\Sigma n}} \quad (18)$$

Note that this limit is derived for the $MVke$ block as a stand alone circuit element. When connecting this block to other circuits one has to take into account the dynamic feedback caused by the other blocks. For example, the charge reservoir C_{cr} at the output of the $MVke$ block might be connected to other blocks that also remove electrons from the reservoir, resulting in a larger positive voltage on the output than accounted for in the equations above, which will decrease the limit. For the $MVke$ block, using the parameters from Section III-D, we obtained an upper limit for k of 529 and utilization of this $MVke$ implementation in the EC based adder proposed in [10] allows for up to 9-bit addition in a depth-2 network.

F. Verifying the Design

The last step of the methodology is the verification of the design through simulation. For the simulation of the $MVke$ block we used the simulator SIMON [9], [7]. The $MVke$ block, was simulated using the parameters that were derived in Section III-D. The simulation proved that the circuit functions correctly and moves exactly 16 electrons from the reservoir for $V_v = 16$ mV.

IV. Conclusion

This paper investigated the design process of Single Electron Tunneling (SET) based building blocks in which logic values are represented by single or few electrons. A design methodology was proposed that, given a circuit topology and the corresponding targeted behavior, allows for the derivation of the circuit parameters in an analytical way. The methodology is based on the mathematical description of the tunnel junctions of the circuit, called the characteristic equations. As future work we intend to implement the proposed methodology in a CAD tool.

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