Computing Periodic Symmetric Functions in Single Electron Tunneling Technology

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Abstract
This paper investigates the implementation of Periodic Symmetric Functions (PSF) in single electron tunneling technology. First, a building block is proposed that performs a multiple input PSF. The block we propose can be used for the computation of any function that is or can be expressed as a PSF, thus it can be utilized for the implementation of a large number of arithmetic operations, e.g., parity, addition, multi-operand addition, as they belong to the class of generalized PSFs. Subsequently, a PSF based addition scheme is proposed and it is demonstrated how this adder can be used in a Single Electron Encoded Logic (SEEL) environment. Finally, a 3-bit instance of the addition scheme is presented and verified by means of simulation.
Keywords**:** *single electron tunneling, periodic symmetric function.*

1. INTRODUCTION

It is generally expected that current semiconductor technologies, i.e., CMOS, cannot be pushed beyond a certain limit because of problems arising in the area of power consumption and scalability. A promising alternative is Single Electron Tunneling (SET) technology [1], which has the potential of performing computation with lower power consumption than CMOS and it is scalable to the nanometer region and beyond [2].

Several proposals have been made to implement computational operations using SET technology and these implementations are mainly categorized in two types (see for example [1], [3]). The first type of implementation represents logic values by voltage (see [3] for an overview) while the second type of implementation represents bits by single electrons. Single Electron Encoded Logic (SEEL) [4] is an examples of the latter.

Thus far most implementations focussed on designing logic gates to perform operations in the digital domain. SET technology however, possesses properties, e.g. Coulomb oscillations, that open new avenues for the implementation of logic and arithmetic functions. In this line of reasoning we assume in this paper a basic SET structure, the electron trap, that exhibits a periodic behavior and use it as a basis for the implementation of Periodic Symmetric Functions (PSFs). As a large number of arithmetic operations, including addition and parity check, can be expressed as PSFs, such a building block can be used to compute a variety of mathematical operations.

The remainder of this paper is organized as follows. Section 2 briefly describes the SET phenomenon and provides some background on symmetric functions. In Section 3 a building block is proposed that performs a multiple input generalized periodic symmetric function. Using this building block in Section 4 a PSF addition scheme is proposed and it is described how this scheme can be adjusted to operate in a SEEL environment. In Section 5 the design and simulation of a 3-bit PSF adder is presented. In Section 6 some practical considerations are discussed and Section 7 concludes the paper.

2. BACKGROUND AND PRELIMINARIES

SET circuits are based on tunnel junctions which consist of an ultra-thin insulating layer in a conducting material. In classical physics no charge transport is possible through an insulator. However, when the insulating layer is thin enough the transport or tunneling of charge can happen in a discrete and accurate manner, i.e., one electron at a time, if it reduces the amount of energy in the system. Tunneling through a junction becomes possible when the junction's current voltage V_j exceeds the junction's critical voltage $V_c = \frac{q_e}{2(C_e+C_j)}$ [5], where $q_e = 1.602 \cdot 10^{-19}C$, C_j is the capacitance of the tunnel junction, and C_e is the capacitive value of the remainder of the circuit as seen from the junction. In other words, tunneling can occur if and only if $|V_j| \geq V_c$, in which case the junction is called unstable. Electron tunneling is stochastic in nature and as such the delay cannot be analyzed in the traditional sense. Instead, for each transported electron one can describe the switching delay as $t_d = \frac{-ln(P_{error})q_eR_t}{|V_j|-V_c}$, where R_t is the junction's resistance and P_{error} is the chance that the desired charge transport has not occurred after t_d seconds. In this paper we assumes $R_t = 10^5\Omega$ and $P_{error} = 10^{-8}$.

Note that the implementations discussed in here are technology independent. SET tunnel junctions can for example be implemented by classical semiconductor lithography and by carbon nanotubes [6]. Therefore, circuit area is evaluated in terms the total number of circuit elements (capacitors and junctions).

A Boolean function of n variables F_s, is symmetric if and only if for any permutation σ of $< 1, 2, ..., n >$, $F_s(x_1, x_2, ..., x_n) = F_s(x_{\sigma(1)}, x_{\sigma(2)}, ..., x_{\sigma(n)})$. In other words, a Boolean symmetric function entirely depends on the sum of its input values

$F_s(x_1, x_2, ..., x_n) = F_s(\sum_{i=1}^{n} x_i)$. A generalized symmetric function $F_g(X)$ is a function that depends on the weighted sum of its inputs $X = (\sum_{i=1}^{n} x_i w_i)$, where w_i is the weight of input x_i.

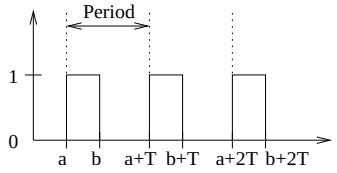
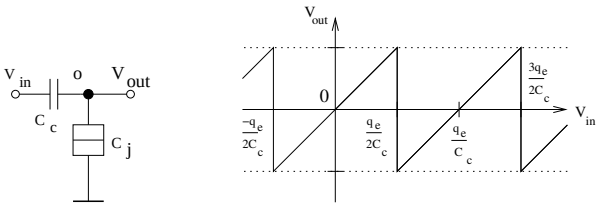


Fig. 1. Periodic Symmetric Function.

A periodic symmetric function is a symmetric function for which there exists a period T such that $F_s(X) = F_s(X + T)$. A PSF is completely defined by the constants a, b and T, where a is the first positive transition and b is the first negative transition (see Figure 1).



(a) Circuit. (b) Transfer function.

Fig. 2. SET electron trap.

A well know SET structure is the electron trap depicted in Figure 2 which has a periodic transfer function. The SET electron trap functions as follows. If the input voltage rises, the output voltage follows due to capacitance division. At some point, though, the voltage across the tunnel junction exceeds the critical voltage and an electron tunnels to the output node. The output voltage therefore drops. As the input voltage continues to rise, the output voltage rises again until it reaches the critical voltage.

The relation between the input voltage V_{in} and the output voltage V_{out} of the electron trap can be derived as

$$V_{in} = \frac{C_{\Sigma o}}{C_i} V_{out} + \frac{q_o}{C_i}, \tag{1}$$

where $C_{\Sigma o}$ is the sum of all capacitances connected to node o and q_o is the net charge in node o. The critical voltage of the tunnel junction is expressed as $V_c = \frac{q_e}{2C_{\Sigma o}}$. We know from the description of the electron trap, that the output voltage reaches its maximum when this voltage reaches the critical voltage of the tunnel junction. Thus, by substituting the expression of the critical voltage into Equation (1), the input voltage for which the output voltage reaches its maximum can be expressed as:

$$V_{i,peak} = \frac{q_e}{2C_i} + \frac{kq_e}{C_i} \quad \text{for } k = 0, 1, 2, ... \tag{2}$$

This equation suggests that the period of the electron trap transfer function is dependent only on the magnitude of capacitance C_i, while the capacitance of the tunnel junction has no influence.

3. MULTIPLE INPUT PSF BUILDING BLOCK

The SET electron trap can be used as a basis for a building block that performs a PSF, though two extensions are needed. First, the number of inputs of the electron trap needs to be increased. Second, the triangular transfer function of the electron trap needs to be converted to a rectangular one.

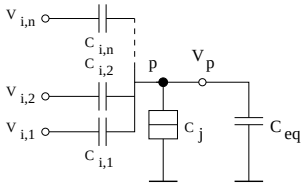


Fig. 3. Multiple input SET electron trap.

Figure 3 presents a modified electron trap, which allows for multiple inputs to drive it in the same time. The capacitance C_{eq} represents the equivalent capacitance of the circuit connected to the output (V_p) of the electron trap. Every input $V_{i,x}$ contributes to the output voltage according to the following expression

$$V_{p,x} = \frac{C_{i,x}}{C_{\Sigma p}} V_{i,x}, \tag{3}$$

where $C_{\Sigma p} = \sum_{x=1}^{n} C_{i,x} + C_j + C_{eq}$ is the total capacitance connected to node p. The total output voltage is the sum of the contributions of all inputs $V_p = \sum_{x=0}^{n} V_{p,x}$.

From Equation (3) it can be observed that every input $V_{i,x}$ is contributing to the voltage on node p according to the size of capacitor $C_{i,x}$. Thus by choosing different values for $C_{i,x}$, inputs can be given different weights. Let $V_{i,high}$ be the input voltage representing logic '1' and let w_x be the weight of input x, the corresponding capacitance of input x can be evaluated as:

$$C_{i,x} = \frac{q_e}{2 w_x V_{i,high}}. \tag{4}$$

To obtain a rectangular shape transfer function we connect to the output of the electron trap a static inverting buffer [4], which then acts as a literal gate. The resulting topology, called the multiple input PSF block is depicted in Figure 4.

The reader should notice that in the multiple input PSF block, one of the inputs of the electron trap is connected to the supply voltage through the capacitor

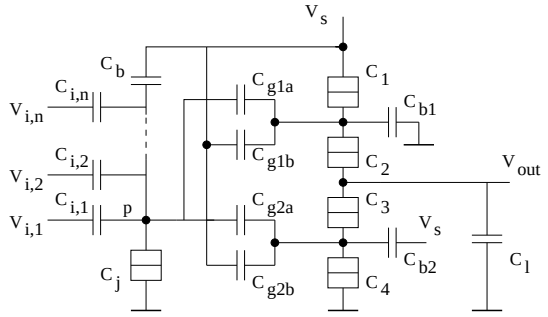
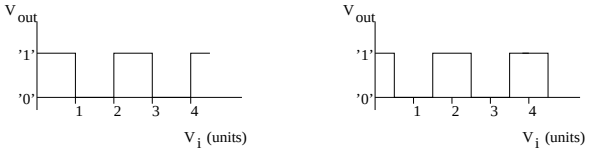


Fig. 4. The multiple input PSF implementation.

C_b. This input causes a bias on node p of the electron trap, which is added for the following reason. Assuming an electron trap with only one input and no bias, the transfer function would be as depicted in Figure 5(a). From the transfer function it is seen that the first negative transition is located at exactly an input voltage corresponding to one unit. If, due to various effects (cross-talking, impurities, parameter deviation, etc.) the input voltage is a little less than the voltage corresponding to one unit, the output of the PSF block would be logic '1' instead of the expected logic '0'.



(a) without bias. (b) with bias.

Fig. 5. PSF block transfer function.

The addition of the bias, with a magnitude of half a unit, causes all transitions to move to the left by a half unit (see Figure 5(b)). Consequently, the first negative transition has moved from an input of one unit to a half unit and in this way the structure is less sensitive to parameter variation, etc. Note that the input, though analog, is discrete in nature and only takes values of whole units. Therefore, adding a bias of a half unit results in maximal robustness of the implementation.

4. PSF ADDITION SCHEME

Binary addition can be seen as a periodic symmetric function, more precisely every output bit of the addition can be described as a generalized periodic symmetric function of the inputs. When adding two binary numbers $A = \{a_{n-1}, ..., a_1, a_0\}$ and $B = \{b_{n-1}, ..., b_1, b_0\}$ the result is a sum $S = \{s_n, ..., s_1, s_0\}$. Each sum bit s_i can be calculated with a periodic symmetric function F_s as:

$$s_i = F_s(\sum_{k=0}^{i} 2^i(a_i + b_i)) \quad (5)$$

where the period of F_s is $T = 2^{i+1}$. Thus a PSF addition scheme can be build by utilizing a multiple input PSF block for each and every output bit and connecting to it all the necessary inputs using the proper weights. For example, the multiple input PSF block producing output bit s_0 has a period $T = 2$, is connected to inputs a_0 and b_0, which both have a weight of 1. Using Equation (4) the corresponding input capacitances of the multiple input PSF block can be calculated as $C_{i,a_0} = C_{i,b_0} = 5aF$.

The PSF addition scheme, consisting of several parallel multiple input PSF blocks functions correct when using ideal input voltage sources. However, when using the PSF addition scheme in a Single Electron Encoded Logic (SEEL) environment the input is not ideal. The output signal of a SEEL gate is generated by a static inverting buffer, which is depicted in Figure 6. The value logic '1' is represented as a net charge of one electron on node o, which results in an output voltage V_o of approximate $16mV$, assuming $C_l = 10aF$. When connecting a gate to the output of the buffer, it is assumed that its input capacitance C_i is much smaller than the load capacitor of the buffer, that is $C_i \ll C_l$. If that is not the case, the output voltage of the buffer would decrease and it might even cause the buffer to malfunction. This situation occurs when connecting a buffer to one input of the PSF addition scheme, or even to a single PSF block.

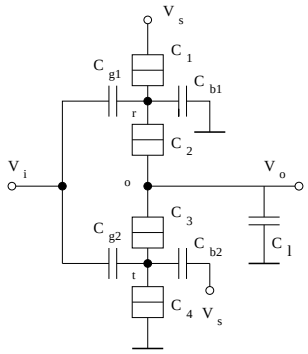


Fig. 6. Static inverting buffer.

The solution to this problem is an integral design of both the output buffers of the SEEL gates and the first stage of the PSF block, the electron trap. For this purpose a mathematical model of the connection between a buffer and an electron trap was derived. The model proved to be non-linear and can only be solved using numerical methods. For a complete description of the model, the reader is referred to [7]. Calculations proved that it is not possible for a buffer to drive multiple electron traps in the same time and have all the latter function correct. Therefore buffers have to be added in front of each input of every PSF block. Moreover, to eliminate feedforward from the gates driving the inputs of the adder a buffer is also

placed on every input of the PSF adder.

5. EXAMPLE

To demonstrate our proposal a buffered 3-bit PSF adder was designed and simulated. The parameter values of the buffers were taken from [8]: $C_1 = C_4 = 0.1aF$, $C_2 = C_3 = 0.5aF$, $C_{b1} = C_{b2} = 4.25aF$, $C_{g1} = C_{g2} = 0.5aF$. For the buffers at the inputs of the adder the standard load capacitance was chosen $C_l = 9aF$. To denote the input capacitor of the PSF block generating output y, connected to input x, the notation $C_{ix,y}$ is used. The load capacitor of the buffer driving that input is denoted as $C_{lx,y}$. The values of these capacitances were calculated by a Matlab program using the mathematical model mentioned before, resulting in $C_{ia0,s0} = 4.96aF$, $C_{la0,s0} = 4aF$, $C_{ia0,s1} = 2.54aF$, $C_{la0,s1} = 6.5aF$, etc. [7]

The simulation results of the buffered 3-bit PSF adder are presented in Figure 7 and indicate that the buffered PSF adder functions correctly. The total area required is 286 circuit elements and the delay is $16.8ns$. In general, the required area for an n-bit buffered PSF adder is $10n^2 + 61n + 13$ circuit elements, thus the area is in the order of $O(n^2)$. However, for small n ($n < 6$) the area cost can be considered as being linear to the number of inputs. The delay is determined by the slowest PSF block, which is the one producing the most significant bit. The delay of the least significant PSF block is approximate $2ns$ but it doubles for every next PSF block, and therefore the overall delay is in the order of $O(n^2)$.

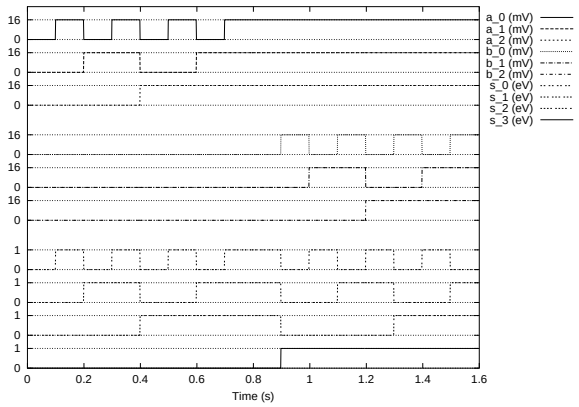


Fig. 7. Simulation results for the 3-bit PSF adder.

6. PRACTICAL CONSIDERATIONS

In theory any arithmetic operation that can be expressed as a periodic symmetric function, could be build using multiple input PSF building block. However, practical considerations limit the number of inputs for the such schemes.

The first problem that arises when designing PSF based circuits with large operands, is the required accuracy. A PSF block with a large weight has a large number of unit steps in a period of its transfer function and thus a small step size. Small unit steps results in small margins for the threshold of the output buffer of the PSF block and therefore a high accuracy is needed. Thus the required accuracy is depending on the number of output bits.

The second problem is the delay of the PSF adder, which is quadratic to the number of output bits. For addition this means that the delay is also quadratic to the number of inputs, since the latter is linear to the number of output bits. But for multi operand addition the relation between the number of inputs and outputs is less than linear, resulting in a delay less than quadratic. For parity check the delay is even independent on the number of inputs ($O(1)$).

To build an adder with large numbers of inputs, based on the PSF addition scheme, a hierarchical approach can be used. In this way the input operands are partitioned in $\frac{k}{2}$-bit blocks, where k is the maximum number of inputs a PSF adder can accommodate. For each block one PSF adder can be used and these PSF adders can be cascaded in a ripple-carry scheme or used in more efficient structures, e.g., carry look-ahead, carry-skip, etc.

7. CONCLUSION

This paper investigated the implementation of Periodic Symmetric Functions (PSF) in single electron tunneling technology. First, a building block was proposed that performs a multiple input PSF. Second, a PSF based addition scheme was proposed and it was shown how this adder can be used in a Single Electron Encoded Logic (SEEL) environment. Finally, a 3-bit instance of the addition scheme was presented and verified by means of simulation.

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