Compact Current and Current Noise Models for Single-Electron Tunneling Transistors

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Abstract — This paper presents an analytic current model for capacitively coupled Single-Electron Tunneling Transistors (SETTs) that is based on a modified M-state steady-state master equation. Based on this current model we also derive a current noise model for SETT. To validate the proposed models we calculate their characteristics at different device parameters and different operation temperatures and compare them with the corresponding characteristics calculated by the full master equation method. The results indicate that the proposed models with M = 3 fit well with the full master equation method at arbitrary device parameters when $T < 0.1e^2/k_BC$ and $V_{DS} < 10e/C$. Due to their simplicity and accuracy in a wide range of working conditions (arbitrary device parameters, $T < 0.1e^2/k_BC$ and V_{DS} <10e/C) the proposed current and noise models can be utilized in large-scale circuit simulation.

Index Terms — Single-electron tunneling, devices, noise, modeling, simulation.

I. INTRODUCTION

The Single-Electron Tunneling Transistor (SETT), first proposed by Likaharev's group [1], is a popular SET device for its small size, low power consumption, and rich functionality [2]. To utilize its inherent features such as Coulomb blockade and Coulomb oscillation in large-scale circuits, an efficient, accurate and analytic model for SETT is highly required. In the early days, some numerical simulators [3-5] and a macro-model [6] have been proposed, but they are either incompatible with conventional circuit simulation or too simple to capture the device inherent behavior. In recent years, some compact analytic models have been also proposed [7-10], however, they are only available in a narrow range of temperature, restricted device parameters, or low drainsource voltage. In this paper, we propose an analytic current model for SETT that is based on a modified Mstate steady-state master equation. The calculated results demonstrate that the proposed models with M = 3 fit well with the full master equation method at arbitrary device parameters and have a quite wide range of temperature (T $<0.1e^{2}/k_{B}C$) and drain-source voltage (V_{DS} <10e/C). Based on the proposed current model, we also derive a current noise model for SETT. The simulations indicate that the current noise model holds the same high accuracy in a wide range of working conditions, which also provides an additional evidence for the validity of the derivation of the proposed compact current model.

II. CURRENT MODEL FOR SETT BASED ON MODIFIED M-STATE MASTER EQUATION



Fig. 1. SETT Schematic

The SETT structure, graphically depicted in Fig. 1, is reminiscent of a usual metallic-oxide-semiconductor fieldeffect-transistor (MOSFET), but with a small conducting island embedded between two tunnel junctions [2], instead of the traditional inversion channel. For the SETT proper operation, both R_D and R_S have to be much larger than R_Q, where R_Q =h/e² $\approx 25.8 \text{ k} \Omega$ is the quantum unit of resistance. Furthermore, we assume that the charge energy is dominant to the thermal fluctuation, that is e²/2C >>k_BT, where $C = C_D + C_S + C_G + C_B$ is the total capacitance between the island and environment.

According to the single-electron orthodox theory, we can easily get the steady master equation for SETT as [11]:

$$\mathbf{\Gamma} \cdot \mathbf{\rho} = 0 \tag{1}$$

If we assume that the SETT has only $M = m_u + m_l + 1$ most possible states, n- m_l, ..., *n*-1, *n*, *n*+1, ..., n+ m_u, we have that Γ is a tri-diagonal $M \times M$ matrix with,

$$\Gamma_{ij} = \begin{cases} \Gamma_{j \to i} & i = j \pm 1 \\ -\Gamma_{i \to i-1} - \Gamma_{i \to i+1} & i = j \\ 0 & others \end{cases}$$
(2)

and $\mathbf{\rho} = (\rho_{n-m_l} \dots \rho_{n-1} \rho_n \rho_{n+1} \dots \rho_{n+m_u})^T$, which can be normalized as:

$$\sum_{i=n-m_l}^{n+m_u} \rho_i = 1 \qquad (3)$$

In the above expressions, $\Gamma_{i \rightarrow j}$ is the electron tunneling rate from state *i* to *j*, and ρ_i is the state probability that there are *i* extra electrons in the island. Additionally,

$$\Gamma_{i \to i+1} = \Gamma_D^+(i) + \Gamma_S^-(i) \tag{4}$$
$$\Gamma_{i \to i-1} = \Gamma_D^-(i) + \Gamma_S^+(i) \tag{5}$$

with

$$\Gamma_{i}^{\pm}(i) = \frac{(\pm V_{i}(i) - e/2C)}{eR_{i}[1 - \exp((\mp V_{i}(i) + e/2C)e/k_{B}T)]} \quad i=D, S \quad (6)$$

with

$$V_{D}(i) = \frac{1}{C} \left[(C - C_{D}) V_{D} - C_{S} V_{S} - C_{G} V_{G} - C_{B} V_{B} - ie - Q_{0} \right]$$
(7)

$$V_{S}(i) = \frac{1}{C} (C_{D}V_{D} - (C - C_{S})V_{S} + C_{G}V_{G} + C_{B}V_{B} + ie + Q_{0})$$
(8)

where Q_0 is the background charge in the island.

At its turn ρ_i can be solved recursively,

$$\rho_{i} = \frac{\Gamma_{i+1 \to i}}{\Gamma_{i \to i+1}} \rho_{i+1} \quad i= n-1, \dots, n-m_{l}$$
(9a)
$$\rho_{i} = \frac{\Gamma_{i-1 \to i}}{\Gamma_{i \to i-1}} \rho_{i-1} \quad i= n+1, \dots, n+m_{u}$$
(9b)

For given V_D , V_S , V_G and V_B values we assume that the most possible M-states are n-m_l, …, *n*-1, *n*, *n*+1, …, n+m_u, where *n* is determined as:

$$n = \left[\frac{1}{2} - \frac{1}{e} (C_D V_D + C_S V_S + C_G V_G + C_B V_B + Q_0) + \frac{C(R_D V_S + R_S V_D)}{e(R_D + R_S)}\right]$$
(10)

where we use the function [x] to represent the maximum integer smaller than or equal to x.

Firstly, we assume that the SETT only works in abovementioned M states. So, the net current through the drain to source in a steady state can be calculated as:

$$I_{DS1} = e\rho_{n+m_u} \Gamma_S^+(n+m_u) - e\rho_{n-m_l} \Gamma_S^-(n-m_l) + \sum_{i=n-m_l+1}^{n+m_u-1} e\rho_i [\Gamma_S^+(i) - \Gamma_S^-(i)]$$
(11a)

or:

$$I_{DS2} = e\rho_{n-m_l}\Gamma_D^+(n-m_l) - e\rho_{n+m_u}\Gamma_D^-(n+m_u) + \sum_{i=n-m_l+1}^{i=n+m_u-1} e\rho_i [\Gamma_D^+(i) - \Gamma_D^-(i)]$$
(11b)

Our calculations indicate that the results calculated by Equation (11a) are almost equal to those calculated by Equation (11b), which is consistent with the physical evidence of the steady current continuity equation. They both fit well with those calculated by the full master equation method in low V_{DS} region and at low temperature *T* when M is small, e.g., M = 3. However both equations produce big deviations in high V_{DS} region and at high *T*, which is consistent with the physical meaning for the states beyond the most possible M-states becoming more and more important with the V_{DS} and *T* increasing.

To compensate for the deviation of the M-state model in high V_{DS} region and at high *T*, we recalculated the steady current by,

$$I_{DS} = \frac{I_{S}R_{S} + I_{D}R_{D}}{R_{S} + R_{D}}$$
(12)

With,

$$I_{S} = \sum_{i=n-m_{l}}^{n+m_{u}} e \rho_{i} \left[\Gamma_{S}^{+}(i) - \Gamma_{S}^{-}(i) \right]$$
(13)

$$I_{D} = \sum_{i=n-m_{l}}^{i=n+m_{u}} e \rho_{i} \Big[\Gamma_{D}^{+}(i) - \Gamma_{D}^{-}(i) \Big]$$
(14)

Equations (12)-(14) constitute the SETT analytic current model we propose.

III. CURRENT NOISE MODEL FOR SETT

Based on the current model in Section II, we recalculated the current noise with the method described in [12], and deduced the final expression for the spectral density of SETT current as follows:

$$S_{II} = \frac{4e^2}{\left(R_D + R_S\right)^2} \cdot \mathbf{A} \cdot \left(-\mathbf{\Gamma}\right)^{-1} \cdot \mathbf{B} + \frac{2e^2}{\left(R_D + R_S\right)^2} \mathbf{D} \cdot \boldsymbol{\rho} \quad (15)$$

where, **A** is a $1 \times M$ matrix, $(-\Gamma)^{-1}$ is a $M \times M$ matrix, **B** is a $M \times 1$ matrix, **D** is a $1 \times M$ matrix. And,

$$\mathbf{A}_{1i} = \left[\Gamma_D^+(n - m_1 + i - 1) - \Gamma_D^-(n - m_1 + i - 1) - I_D / e\right] R_D + \left[\Gamma_S^+(n - m_1 + i - 1) - \Gamma_S^-(n - m_1 + i - 1) - I_S / e\right] R_S \quad (16)$$

$$\mathbf{B}_{l1} = \left[\Gamma_{D}^{+}(n-m_{l}+i-2)R_{D} - \Gamma_{S}^{-}(n-m_{l}+i-2)R_{S} \right] \rho(n-m_{l}+i-2) \\ + \left[\Gamma_{S}^{+}(n-m_{l}+i)R_{S} - \Gamma_{D}^{-}(n-m_{l}+i)R_{D} \right] \rho(n-m_{l}+i) \\ - \left(R_{D} + R_{S} \right) I_{DS1} / e \cdot \rho(n-m_{l}+i-1)$$
(17)

with,

$$\rho(n-m_l-1)=0\tag{18a}$$

$$\rho(n+m_u+1) = 0 \tag{18b}$$

$$\mathbf{D}_{1i} = R_s^{2} \left[\Gamma_s^+ (n - m_l + i - 1) + \Gamma_s^- (n - m_l + i - 1) \right] + R_D^{2} \left[\Gamma_D^+ (n - m_l + i - 1) + \Gamma_D^- (n - m_l + i - 1) \right]$$
(19)

We note here that apart of the current noise model, that is the commonest noise model in MOSFET technology, two other noises, the voltage noise and the voltage-current mutual noise, might be of interest too. For the time being our approach has not been extended to model those two noises as well and this is meant for future work.

IV. RESULTS AND COMPARISONS

To demonstrate the validity of our proposed models, we instantiate and calculate three cases of I_{DS} - V_{GS} , I_{DS} - V_{DS} , S_{II} - V_{DS} characteristics by using the proposed current and current noise models with M = 3 ($m_u = m_l = 1$) at different device parameters ($C_D = C_S$, $R_D = R_S$, $C_D = 10C_S$, $R_D = 15R_S$, and $C_D = C_S$, $R_D = 0.1R_S$). We compared the calculated results with the corresponding characteristics calculated by the full master equation method. If we assume $C_B = 0$, $V_B = 0$, $Q_0 = 0$, $C_G = 10C_S$, $V_{DS} = 0.4$ (e/C) for I_{DS} - V_{GS} curves and $V_{GS} = 0$ for I_{DS} - V_{DS} curves, the calculated results at

different temperature (T = 0, $0.02e^2/k_BC$, $0.1e^2/k_BC$) are depicted in Fig. 2,3,4, respectively.

Our calculations indicate that, when $T = 0.1e^2/k_BC$ and $V_{DS} < 10e/C$, the error compared with the full master equation method is: within 1.4% for I_{DS} and 1.5% for S_{II} for the case of $C_D = C_S$ and $R_D = R_S$; within 0.7% for I_{DS} and 8% for S_{II} for the case of $C_D = 10C_S$ and $R_D = 15R_S$; and within 0.7% for I_{DS} and 8% for S_{II} for the case of $C_D = C_S$ and $R_D = 0.1 R_S$. Therefore, we can conclude that the proposed current and current noise models with M = 3 fit well with the full master equation method at arbitrary device parameters when $T < 0.1e^2/k_BC$ and $V_{DS} < 10e/C$.



Fig. 2. Calculated SETT I_{DS} - V_{GS} , I_{DS} - V_{DS} , S_{II} - V_{DS} characteristics at different operation temperature (T = 0, $0.02e^2/k_BC$, $0.1e^2/k_BC$ from bottom to top, and vertical offset is 0.1 normalized unit for I_{DS} - V_{GS} curves and 2 normalized unit for I_{DS} - V_{DS} , S_{II} - V_{DS} curves) for the case of $C_D = C_S$, $R_D = R_S$. Dot is used for the proposed analytic models and solid line for the full master equation method.



Fig. 3. Calculated SETT I_{DS} - V_{GS} , I_{DS} - V_{DS} , S_{II} - V_{DS} characteristics for the case of $C_D = 10C_S$, $R_D = 15R_S$, and the curves are arranged similar to Fig.2.



Fig.4. Calculated SETT I_{DS} -V_{GS}, I_{DS} -V_{DS}, S_{II} -V_{DS} characteristics for the case of C_D = C_S , R_D =0.1 R_S , and the curves are arranged similar to Fig.2.

V. CONCLUSION

First we proposed an analytic current model for capacitively coupled SETT. It is based on a modified Mstate steady-state master equation. Subsequently, we developed a current noise model for SETT based on the proposed current model. We calculated the characteristics of the proposed models for different device parameters and at different operation temperature and compared them with the corresponding characteristics calculated by the full master equation model. Our results demonstrate that when assuming M = 3 the proposed models fit well with the full master equation method at arbitrary device parameters when T $<0.1e^2/k_BC$ and $V_{DS} <10e/C$. The proposed compact current and noise models are promising with respect to their application in large-scale circuit simulation for their simplicity and accuracy in a wide range of working conditions (arbitrary device parameters, $T < 0.1e^2/k_BC$ and $V_{DS} < 10e/C$). Moreover, the developed current noise model is the most compact SETT noise model so far (when compared with [11,12]).

REFERENCES

- D.V. Averin and K. K. Likharev, "Coulomb blockade of Single-electron Tunneling, and coherent oscillations in small tunnel junction," *Journal of low temperature physics*, vol. 62, no. 3/4, pp. 345-373, 1986.
- [2] K.K. Likharev, "Single-electron devices and their applications," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 606-632, April 1999.
- [3] R.H. Chen, A. N. Korotkov, and K. K. Likharev, "Singleelectron Transistor logic," *J. Appl. Phys.*, vol.68, pp. 1954-1956, April 1996.
- [4] C. Wasshuber, H. Kosina, and S. Selberherr, "SIMON a simulator for single-electron tunnel devices and circuits," *IEEE Transactions on Computer-Aided Design*, vol. 16, no. 9, pp. 937-944, September 1997.
- [5] L. R. C. Fonseca, A. N. Korotkov, K. K. Likharev, and A. A. Odintsov, "A numerical study of the dynamics and statistics of single electron systems," *J. Appl. Phys.*, vol. 78, no. 5, pp. 3238–3251, Sept. 1995.
- [6] Y. S. Yu, W. Hwang, and D. D. Ahn, "Macromodeling of single-electron transistor for efficient circuit simulation," *IEEE Transactions on Electron Devices*, vol. 46, pp. 1667-1671, August 1996.
- [7] K. Uchida, K. Matsuzawa, J. Koga, R. Ohba, S. Takagi, and A. Toriumi, "Analytical Single-Eelectron Transistor (SET) model for design and analysis of realistic SET circuits," *Jpn. J. Appl. Phys.*, vol. 39, pp. 2321–2324, April 2000.
- [8] X. Wang and W. Porod, "Single-electron transistor analytic I-V model for SPICE simulations," *Superlatt. Microstruct.*, vol. 28, pp. 345–349,2000.
- [9] H. Inokawa and Y. Takahashi, "A Compact Analytical Model for Asymmetric Single-Electron Tunneling Transistors," *IEEE Trans. Electron Devices*, vol. 50, no. 2, pp. 455- 461, 2003.
- [10] S. Mahapatra, A. M. Ionescu and K. Banerjee, "A Quasi-Analytical SET Model for Few Electron Circuit Simulation," *IEEE Electron Device Letters*, vol. 23, no. 6, pp. 366-368, June 2002
- [11] S. Hershfield, J. H. Davies, P. Hyldgaard, C. J. Stanton, and J. W. Wilkins, "Zero-frequency current noise for the double-tunnel-junction Coulomb blockade," *Physical Review B*, vol. 47, no. 4, pp. 1967-1979, January 1993.
- [12] A. N. Korotkov, "Intrinsic noise of the single-electron transistor," *Physical Review B*, vol. 49(15), pp. 10381-10392, 1994.