SPICE Implementation of a Compact Single Electron Tunneling Transistor Model

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***Abstract* — A novel compact Single Electron Tunneling Transistor (SETT) SPICE model is described in this paper. This SPICE implementation is based on an analytical model derived from a simplified full master equation model. Besides of being able to accurately capture the SETT behavior under various circuit and temperature conditions our proposal can also evaluate background charge effects in SETT circuits. This is achieved by associating random seeds that model the random background charge noise effect to each SETT in the circuit. To validate our proposal we simulated with the proposed model, as well as with other more computationally demanding models, an inverter, a ring oscillator, and a hybrid SETT/MOSFET circuit. The simulation results clearly indicate that our model provides the same accuracy as other state-of-the-art SETT SPICE models. However due to the simplicity of the compact current model we use our proposal can save on simulation time and this makes it potentially applicable for large-scale circuit simulation.**

***Index Terms* — Single electron tunneling transistor, SPICE, simulation.**

I. Introduction

When scaling trend continues in the field of electronics, fabrication technology developments make novel device possible. Single electron tunneling transistor (SETT), which works by tunneling and Coulomb blockade, provides great advantages in power dissipation and device density and thus it is of potential interest for future integrated circuits [1-3].

To simulate large-scale integrated SETT circuits and/or hybrid SETT/MOS circuits, several SPICE models for SETT have reported [4-9]. However, they are either only available in a narrow range of temperature, restricted device parameters, or low drain-source voltage [4-7], or spend too much time in simulation [8], or too simple to capture the device inherent behavior [9]. This paper describes a SETT SPICE model based on a recently proposed model, which was validated for a wide range of working conditions (arbitrary device parameters, T $<0.1e^2/k_BC$ and V_{DS} $<10e/C$) [10]. Due to the efficiency and simplicity of the compact current model we implemented, our proposal reduces the simulation time substantially and consequently can be potentially utilized for large-scale circuit simulation. Furthermore, not like some other SETT SPICE models based on MOS sub-models, sub-circuits, or macro-models, our work introduces a new, level-independent SETT model in the SPICE program. Additionally, the SPICE model we developed embeds a mechanism that supports the evaluation of background charge noise, modeled as random island charge that can be set for each SETT in the circuit, effects in simulations.

The remainder of this paper is organized as follows: The SPICE implementation of the compact SETT model is described in Section II. Section III provides simulation results for several circuits. The random background charge noise setting is explained in Section IV and Section V concludes the paper.

II. SETT Model Implementation in SPICE

According to [10], a compact M-state (M=2L+1) current model for SETT is described by

$$I_{DS}=\frac{e\sum_{i=n-L}^{n+L}\left(R_S\rho_i\left[\Gamma_S^+(i)-\Gamma_S^-(i)\right]+R_D\rho_i\left[\Gamma_D^+(i)-\Gamma_D^-(i)\right]\right)}{R_S+R_D} \quad (1)$$

where the ρ_n is the state probability that there are n extra electrons in the island, Γ is the electron tunneling rate. D and S point out the terminal and positive and negative signs indicate electron tunnel direction. The most possible M states are assumed to be n-L, …, n-1, n, n+1, …, n+L, where n is determined by

$$n=\left[\frac{1}{2}-\frac{1}{e}\left(C_DV_D+C_SV_S+C_GV_G+C_BV_B+Q_0\right)+\frac{C\left(R_DV_S+R_SV_D\right)}{e\left(R_D+R_S\right)}\right] \quad (2)$$

where R_D and R_S are drain and source tunnel resistances respectively. C_D, C_S, C_G, and C_B are capacitances of drain, source, gate, and back gate, C is the sum of all the four capacitances, and Q_0 is the background charge in the island.

TABLE I
SETT MODEL PARAMETER SET

Name	Description	Default Value	Name	Description	Default Value
cdrain	Drain capacitance	1aF	rsource	Source tunnel resistance	100kohm
csource	Source capacitance	1aF	temp	Operation temperature	4.2K
cgate	Gate capacitance	1aF	Sorder	Used to determine number of states to be calculated	1
cbgate	Back gate capacitance	1aF	BCC	Background charge center	0
rdrain	Drain tunnel resistance	100kohm	BCR	Background charge range	0

Equations (1), (2) are validated for a wide range of working conditions (arbitrary device parameters, T <0.1e^2/k_BC and V_{DS} <10e/C) in [10] and the SETT model we implemented in SPICE is based on this compact model.

The parameter set of our SPICE model is presented in Table 1. Sorder is used to determinate the number of the to be calculated states (the actual number of states to be calculated is 2*Sorder + 1), that is, default Sorder =1 means that three-state will be calculated in the SPICE simulation. Parameters BCC and BCR are used to randomize the background charge noise for each SETT in the modeled circuit, where BCC is used to determine the average value of the background charge for a SETT, while BCR gives the range of the charge noise swing (the possible maximum of BCR is *e*). Thus for a certain SETT the random background charge obeys evenly random distribution in the interval [BCC-BCR/2, BCC+BCR/2].

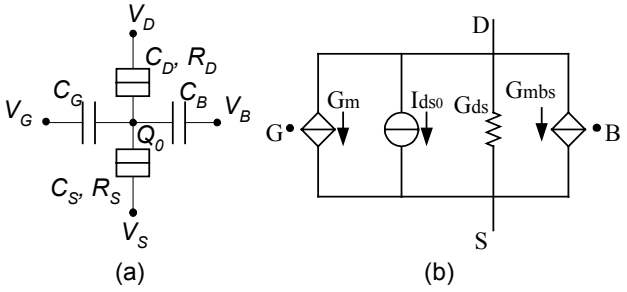

Fig. 1. (a) SETT Schematic (b) SETT SPICE equivalent circuit

In SPICE simulation, the SETT is taken as a four-terminal device. Its schematic and SPICE equivalent circuit are depicted in Fig. 1. G_m, G_{ds}, and G_{mbs} can be calculated from the derivatives of drain current in Equation (1). For example, G_m can be expressed as:

$$G_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{e}{R_S + R_D} \sum_{i=n-Sorder}^{n+Sorder} R_S \left[\frac{\partial \rho_i}{\partial V_{GS}} \left[\Gamma_S^+(i) - \Gamma_S^-(i) \right] + \rho_i \left[\frac{\partial \Gamma_S^+(i)}{\partial V_{GS}} - \frac{\partial \Gamma_S^-(i)}{\partial V_{GS}} \right] \right] + \frac{e}{R_S + R_D} \sum_{i=n-Sorder}^{n+Sorder} R_D \left[\frac{\partial \rho_i}{\partial V_{GS}} \left[\Gamma_D^+(i) - \Gamma_D^-(i) \right] + \rho_i \left[\frac{\partial \Gamma_D^+(i)}{\partial V_{GS}} - \frac{\partial \Gamma_D^-(i)}{\partial V_{GS}} \right] \right] \quad (3)$$

where ρ_i, $\Gamma_D^{\pm}(i)$, and $\Gamma_S^{\pm}(i)$ can be obtained from the expressions presented in [10].

With G_m, G_{ds}, G_{mbs} and I_{DS} calculated, the equivalent circuit for any SETT can be built, in which the value of current source I_{ds0} is determined by:

$$I_{ds0} = I_{DS} - G_m V_{GS} - G_{ds} V_{DS} - G_{mbs} V_{BS} \quad (4)$$

Fig. 2 depicts the characteristics of a SETT with three-state simulation (Sorder = 1).

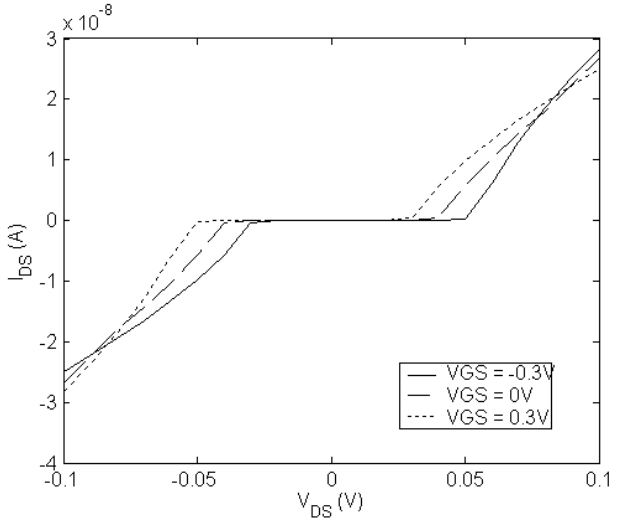

Fig. 2. I_{DS} - V_{DS} curves of three-state simulation of SETT with different V_{GS}. Parameters are set as follows: cdrain = csource = cgate = 1aF, cbgate = 0, rdrain = rsource = 1Mohm, temp = 4.2K, and background charge is set to 0.

III. CIRCUIT SIMULATION

To validate our proposal we simulated with the proposed model an inverter, a ring oscillator, and a hybrid

SETT/MOSFET circuit. In all the simulations we assumed that Sorder=1 for all the SETTs in the considered circuits. Fig. 3-5 present the simulation results corresponding to the considered circuits. To verify the accuracy of our model, we compared our simulations with the 11-state SPICE SETT model based on sub-circuit approach described in [8].

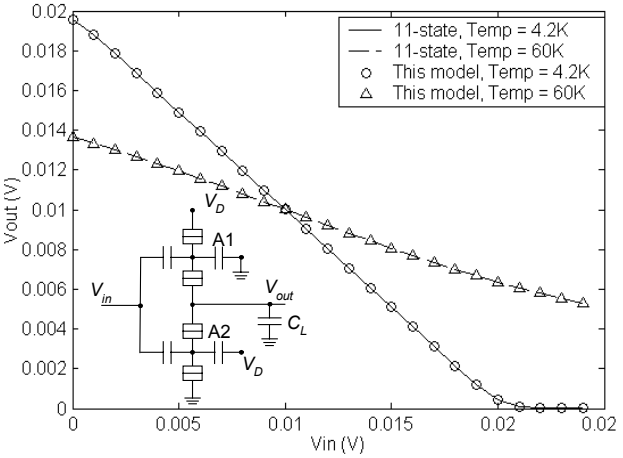

Fig. 3. Simulated inverter characteristics, compared with 11-state calculation by the approach [8].

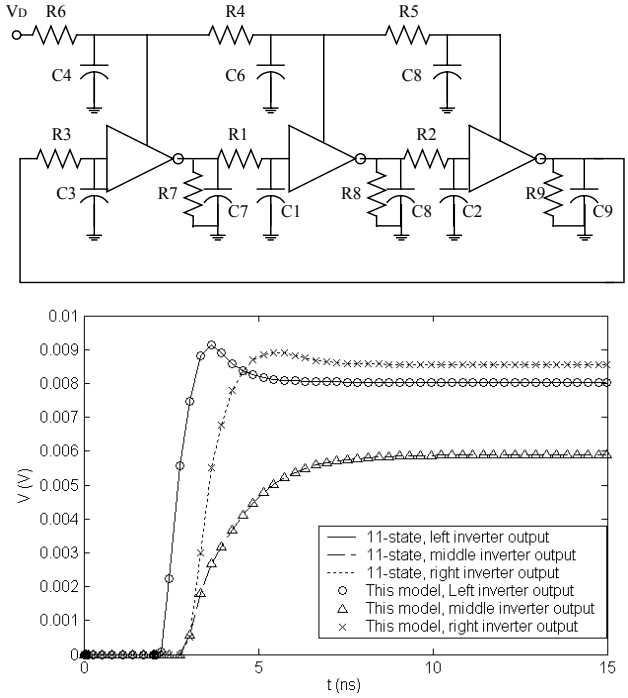

Fig.4. Ring oscillator and its response to pulse input, compared with 11-state calculation by the approach [8].

The parameters of the SETTs in Fig. 3 are as follows: rdrain = rsource = 10Mohm, cdrain = csource = cgate = 1aF, and cbgate = 0. The background charge of A1 and A2 are BCC=0.15, BCR=0 and BCC=-0.15e, BCR=0, respectively. Moreover, the load capacitance C_L is needed to be large enough to make the SPICE SETT model valid and we have choose C_L =0.1fF.

For the ring oscillator in Fig.4, all SETTs have the same drain and source resistance value of 200Kohm. Capacitances of drain, source and gate are 1aF. The grounded SETTs in the three inverters have background charge with BCC=0.15e and BCR=0, while devices connected to power supply have BCC=-0.15e and BCR=0. R1 = R2 = R3 = 20Mohm, R4 = R5 = R6 = 2000ohm, R7 = R8 = R9 = 500Tohm, C1 = C2 = C3 = 0.05fF, C4 = C5 = C6 = 0.1pF, C7 = C8 =C9 = 0.1fF. Operation temperature is 0.01K. The input signal is a pulse supply rise from 0 to 0.035V in the first 2ns.

As depicted in Fig.5, the input of the hybrid circuit is connected to gate of the SETT, which drives the load transistor MN1. Output signal is then fed into the gate of MN2 to get a potential shift of about 0.4V. The parameters of the SETT are the same as those in Fig. 3. RL = 10Kohm, threshold voltages of MN1 and MN2 are –1 and –0.5V, respectively. KP of MN1 and MN2 are 0.1 and 0.01μs/V. Operation temperature is 4.2K. Background charge noise is set to zero.

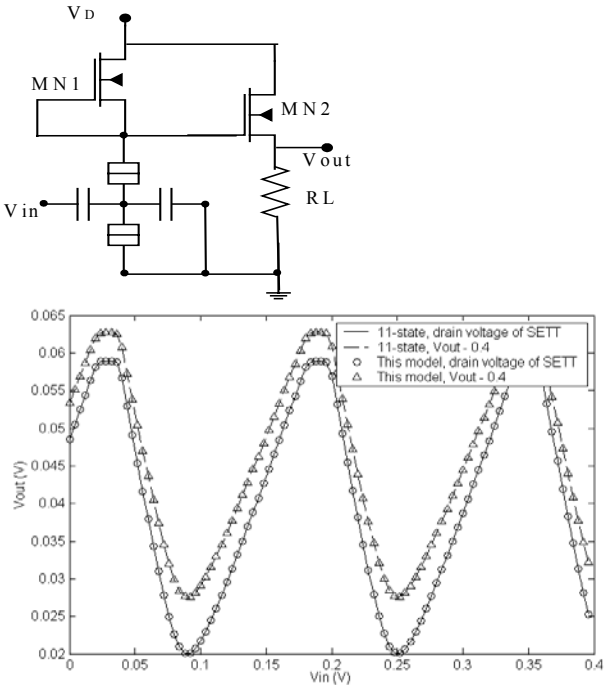

Fig. 5. Schematic and output characteristic of hybrid circuit of SETT and MOSFET, compared with 11-state calculation by the approach [8].

Our experiments clearly indicate that for all the considered circuits, the results produced by our model match perfectly well the results produced by the 11-state model. However due to the much smaller number of states we consider we expect a substantial improvement in simulation speed. A detailed analysis of execution time is left as future work.

IV. Random Background Charge Noise Setting

Generally, the background charge for SETTs cannot be determined accurately. SETTs fabricated with the same process will have different background charge noise. Moreover, the characteristics of SETTs are sensitive to the distortion. In this sense, making background charge randomized is a realistic assumption for simulation purposes.

In our approach, the distribution of background charge is assumed to be uniformly random distribution. When a SETT is loaded into the circuit matrix for the first time, the random background charge is calculated and stored. That is, the background charge is randomized only once for each SETT under simulation.

Fig. 6 gives the simulation results corresponding to an inverter with random background charge. The parameters of A1 and A2 are the same as those in Fig. 3 but BCR is set to 0.2 e.

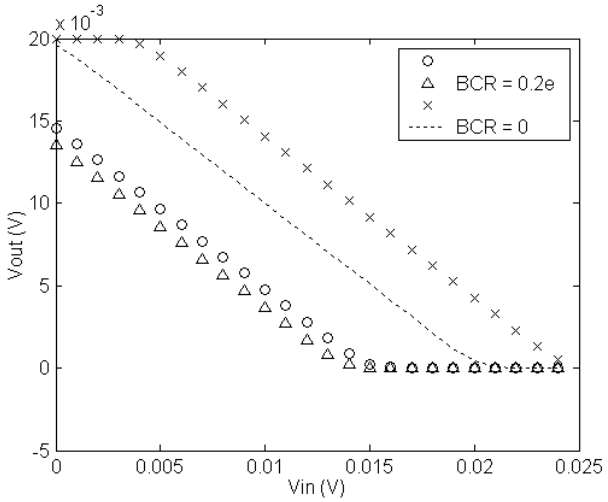

Fig. 6. Simulation results of inverter with random background charge

V. Conclusion

A novel compact SETT SPICE model based on an analytical model deduced from a simplified full master equation model was described. Besides of being able to accurately capture the SETT behavior under various circuit and temperature conditions our proposal can also evaluate background charge effects in SETT circuits. This feature creates the possibility to investigate and explore the sensitivity of circuit performance to background charge noise present in different circuit islands. We validated our proposal by simulating an inverter, a ring oscillator, and a hybrid SETT/MOSFET circuit. The simulation results clearly indicated that our model provides the same accuracy as other state-of-the-art SETT SPICE models. However due to the simplicity of the compact current model we use our proposal leads to reduced simulation time and this makes it applicable for large-scale circuit simulation.

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