Influence of Bit Line Twisting on the Faulty Behavior of DRAMs

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Abstract: *Bit line twisting is an effective design method commonly used to reduce the impact of bit line coupling noise in high density memory devices. This paper investigates the way bit line twisting influences the faulty behavior of DRAMs, based on an analytical evaluation of coupling effects on the one hand, and a simulation-based fault analysis using a Spice simulation model on the other. Two different DRAM twisting schemes, in addition to a third untwisted bit line scheme, are presented and analyzed. Both the analytical and the simulation-based evaluation results show that each scheme has its own specific impact on the faulty behavior. The same approach presented in the paper can be used to analyze the impact of other bit line twisting schemes on the memory faulty behavior.*

Keywords: *Bit line twisting, bit line coupling, crosstalk noise, DRAMs, defect simulation, faulty behavior.*

1 Introduction

As the integration density of DRAM devices increases, the problems associated with crosstalk noise become ever more significant, particularly for bit lines (BLs) because of the weak cell signals that must be sensed reliably [Redeker02]. In order to reduce the impact of crosstalk on BL functionality, some kind of BL twisting technique is sometimes implemented so that noise cancellation can take place [Aoki88].

Previous research on crosstalk reduction on BLs in memory devices investigates the effectiveness of BL twisting techniques in eliminating BL noise in current and future fabrication technologies [Redeker02]. In addition, there is some published qualitative analysis of the possible impact of BL twisting on the faulty behavior of memories [Schanstra03]. However, there is no published quantitative evaluation, supported by simulation, of the impact of noise reduction and BL twisting on memory faults, and on the way neighboring cells influence the faulty behavior for a specific victim cell.

This paper investigates the influence of BL twisting on the faulty behavior of DRAMs. After a quantitative evaluation of BL coupling is presented, the paper discusses the impact of twisting both theoretically and using an electrical simulation model to evaluate the behavior. A number of BL twisting techniques are evaluated and the way a neighborhood of cells influences the behavior is shown.

Section 2 begins with a description of the used Spice simulation model. Section 3 gives a qualitative evaluation of BL coupling on the faulty behavior of an untwisted BL scheme, followed by an evaluation of the impact of twisted BL schemes in Section 4. Section 5 presents the results of a simulation-based fault analysis study of the different BL organizations. Section 6 ends with the conclusions.

2 Spice simulation model

The simulation model used in this paper is based on a design-validation model of an actual DRAM produced by Infineon Technologies. Since the time needed for simulating a complete memory model is excessively long, the simulation model used in our analysis is simplified to keep simulation time in check.

Figure 1 shows a block diagram of the folded BL pair to be simulated. This simplified simulation model contains a 2×2 cell array with nMOS access transistors, in addition to a sense amplifier and precharge devices. The removed memory cells are compensated for by load cells and parasitic components of different values distributed along the BLs. External to the BL pair, the simulation model contains one data output buffer needed to examine data on the output, and a write driver needed to perform write operations. The memory model employs Spice BSIM3v3 device parameters for the simulations.

The model contains three BL pairs, denoted as BLt for

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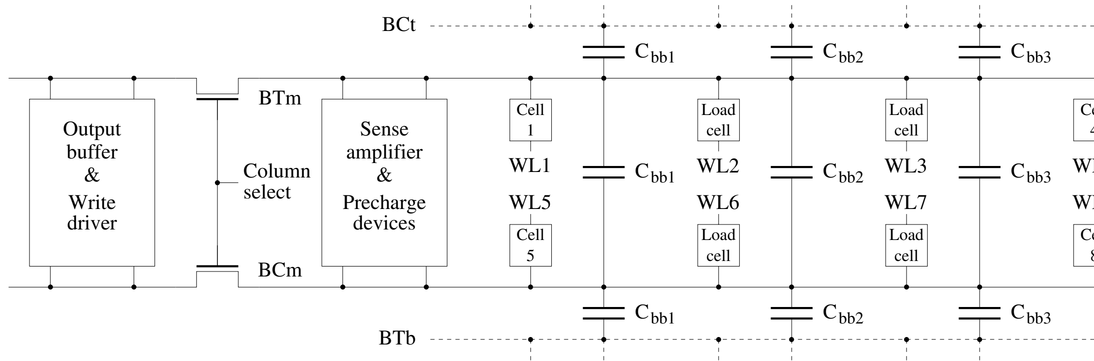

Figure 1. Block diagram of the BL pair used for simulation.

top, BLm for middle, and BLb for bottom, as shown in Figure 2. Figure 1 shows both the true (BTm) and complementary (BCm) bit lines of BLm, only the complementary (BCt) bit line of BLt, and only the true (BTb) bit line of BLb.

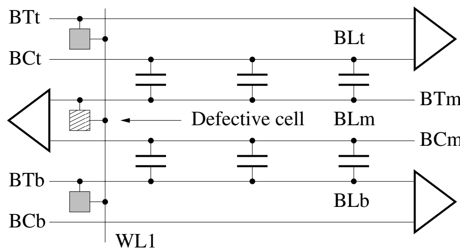

Figure 2. Three BL pairs implemented in the simulation model.

The different BLs influence each other by a number of distributed coupling capacitances ($C_{bb1} + C_{bb2} + C_{bb3} = C_{bb}$). Note that BL coupling capacitances are the same whether coupling takes place within a given BL pair or between different BL pairs. This is true since all BLs on a chip are manufactured in the same way, using the same materials, having the same dimensions, and at the same distances from each other. Identifying a given BL as BT or BC depends solely on the way that BL is connected to the sense amplifier and not on the way it is manufactured.

The total BL capacitance (C_b) is made up of the sum of the BL coupling capacitance (C_{bb}), and the remaining capacitance (C_{br}) not related to BL coupling, but to word line (WL) coupling, substrate coupling, etc. In the simulation model of Figure 1, these capacitances are related as follows:

$$C_b = C_{bb} + C_{br} = 10 \times C_{bb} \tag{1}$$

As a result of (C_{bb}), two different kinds of coupling effects may take place: *pre-sense coupling* and *post-sense coupling* [Aoki88].

Pre-sense coupling (ΔV_1) is generated after the WL is activated and cells are accessed, but before the sense amplifier is activated. The noise on a given floating BL results from coupling to two BLs, above and below the victim BL. The amount of coupling noise depends on the background data stored in accessed neighboring cells. The worst-case background in this situation is when both accessed neighboring cells contain the same data (either both 1 or both 0)[1]. The amount of worst-case ΔV_1 developing on the floating victim BL relative to the full voltage V_1 developing on neighboring BLs can be approximated as [Hidaka89]:

$$\frac{\Delta V_1}{V_1} \approx \frac{1}{2 + (C_{br}/C_{bb})} \tag{2}$$

This relation indicates that the amount of pre-sense coupling noise increases with increasing C_{bb} from 0 V for $C_{bb} = 0$ to $\frac{1}{2}$ as C_{bb} approaches ∞. For the used simulation parameters in Equation 1, the worst-case $\frac{\Delta V_1}{V_1} \approx \frac{1}{11}$.

Post-sense coupling (ΔV_2) is generated after the sense amplifier is activated and BLs are pulled either to 0 or 1 according to the logic value sensed by the sense amplifier. The main reason for this type of noise is the time difference between sense amplifier activation and the instant the sense amplifier decides to sense a 1 or 0 (Δt). The amount of ΔV_2 can be approximated according to the following relation [Aoki88]:

$$\Delta V_2 \approx \alpha \frac{C_{bb}}{C_b^2} (\Delta t)^3 \tag{3}$$

where α is a constant that generally refers to the operation speed of the sense amplifier. The relation shows the strong dependence of ΔV_2 on the time delay until the sense amplifier pulls the BLs either up or down. This means that even small delays in the sense amplifier operation can cause a relatively large amount of coupling noise.

[1] This worst-case background induces the largest amount of BL coupling noise, but it is not the worst-case background for the faulty behavior of a victim cell, as discussed later in Section 3

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The total amount of BL coupling noise ΔV is equal to the sum of pre-sense and post-sense coupling ($\Delta V_1 + \Delta V_2$). Whether ΔV_1 or ΔV_2 constitutes the dominant factor in ΔV depends on design specific parameters that generally cannot be analytically evaluated, which leaves circuit simulation as the only analysis option [Itoh01].

3 Effects of coupling

BL coupling causes small coupling voltages on adjacent BLs, which influences proper sense amplifier operation. From a testing point of view, it is important to understand how a specific initialization of a neighborhood of cells affects the sensing of a given victim, so that the worst-case values can be written in the neighboring cells.

The model considered here [see Figure 2] consists of 3 BL pairs, each with 2×2 cells, resulting in a total number of $3\times2\times2 = 12$ cells in the simulation model. However, only those cells accessed simultaneously by sharing a given WL can influence each other through BL coupling. This means that the neighborhood of aggressors consists of only two cells, each containing either 0 or 1, which results in $2^2 = 4$ different data backgrounds (BGs).

The effects of BL coupling on the faulty behavior can be divided into pre-sensing effects, and post-sensing effects. Figure 3 gives graphical representations for both cases, when Cell 1 on BTt contains a logic 1 and Cell 1 on BTb contains a logic 1 as well.

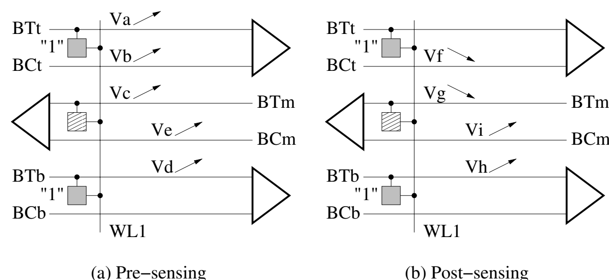

Figure 3. Effects of (a) pre-sense and (b) post-sense coupling.

Pre-sensing effects. As soon as WL1 is accessed, Cell 1 on BTt starts to pull the voltage on BTt by an amount of V_a to a higher level; this is indicated by the up-arrow next to V_a in the figure. As a result of C_{bb}, the voltage on BCt is also pulled by an amount of V_b to higher level as indicated. Finally, as a result of C_{bb} between BCt and BTm, the voltage on BTm is pulled higher by an amount of V_c, which promotes sensing a *logic 1* in the victim[2]. From Equations 1 and 2, the amount V_c is related to V_a by the relation $\frac{V_c}{V_a} = \frac{V_b}{V_a}\frac{V_c}{V_b} \approx \frac{1}{11^2}$. In the same way, as soon as WL1 is accessed, Cell 1 on BTb starts to pull the voltage on BTb by an amount of V_d to a higher level, which in turn pulls the voltage on BCm by an amount of V_e higher. This increase in the voltage on BCm promotes sensing a *logic 0* in the victim cell. The values of V_d and V_e are related by $\frac{V_e}{V_d} \approx \frac{1}{11}$, which means that the cell on BTb has a much higher influence on the faulty behavior than the cell on BTt. In conclusion:

1. The worst-case pre-sensing BG is $\bar{x}_{a_t} x_v x_{a_b}$ (i.e., Cell 1 on BTt contains $\bar{x}$ and Cell 1 on BTb contains x).
2. Cell 1 on BTb has a much higher pre-sensing influence (first-order effect) on the faulty behavior than Cell 1 on BTt (second-order effect).

[2]The increase in the voltage on BTm further results in an increase in the voltage on BCm, but this effect is an order of magnitude less and is therefore negligible

Post-sensing effects. Once the sense amplifier is activated, and since Cell 1 on BTt contains 1, the sense amplifier pulls the voltage on BTt high while the voltage on BCt is pulled low by an amount of V_f [see Figure 3(b)]. As a result of C_{bb}, the voltage on BTm is pulled low by an amount of V_g, which promotes sensing a logic 0 in the victim cell. In a similar way, once the sense amplifier is activated, and since Cell 1 on BTb contains a 1, the sense amplifier pulls the voltage on BTb high by an amount of V_h as indicated in Figure 3. As a result of C_{bb}, the voltage on BCm is also pulled high by an amount of V_i, which promotes sensing a logic 0 in the victim cell. Both neighboring cells have a first-order effect on the victim. In conclusion:

1. The worst-case post-sensing BG is $x_{a_t} x_v x_{a_b}$ (i.e., Cell 1 on BTt contains x and Cell 1 on BTb contains x).
2. Both cells have a comparable first-order effect on the faulty behavior.

Comparing the two results of pre and post-sensing, we find that each requires a different BG to ensure the worst-case sensing condition. It is possible to use a memory test that covers both BGs to ensure covering the worst-case condition. But to reduce test time, a single worst-case BG is needed, and therefore we should identify whether pre-sensing or post-sensing is more dominant.

4 Impact of twisting

BL twisting is used to reduce the influence of BL coupling on the behavior of the memory, by shielding parts of a BL from neighboring BLs. There are many types of BL twisting schemes used in the industry. Figure 4 compares the untwisted BL scheme with other important

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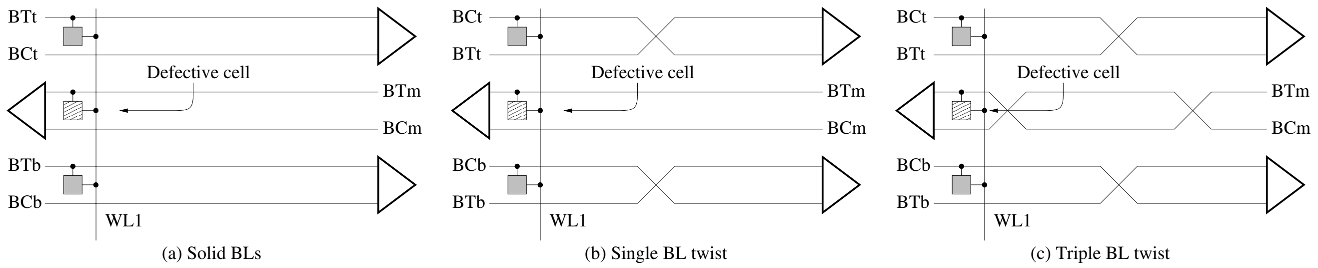

Figure 4. Analyzed BL organizations: (a) solid BLs, (b) single BL twist, (c) triple BL twist, and (d) complex BL twist.

twisted BL organizations: a. the solid BLs (no twist), b. the single BL twist, and c. the triple BL twist [Aoki88]. These BL organizations are known to be effective at reducing crosstalk between adjacent BLs and they have all been used in commercially produced memory components [Redeker02]. Note how BL twisting modifies the type of BLs simultaneously accessed, making cells on both BT and BC to be accessed at the same time with a given WL rather than cells connected only to BT or BC. In Section 3, we analyzed the impact of solid BLs on the behavior, and in this section, we discuss the impact of single and triple twisting on the behavior.

Single twist

Close consideration of the impact of the single twist on memory behavior shows that the single twist fails in completely eliminating pre-sense BL coupling but succeeds in eliminating post-sense coupling. The net effect is that the single twist results in making pre-sense coupling more significant than post-sense coupling on the faulty behavior of the memory. In the following, a more detailed discussion of this point is given.

For pre-sense coupling, Figure 5 shows the pre-sense voltage development on BTm and BCm as a result of a logic 1 stored in both neighboring cells. Since the accessed cell on BCt has a logic 1, a small upward voltage differential of V_a develops on BCt during pre-sensing, which in turn results in pulling BTm up by V_b. As a result of BL twisting, the amount of V_b developing on BTm is almost one half of that in the case of solid BLs[3]. The same situation takes place with BCb, where an up voltage differential of V_c induces an up voltage differential of V_d on BCm. In conclusion, the single twist cuts the amount of pre-sense BL coupling by almost one half, where the remaining coupling effect requires a worst-case BG of $\bar{x}_{a_t} x_v x_{a_b}$ (i.e., Cell 1 on BCt contains $\bar{x}$ and Cell 1 on BCb contains x).

[3] It is actually slightly higher than one half as a result of second-order coupling which is not considered in this discussion

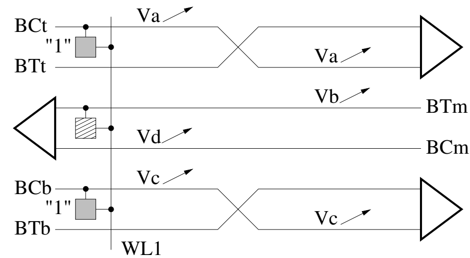

Figure 5. Pre-sense voltage development for a single twist.

For post-sense coupling, Figure 6 shows the voltage development on BTm and BCm as a result of a logic 1 stored in both neighboring cells. During post-sensing, and since the accessed cell on BCt has a logic 1, the top sense amplifier pulls the voltage on BCt up by an amount of V_{a1}, which induces an up differential voltage of V_{a2} on BTm. At the same time, the top sense amplifier pulls the voltage on BTt down by an amount of V_{b1} resulting in a down voltage of V_{b2} on BTm. Since V_{a2} and V_{b2} are equal and opposite to each other, they nullify each other leaving a zero net coupling voltage on BTm. The same situation takes place with the bottom sense amplifier, which pulls BCb down by V_{c1} inducing V_{c2} on BCm, and pulls BTb up by V_{d1} inducing V_{d2} on BCm. V_{c2} and V_{d2} nullify each other leaving a zero net coupling voltage on BCm. In conclusion, the single BL twist totally eliminates post-sense coupling effects.

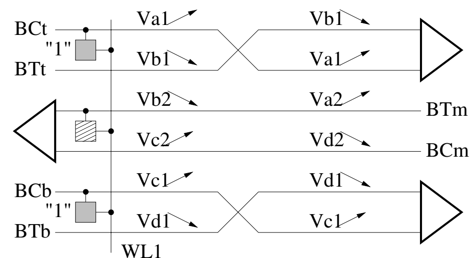

Figure 6. Post-sense voltage development for a single twist.

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Triple twist

Close consideration of the impact of the triple twist on the memory behavior reveals that the triple twist succeeds in completely eliminating the influence of BL coupling, both pre-sense and post-sense coupling. This means that one cannot evaluate the impact of the triple twist on the faulty behavior of the memory by theoretically analyzing the effect of BL coupling, and therefore electrical simulation here becomes necessary to evaluate the faulty behavior.

This can be understood by noticing that the triple twist splits the BL into four equal parts, such that one half of any coupling effect is induced onto BTm while the other half is induced onto BCm. Since only a voltage *differential* between BTm and BCm is able to influence the behavior of the memory, then a common change (whether increasing or decreasing) in the voltage of BTm and BCm has no impact on the behavior. In other words, the triple twist transforms the differential mode noise into common mode noise for which the sense amplifier is insensitive

As an example, Figure 7 shows the pre-sense coupling voltage development on BTm and BCm as a result of a logic 1 stored in both neighboring cells. During pre-sensing, and since the accessed cell on BCt has a logic 1, an up voltage of V_a develops on BCt, which in turn results in pulling BCm up by V_{b1} and in pulling BTm up by V_{b2} at the same time. Both V_{b1} and V_{b2} are equal and therefore do not result in a differential voltage developing between BTm and BCm. The same situation takes place with BCb, where an up voltage V_c induces an up voltage of V_{d1} on BCm and an up voltage of V_{d2} on BTm. Since both V_{d1} and V_{d2} are equal, they do not result in a differential voltage developing between BTm and BCm.

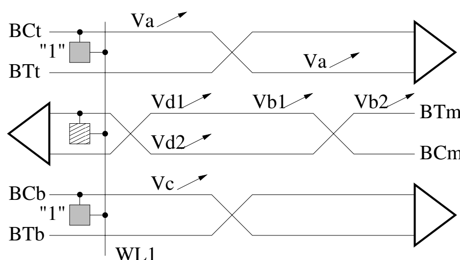

Figure 7. Pre-sense voltage development for a triple twist.

5 Analysis results

This section presents the results of the simulation analysis of the three different BL organizations shown in Figure 4 and discusses their impact of the faulty behavior. The simulation employs the concepts of result planes and the cell sense voltage (V_{cs}) curves previously used to analyze the faulty behavior of DRAMs in general [Al-Ars02], and to evaluate the impact of BL coupling in particular [Al-Ars04].

Consider the defective DRAM cell shown in Figure 8, where a resistive open (R_{op}) between BT (true bit line) and the pass transistor limits the ability to control and observe the voltage across the cell capacitor (V_c). The open is injected into Cell 1 and simulated as part of the reduced memory model shown in Figure 1. The reasons for choosing this specific cell defect to analyze BL coupling include the following.

1. This defect models a strap connection between the drain of the pass transistor and the cell capacitor that is difficult to manufacture and may have resistive values that are higher than normal [Adler95].
2. Gradually increasing the resistive value of this defect results in the gradual reduction of the differential BL signal needed for proper sensing. Therefore, this defect is ideal for analyzing the impact of BL coupling on the faulty behavior.
3. The relative simplicity of the defect model and the required fault analysis.

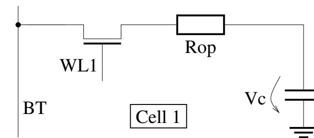

Figure 8. Open injected into Cell 1.

Figure 9 shows three result planes for the three BL organizations discussed in this paper: a. solid BLs, b. single twist and c. triple twist. The x-axis of the result plane represents the value of the voltage within the cell V_c, while the y-axis represents the value of the defect resistance R_{op}. Each result plane shows 4 different V_{cs} curves, one for each of the four possible BGs: $0x0$, $1x0$, $0x1$ and $1x1$. The V_{cs} curve is the cell-sense threshold voltage, which is the cell voltage at which the sense amplifier distinguishes a 0 from a 1. This means that if a read operation is performed when $V_c > V_{cs}$ then the sense amplifier detects a logic 1, while $V_c < V_{cs}$ results in sensing a logic 0. Therefore, the leftmost V_{cs} curve in any of the result planes is associated with the worst-case BG for detecting a 0, while the rightmost V_{cs} curve is associated with the worst-case BG for detecting a 1.

Figure 9(a) presents the 4 BGs associated with the solid BL organization, where no twisting is used. The figure shows that the worst-case BG for detecting a 0 in the defective cell is $0x0$, while the worst-case BG for detecting a 1 in the cell is $1x1$. In other words, a worst-case BG of xxx is needed, which means that the post-sense coupling effect is prevalent for the simulated memory model according to Section 3.

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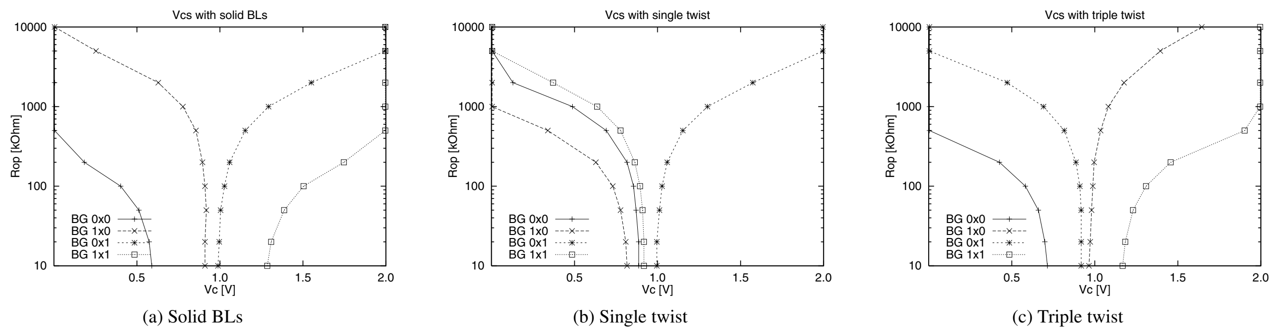

(a) Solid BLs (b) Single twist (c) Triple twist

Figure 9. V_{cs} curves with different BGs for the (a) solid BL organization, (b) single twist, and (c) triple twist.

Figure 9(b) shows the 4 BGs associated with the single twist BL organization, which according to the analytical evaluation presented in Section 4 should only be affected by pre-sense BL coupling. The figure shows that the worst-case BG for detecting a 0 in the cell is $1x0$, while the worst-case BG for detecting a 1 in the cell is $0x1$. In other words, a worst-case BG of $\bar{x}xx$ is needed, which indeed matches that of a pre-sense coupling effect. This means that by introducing the single twist into the model, post-sense coupling effects (prevalent before introducing the twist, as indicated by Figure 9(a)) have been neutralized, which makes pre-sense coupling effects become the more prevalent sort of BL coupling.

Figure 9(c) shows the 4 BGs associated with the triple twist BL organization, which according to the analytical evaluation presented in Section 4 should totally eliminate pre-sense as well as post-sense BL coupling effects. The figure shows that the worst-case BG for detecting a 0 in the cell is $0x0$, while the worst-case BG for detecting a 1 is $1x1$, which indicates an existing post-sense coupling effect on the defective cell. Although this may seem to be contradictory with the analytical evaluation of Section 4, it can actually be explained by the fact that Section 4 only took into consideration first-order BL coupling effects caused by BL to BL coupling capacitances. It is important to note, however, that second-order BL coupling exists in the form of BL to "line" to BL coupling (BL to WL to BL, for example), which is negligible when compared to the direct first-order BL to BL coupling. But in the absence of first-order coupling, second-order coupling becomes the major factor in the faulty behavior. This is also indicated by the fact that the V_{cs} curves of Figure 9(c) are located closer together than those of Figure 9(a), which means that the post-sense coupling effect with the triple twist represents a fraction of the full post-sense coupling effect without any twists.

In the case of the triple twist, analytical evaluation of second-order BL coupling effects on the behavior is overly complex, and electrical simulation can provide considerable insight into the faulty behavior of a defective memory.

6 Conclusions

This paper analyzed the effects of BL twisting on the faulty behavior of DRAMs. Three well-known BL organizations have been presented and analyzed: solid BLs, single twists and triple twists. Two different types of BL coupling were described (pre-sense and post-sense coupling), and the way BL twisting influences these two coupling effects was analyzed. The single twist eliminates post-sense coupling which makes pre-sense coupling the more prominent factor, while the triple twist eliminates pre-sense and post-sense first-order coupling which makes second-order coupling become prominent. The analytical evaluation of BL twisting was validated by electrical simulation and shown to correspond well with the analytical results. Fault analysis based on electrical simulation can provide great insights into the faulty behavior, and reduces the complexity of analyzing the second-order coupling promoted by the triple twist.

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