J Electron Test (2012) 28:15–25
DOI 10.1007/s10836-011-5270-3

Test Impact on the Overall Die-to-Wafer 3D Stacked IC Cost

Mottaqiallah Taouil · Said Hamdioui · Kees Beenakker · Erik Jan Marinissen

Received: 23 January 2011 / Accepted: 8 November 2011 / Published online: 8 December 2011

Abstract One of the key challenges in 3D Stacked-ICs (3D-SIC) is to guarantee high product quality at minimal cost. Quality is mostly determined by the applied tests and cost trade-offs. Testing 3D-SICs is very challenging due to several additional test moments for the mid-bond stacks, i.e., partially created stacks. The key question that this paper answers is what is the best test flow to be used in order to optimize the overall cost while realizing the required quality? We first present a framework covering different test flows for 3D Die-to-Wafer (D2W) stacked ICs. Thereafter, we present a cost model that allows us to evaluate these test flows. The impact of different test flows on the overall 3D-SIC cost for several die yields and stack sizes are investigated; a breakdown of the cost into test, manufacturing and packaging cost is also provided. Our simulation results show that both the test cost and the overall cost in D2W stacking strongly depends on the selected test flow; test flows with pre-bond and mid-bond stacking tests (performed during the stacking process) show a higher test cost share, but significantly reduce the overall 3D-SIC cost.

Keywords 3D test flow · 3D test cost · Die-to-Wafer stacking · 3D manufacturing cost · Through-Silicon-Via

Responsible Editor: Y. Zorian

M. Taouil (✉) · S. Hamdioui · K. Beenakker
Faculty of EE, Mathematic and CS, Delft University of Technology, Mekelweg 4, 2628 CD Delft, The Netherlands
e-mail: M.Taouil@tudelft.nl

S. Hamdioui
e-mail: S.Hamdioui@tudelft.nl

K. Beenakker
e-mail: C.I.M.Beenakker@tudelft.nl

E. J. Marinissen
IMEC vzw, 3D Integration Program, Kapeldreef 75, 3001 Leuven, Belgium
e-mail: erik.jan.marinissen@imec.be

1 Introduction

The potential benefits that 3D Stacked ICs (3D-SICs) offer is leading to an escalation of research and work both in academy and industry [6, 9, 11, 14–16, 20, 21]. The feasibility to stack dies allows long wires that normally cover long distances to be mapped on Trough-Silicon-Vias (TSVs). TSVs are holes that go through the silicon substrate filled with a conducting material. TSVs reduce the interconnect distance between stacked dies. This lowers the latency and power dissipation in such connections. Moreover, the incorporation of possibly heterogeneous dies results in a high transistor density at a smaller footprint. The ability to place the TSVs anywhere on the surface of the chip allows the establishment of high bandwidth communication between dies [6].

Wafer-to-Wafer (W2W), Die-to-Wafer (D2W) and Die-to-Die (D2D) bonding [9] are the existing methods that could be employed in order to manufacture 3D-SICs. W2W bonding leads to highest throughput, as dies are processed in parallel at wafer level, and makes the manufacturing of tiny dies feasible [9]. Regarding yield, D2W and D2D are superior, due to the opportunity to apply Known-Good-Die (KGD) testing [9].

This paper focuses on D2W stacking as it is currently the most relevant stacking approach in industry.

Testing for manufacturing defects is required to satisfy the required product quality. In addition to the traditional defects that may occur during processing of planar wafers, new faults inherent to the 3D processes have to be considered. Good tested dies in the *pre-bond* test phase could get corrupted during the stacking. Typical sources of die failures during stacking include the processing steps involved in thinning, bonding, as well as TSV failures such as misalignments and opens [10]. If it is known beforehand that a particular stack is corrupted, silicon, stacking and bonding costs can be prevented for the successive dies that have to be stacked. The number of test moments, both for interconnects as well as dies, increases significantly during stacking. Pre-bond tests prevent corrupted dies from entering the stack, while post-bond tests verify the correctness of the dies and interconnects for the stack. To guarantee high 3D-SIC product quality at low cost, appropriate test flows need to be developed that take the different test phases (e.g. pre-bond testing, post-bond testing, etc.) into consideration.

This paper introduces a framework of test flows and analyzes the impact of such test flows on the overall cost of D2W based 3D-SIC. An appropriate cost model is developed to accurately evaluate the impact of the test flows while considering different process parameters such as stack size, die yield, etc.

The remainder of the paper is organized as follows. Section 2 introduces the test flow framework. Section 3 describes the cost model. Section 4 describes the simulation setup. Section 5 presents the simulation results and discusses them. Section 6 concludes the paper.

2 Test Flow Framework

This section presents first the differences between 2D and 3D test flows and shows that for 3D many test moments are possible. These test moments are thereafter compiled into a framework of test flows.

2.1 2D Versus 3D Test Flow

A conventional 2D test flow for planar wafers is depicted in Fig. 1a [13]. Here, usually two *test moments* are applicable; i.e., a wafer test prior to packaging and a final test after packaging. The wafer test can be cost-effective when the yield is low, since it prevents unnecessary assembly and packaging costs. The goal of the final test is to guarantee the final quality of the packaged chip. During the manufacturing of a 3D-SIC, additional test points can be defined for each partial stack. At each test point a distinction can be made between die tests and interconnect tests. Die tests ensure the functionality of individual dies, while interconnect tests ensure functional TSVs between dies. For 3D-SICs, four test moments can be distinguished in time as depicted in Fig. 1b, and explained next.

1. T_{pr}: n *pre-bond* wafer tests, since there are n layers to be stacked. T_{pr} tests prevent faulty dies entering the stack. Besides die test, preliminary TSV interconnect tests can be applied (in case of via-first [9]) as well. An example of a preliminary test that detects some faulty TSVs could be a capacitance test [5].
2. T_{mi}: n-2 *mid-bond* tests applicable for partial created stacks. In this case, either the dies, the interconnects, their combination or none of them can be tested. Good tested dies in the pre-bond test phase could get corrupted during the stacking process as a consequence of e.g., die thinning, and bonding [10]. In the simulation model of our test flows, first the interconnects are tested and thereafter the dies in bottom up order (in case both are tested for); if a fault is detected in the interconnects, then there is no need to test the dies as the 3D-SIC will be faulty anyway. The reason for this particular test order is that the test cost for interconnects is considered cheaper, as will be explained in Section 3.
3. T_{po}: one *post-bond* test. This test can be applied after the complete stack is formed. Analogous to wafer testing in the 2D test flow, T_{pr} can be applied to save unnecessary assembly and packaging costs. Both interconnects and dies can be tested.
4. T_{fi}: one *final* test can be applied after assembly and packaging to ensure the required quality of the complete 3D-SIC. Other specific packaging related tests could be applied at this test moment as well.

Note that in total there are $2 \cdot n$ different test moments.

Depending on whether one or more companies are involved in the manufacturing of 3D-SICS, different requirements can be set for the pre-bond wafer test quality [12]. If the wafers are produced by one or more companies and the final 3D-SIC product is processed and manufactured by another company, a high pre-bond wafer test quality (e.g. a KGD) often is agreed upon. If a KGD contract is in place, high-quality pre-bond testing is required. If such a contract is not in place, the pre-bond test quality is subject to optimization. This means, there is not only the option to perform pre-bond testing or not, but also to perform pre-bond testing at a higher or lower test quality. Faulty

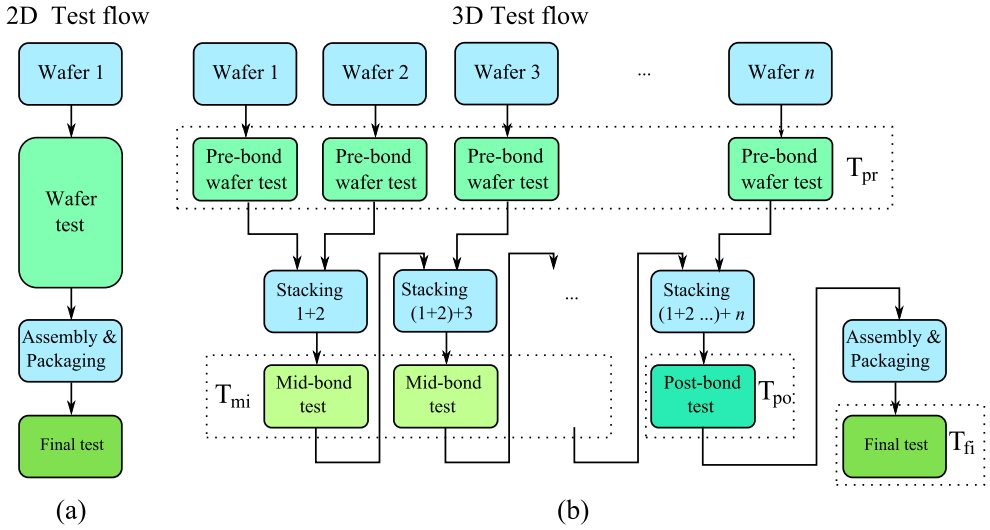

Fig. 1 2D versus 3D D2W test flows

undetected dies can be detected in a later stage, e.g., in higher quality final tests. Similarly, high quality mid- or post-bond tests (Known-Good-Stack tests) can be applied.

2.2 3D Test Flow Framework

The test flow framework for 3D D2W stacking can be extracted from the test flow moments depicted in Fig. 1b. Depending on whether no or at least one test is performed at each possible test moment, we can distinguish 2^{2n} possible test flows out of $2n$ test moments. This number will further increase if we consider that tests at each phase may target different faults; e.g., if we assume that T_{mi} may test (1) one or more interconnects, (2) one or more dies, (3) a combination of (1) and (2), or (4) none, then the number of possibilities for T_{mi} will be 4^{n-2}. This increases the number of test flows from 2^{2n} to $2^n\,(T_{pr}) \times 4^{n-2}\,(T_{mi}) \times 2\,(T_{po}) \times 2\,(T_{fi}) = 2^{3n-2}$. It is clear that considering all 'theoretical' possible test flows will result in an unmanageable space. Therefore, realistic assumptions have to be made in order to create a clear overview (without loss of generality) for the work presented in this paper. Our assumptions consist of the following.

1. A linear stacking approach is assumed, i.e., dies are stacked sequentially in a bottom-up approach starting from the bottom wafer. During stacking, it is assumed that only the *top* two dies and the interconnect between them could be corrupted; they are assumed to be defect-prone to stacking/bonding steps like heating, thinning, pressure.
2. All die tests are identical; a similar assumption applies to all interconnects.
3. Each test flow has to guarantee that a 3D-SIC is fault free before it is packaged to prevent unnecessary assembly and packaging cost. The test phases 'T_{pr}+T_{mi}+T_{po}' test each die and each interconnect of the SIC at *least* once.
4. The final test in T_{fi} is a complete test, i.e., all dies and interconnects are tested.

Because of Assumption 1, T_{mi} will test only for one of the following:

- Only for the *interconnect* between the top dies (i_t = top interconnect).
- Only for the *top dies* (d_t = dies top).
- For both the *top interconnect* and *top dies* ($i_t d_t$).
- none (n).

This results into $T_{mi} \in \{i_t, d_t, i_t d_t, n\}$.

Table 1 shows the test flow framework of all possible test flows based on the above assumptions. The first column denotes the two possibilities for T_{pr} (pre-bond test), either it is performed ('y') or not ('n'). The second column gives the four possible values of $T_{mi} \in \{i_t, d_t, i_t d_t, n\}$. The last column lists the different

Table 1 Test flow framework

Test flow	T_{pr}	T_{mi}	T_{po}
TF1	n	n	$i_a d_a$
TF2	n	i_t	$i_a d_t$
TF3	n	i_t	$i_t d_a$
TF4	n	$i_t d_t$	$i_t d_t$
TF5	y	n	$i_a d_a$
TF6	y	i_t	$i_a d_t$
TF7	y	i_t	$i_t d_a$
TF8	y	$i_t d_t$	$i_t d_t$

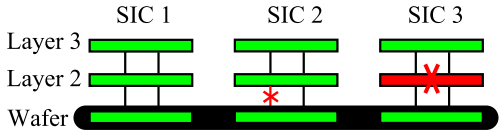

Fig. 2 Examples of defects (x) occurring during stacking

possible values of T_{po}. In order to satisfy Assumption 3 (a fault-free 3D-SIC prior to packaging) T_{po} is limited to the following values:

- $i_t d_t$: test for *top* interconnect and *top* dies.
- $i_t d_a$: test for *top* interconnect and *all* dies.
- $i_a d_t$: test for *all* interconnects and *top* dies.
- $i_a d_a$: test for *all* interconnects and *all* dies.

Each possible test flow is given a name in the table; e.g., TF1 denotes a test flow based on no T_{pr}, no T_{mi} and $T_{po} = i_a d_a$. There are eight test flows in total, i.e., TF1 to TF8.

To provide more insight into the different test flows and their impact on the total 3D-SIC cost, we consider the example shown in Fig. 2. It consists of three SICs with $n = 3$ layers each. For simplicity, it is assumed that all dies in the pre-bond phase were manufactured with 100% yield and that two faults occurred during stacking of Layer 2 on the bottom layer, one in SIC2 and one in SIC3. In SIC2, a fault occurred in the interconnects between the bottom die (i.e., Layer 1) and the die at Layer 2 (e.g., due to misaligned TSVs), while in SIC3 a defect occurred in Layer 2 (e.g., due to thinning). It is assumed that during the mid-bond and post-bond tests, first interconnects are tested, followed by the dies in bottom up order.

Table 2 shows the impact of four test flows TF1, TF2, TF3 and TF4 on three different cost factors: manufacturing, test, and packaging. Each entry in the table is composed of four numbers, associated with SIC1, SIC2 and SIC3 respectively, followed by their sum. The manufacturing, test and packaging costs for the three 3D-SICs are explained next.

The manufacturing cost is considered to include the number of used dies (the second column of the table) and the number of stacking operations that are performed (the third column of the table). For example, in TF1 only $T_{po} = i_a d_a$ is performed (see Table 1); therefore this will result in: (a) stacking of three dies per 3D-SIC, hence $3 + 3 + 3 = 9$ dies, and (b) two stacking operations per SIC, thus a total of $2 + 2 + 2 = 6$ stacking operations.

The test cost is classified according to the test phases defined in Section 2.1; i.e., pre-bond wafer tests T_{pr}, mid-bond tests T_{mi}, post-bond tests T_{po} and final tests T_{fi}. Note that T_{fi} is not included in the table as we assumed that final tests are the same for all test flows (Assumption 4). Except for the T_{pr} phase, each test phase distinguishes between tests for interconnects and tests for dies. Consider test flow TF4 which performs the following tests (see also Table 1):

- No pre-bond test (i.e., $T_{pr} = n$): no tests are executed and therefore no pre-bond tests for the three SICs are performed.
- Mid-bond tests consisting of (a) test for top interconnect and (b) tests for top dies (i.e., $T_{mi} = i_t d_t$). Note that there is $n - 2 = 1$ test moment. Hence, in this phase TF4 tests for the interconnects between the bottom layer and Layer 2 of each SIC, resulting in $1 + 1 + 1 = 3$ tests. In addition, TF4 tests for two bottom dies of SIC1 (i.e., the first two layers), no dies in SIC2 (since the interconnect found to be faulty during i_t tests) and the two bottom dies of SIC3 resulting into $2 + 0 + 2 = 4$ tests.
- Post-bond tests consisting of testing top dies and top interconnects of the SIC ($T_{po} = i_t d_t$). In this phase, TF4 tests only for the top interconnects and the two top dies of SIC1, not those of SIC2 and SIC3 as they are already considered faulty after the mid-bond tests were applied. This results in a total test of one interconnect and two dies during this phase.

The packaging cost is given in the last column of Table 2. Because of Assumption 3, the packaging cost is the same for all the four test flows. Only SIC1 will be packaged, while the other two SICs will be discarded.

Table 3 summarizes the cost required to manufacture and test the three 3D-SICs. The table clearly shows the

Table 2 Impact of test flows

TF	Manufacturing cost		Test cost					Packaging cost
	#dies	#stacking operations	T_{pr} #dies	T_{mi} #inter	T_{mi} #dies	T_{po} #inter	T_{po} #dies	#packaged SICs
TF1	$3+3+3=9$	$2+2+2=6$	$0+0+0=0$	$0+0+0=0$	$0+0+0=0$	$2+1+2=5$	$3+0+2=5$	$1+0+0=1$
TF2	$3+2+3=8$	$2+1+2=5$	$0+0+0=0$	$1+1+1=3$	$0+0+0=0$	$1+0+1=2$	$3+0+2=5$	$1+0+0=1$
TF3	$3+3+2=8$	$2+2+1=5$	$0+0+0=0$	$0+0+0=0$	$2+2+2=6$	$2+1+0=3$	$2+2+0=3$	$1+0+0=1$
TF4	$3+2+2=7$	$2+1+1=4$	$0+0+0=0$	$1+1+1=3$	$2+0+2=4$	$1+0+0=1$	$2+0+0=2$	$1+0+0=1$

Table 3 Manufacturing versus test trade-off

Test flow	Manufacturing cost		Test cost	
	#dies	#stacking operations	#dies	# interconnects
TF1	9	6	5	5
TF2	8	5	5	5
TF3	8	5	9	3
TF4	7	4	6	4

cost trade-off between manufacturing and testing. For example, TF1 requires the manufacturing of nine dies and needs six stacking operations at a test cost of testing five dies and five interconnects. On the other hand, TF4 requires the manufacturing of seven dies and needs four stacking operations, at a test cost of six dies and four interconnects. Choosing the test flow resulting in optimal overall cost needs the evaluation of all possible test flows using an appropriate generic cost model; the latter is given in the next section.

3 Cost Model

To evaluate the impact of the different test flows on the overall 3D-SIC cost, an appropriate generic cost model is built. Figure 3 shows a diagram of this cost model; it considers three major input classes [19]:

- Manufacturing: this consists of all parameters related to 3D-SIC manufacturing process such as wafer cost, costs required for wafer processing, TSVs and 3D bonding and thinning, the number of dies per wafer, die yield etc.
- Test: This consists of all parameters related to DFT, test and test flows such as cost related to testing dies and interconnects. Test flows have a large impact on this cost since they determine when and what to test for.
- Packaging: The cost of 3D-SIC packaging.

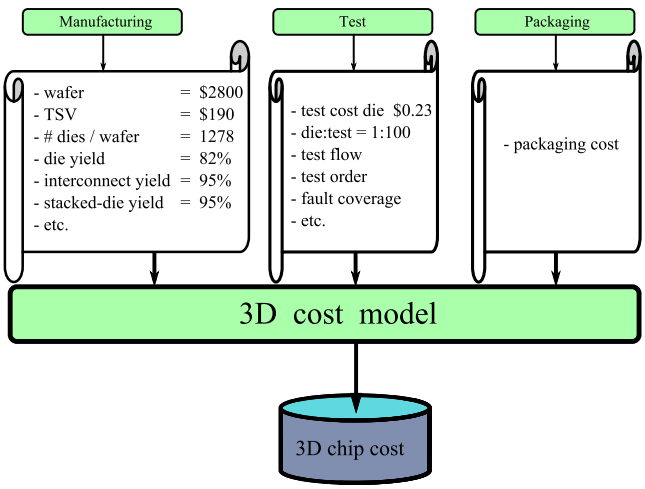

Fig. 3 Test cost model 3D D2W Stacking

The cost model is able to evaluate each test flow and calculates the overall 3D cost per test flow. In addition, it also determines the share of the test cost as compared to the overall cost. In fact, the model performs more *elaborate* and *comprehensive* calculations and analysis of those explained in the example of Section 2.2. The model has, for example, the ability to evaluate parallel testing of dies and it can handle more test flows than those described in Table 1. The model collects statistical data (in our case based on 1,000 wafers) while considering the different costs. The monitored data includes e.g., the number of used dies, the number of stacking/bonding operations, the number of packaged SICs, the number of tests performed (for dies and interconnect), etc.

Since the purpose of this work is to investigate the impact of different test flows rather than to observe the impact of different manufacturing processes (e.g., transistor feature size, TSV via-first or via-last, Face-to-Face or Back-to-Face bonding orientation, the number of TSVs etc.), the manufacturing costs are assumed to be constant; these will be discussed in Section 4.1. However, the test cost strongly depends on other parameters like die yield, interconnect yield, stacking yield, number of stacked layers, etc. These parameter are described in Section 4.2.

4 Simulation Setup

In order to appropriately perform simulations, different input parameters of the cost model have to be defined. These parameters are classified into fixed and variable ones.

4.1 Fixed Parameters

The fixed parameters of each of the input classes are given next.

Manufacturing Cost It includes wafer cost, costs required for wafer processing, TSV fabrication and 3D stacking/bonding. For wafers and their processing, we used the cost models of [17] and [4]; the total price of a 300 mm wafer is estimated at approximately $2,779. The model in [17] considers a variety of costs, including installation, maintenance, lithography and material. For TSV fabrication, the work of EMC-3D consortium [18] is used; the cost to fabricate 5 μm TSVs in a single wafer is assumed to be $190 and these cost

are additive to the wafer cost. We assume the cost of manufacturing TSVs to be 60% of the 3D stacking process cost [22].

Test Cost This cost is related to tests and test flows. To estimate the test cost per die, the model in [3] is used; it includes depreciation, maintenance and operating cost and assumes five ATE machines operating simultaneously. The derived test cost equals 3.82 $cent/second per die. Assuming a test time of 6 seconds per die, the test cost will be $0.23 per die. To estimate the interconnect test cost, a ratio of 1:100 between the test time of dies and interconnects is assumed (as in [23]).

Packaging Cost The packaging cost for 3D SICs used in our model is based on oral conversations with Boschman BV [2] and DIMES [8]. The costs are comprehensive and include machine, maintenance, labor and material cost.

4.2 Variable Parameters

Several variables, either related to manufacturing or test, have a large impact on the overall cost picture of 3D-SICs. Examples of the former are die yield, stack size, number of dies per wafer, stack yield, etc; and examples of the latter are fault coverage, test order, etc. The default values of the parameters used in our cost model are described next and are depicted in Fig. 3. In the remainder of this paper, these default parameters (depicted in Fig. 3) are referred to as the reference process.

Manufacturing The die yield is based on the stacking process in [23], where a standard 300 mm diameter wafer is used with an edge clearance of 3 mm. This work assumes a defect density of $d_0 = 0.5$ defects/cm^2 and a defect clustering parameter $\alpha = 0.5$. With a die area $A = 50$ mm^2, the number of Gross Dies per Wafer (GDW) are estimated to be 1,278 [7]. With the negative binomial formula for yield, a die yield of $Y_D = (1 + \frac{A \cdot d_0}{\alpha})^{-\alpha} = 81.65\%$ is expected [3]. For the stack size we assume a default stack size $n = 5$. The stacking yield is composed of two parameters: the interconnect (TSV) yield Y_{INT} and the stacked-die yield Y_{SD}. In our simulations, the interconnect yield Y_{INT} is considered to be 95%. For the good dies that enter the stack, a small probability exists that they get corrupted during stacking; this is modeled by the stacked-die yield Y_{SD} and is assumed to be 95% as well. Several research works assume a complete stack yield of approximately 95% [1, 23].

Test The order of testing is performed sequentially, bottom-up, starting first with the interconnects followed by the dies. In this work, we consider only the eight test flows defined in Table 1 for evaluation and analysis. A fault coverage of 100% is assumed for both dies and interconnect.

5 Simulation Results

In this section, we measure the impact of the test flows defined in Table 1 by using the cost model depicted in Fig. 3. We investigate not only the impact of the test flows on the overall cost, but also the share of test cost as compared with test, manufacturing and packaging; this will be performed for different die yields and stack sizes. The following experiments have been conducted:

1. **Impact of stack size** In this experiment, the impact of different test flows and the share of test cost will be investigated while considering different stack sizes n: $2 \leq n \leq 6$.
2. **Impact of die yield** Similar experiment as the previous one, but now by having a fixed stack size of $n = 5$, and variable die yield Y_D: $60\% \leq Y_D \leq 90\%$.
3. **Impact of stack yield** In this case, the reference process is used (e.g., $n = 5$, $Y_D = 81.65\%$, etc.), but the stack yield is varied; this yield consists of interconnect yield Y_{INT} and stacked-die yield Y_{SD}: $91\% \leq Y_{INT}, Y_{SD} \leq 99\%$.

5.1 Impact of Stack Size

Figure 4 depicts the relative overall 3D-SIC cost of the test flows for a stack size between $2 \leq n \leq 6$. Here, the 3D cost for each test flow is normalized to the 3D cost of TF1 for each stack size. For $n = 2$, test flows TF1, TF2, TF3 and TF4 result in equal cost; the same thing applies to test flows TF5, TF6, TF7 and TF8. The reason is that in this case, the test flows are the same

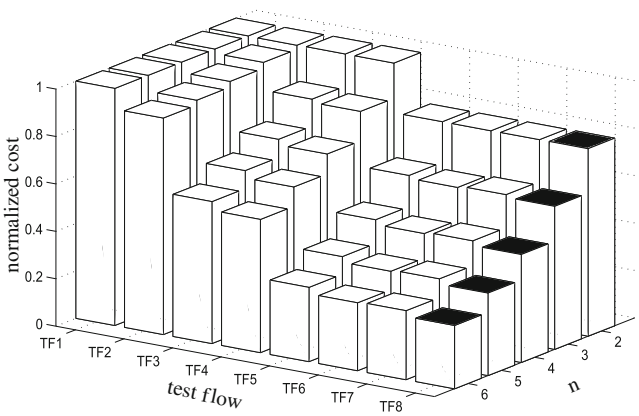

Fig. 4 Normalized overall cost for different stack sizes

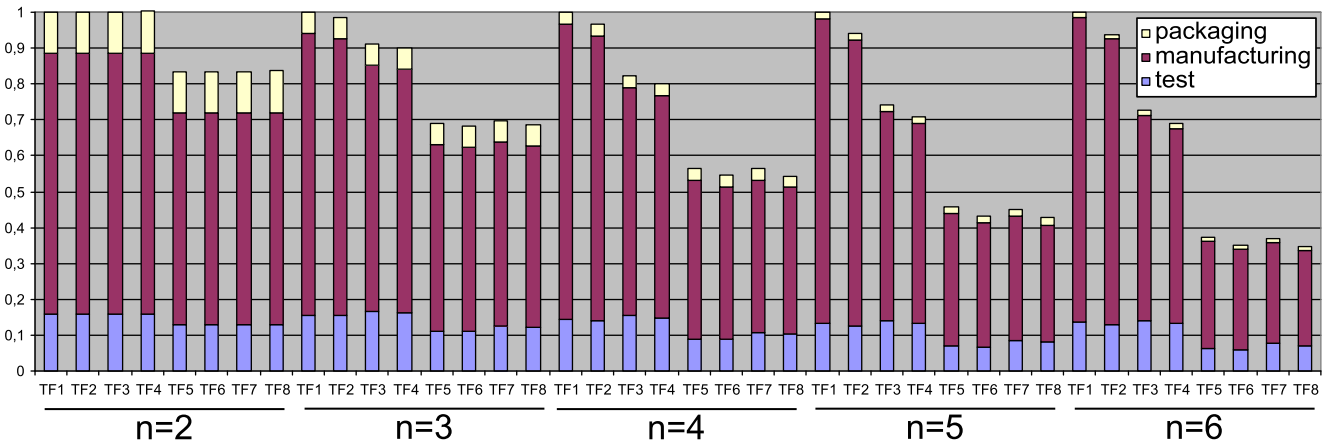

Fig. 5 Cost breakdown for different stack sizes

(as there are no mid-bond test moments). The following conclusions can be drawn from the figure:

- Test flows with pre-bond tests significantly reduce the overall cost. The larger the stack size n, the larger the reduction.
- TF8 is the most cost-effective test flow irrespective of n. The bars with black tops represent the test flows with the lowest costs per layer. For $n = 2$, TF5 until TF8 result in same cost.
- TF2 has a marginal impact on the cost reduction irrespective of n. This is because TF2 neither performs pre-bond tests nor die tests during the mid-bond phase. This is not the case for TF3 and TF4, as they both test for dies in the mid-bond phase.
- While test flow TF2 results in higher cost than test flow TF3, the reverse occurs for the test flows TF6 and TF7. Note that TF1 and TF3 are similar to TF6 and TF7, respectively, except that TF6 and TF7 also include pre-bond testing. In case of TF6 and TF7 only good dies will be stacked. Hence, it is cost-wise cheaper to test the interconnects (TF6) than to re-test the dies (TF7) during the mid-bond phase. Nevertheless, testing both interconnects and dies during the mid-bond phase is the most cost-effective test flow (i.e., TF8).

Figure 5 gives a different representation of Fig. 4, it breaks down the cost into manufacturing, test and packaging cost. In addition to the conclusions drawn from Figs. 4 and 5 shows that the share of packaging cost decreases as the stack size increases, while the test share increases with larger stack sizes. For test flow TF8, the test share is 15.4% for a stack size of $n = 2$, while this ratio increases to 20.6% for a stack size of $n = 6$. It is worth noting that although TF8 has the highest test cost share, it results in the lowest overal 3D-cost.

To get more insight into the impact of test flows and the cost break down, we will zoom on the case of the reference process. Figure 6 shows the overall cost normalized to TF1 for the eight test flows. TF3 results in an overall cost which is 74.27% of that of TF1. Since the stack yield is assumed to be much higher than the die yield, test flow TF3 (test for dies during the mid-bond phase) results in a lower cost than TF2 (test for interconnects only during the mid-bond phase). The reverse occurs for the test flows TF6 and TF7. Test flow TF8 is able to reduce the cost by 57.34% compared to TF1 (that considers only post-bond tests) and 6.7% as compared to test flow TF5 (that contains pre-bond and post-bond tests).

Figure 7 plots the breakdown of the 3D cost for the reference process. For each test flow, the shares of test, manufacturing and packaging are depicted. From the Figs. 7 and 5 the following can be concluded:

- The manufacturing cost is the most dominant cost factor for each test flow. However, the absolute

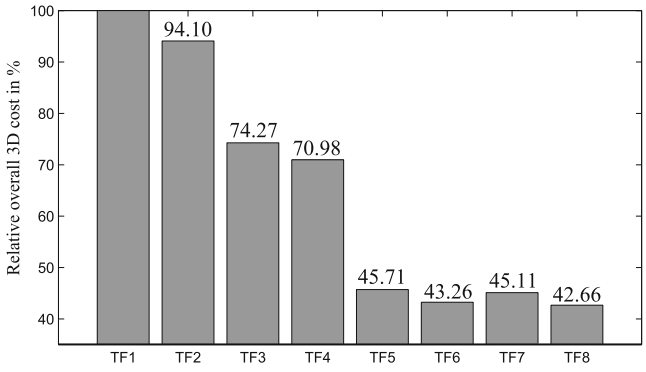

Fig. 6 Normalized 3D cost for the reference process

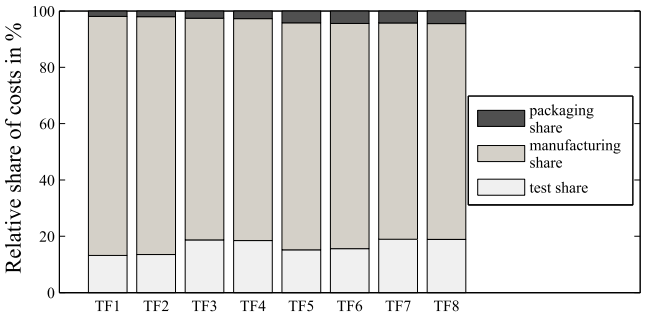

Fig. 7 Cost breakdown for the reference process

manufacturing cost depends strongly on the selected test flow.
- Test flows resulting in lower overall 3D cost do have a higher packaging cost share; this applies for test flows TF5 to TF8. This is because these test flows guarantee fault-free 3D-SICs before packaging.
- The share of test cost is between 13% and 19% depending on the test flow. Test flows containing die tests during the mid-bond phase result in a relatively higher test cost share as compared with the rest. For instance, test flow TF3, TF4, TF7 and TF8 result in a test cost share of about 19%.
- A higher test cost share does not necessarily result in higher overall cost.

5.2 Impact of Die Yield

Figure 8 depicts the relative 3D cost of the test flows with a die yield varying between $60\% \leq Y_D \leq 90\%$ for the reference process. Here, the 3D cost for each test flow is normalized to the 3D cost of TF1. From the figure we conclude the following.

- Test flows with pre-bond tests significantly reduce the overall cost. The lower the die yield, the larger the reduction (except for TF2 since this test flow does not test for dies during the pre-bond and mid-bond phases).
- TF2 has a marginal impact on the cost, irrespective of the die yield. This is not the case for TF3 and TF4, as they both test for dies in the mid-bond phase.
- Similar conclusions can be drawn as those from Fig. 4 for the test flows enabled with pre-bond testing. It is cheaper to test for interconnects only (TF6) than to test for dies only (TF7) during the mid-bond test phase. Nevertheless, testing for interconnects and dies during the mid-bond phase is the most cost-effective test flow (i.e., TF8).

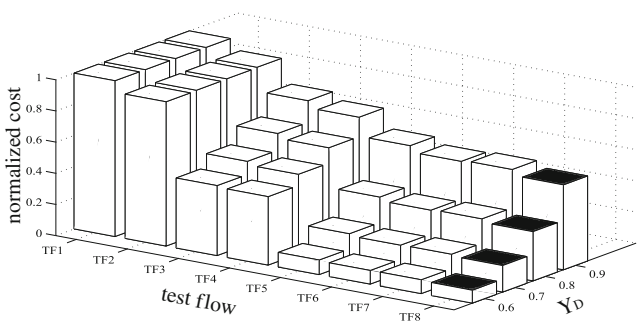

Fig. 8 Normalized cost for different die yields

Figure 9 gives the cost breakdown for the reference process and for $30\% \leq Y_D \leq 90\%$. For each Y_D, the overall costs are normalized to TF1. Within each bar, the share of test, manufacturing and packaging are depicted. The figure clearly reinforces the conclusions previously drawn from Fig. 8. For example, test flows with pre-bond tests (TF5 to TF8) result in the lowest overall cost irrespective of the value of the die yield; the cost difference with test flows without pre-bond test becomes more significant for lower yields. In addition, the figure reveals that TF8 results into the lowest overall cost in all cases, and that the test cost and packaging cost shares increases as the yield increases. The test and packaging share increase from 13 and 2%, respectively, for a die yield of 30%, to 20 and 5%, respectively, for a die yield of 90%. This figure also clarifies the importance of mid-bond tests; test flows with mid-bond tests result in lower cost. For example, TF8 results in 7% lower overall cost as compared to TF5; note that TF8 and TF5 are the same except that TF8 also consists of mid-bond tests.

5.3 Impact of Stack Yield

Figure 10 depicts the overall 3D cost versus stacked yield (i.e., interconnect Y_{INT} and stacked-die Y_{SD}) for the test flows. In the figure, Y_{INT} and Y_{SD} are set to either 91 and 99%. The 3D cost of the flows are normalized to the cost of TF1 for each different stack yield. The bars with black tops present test flows resulting in optimal overall cost per stacking yield. For example, for a stack yield of $[Y_{INT}, Y_{SD}] = [0.99, 0.99]$, TF6 is the most cost-effective test flow.

From the figure we conclude that TF6 and TF8 are the most cost-effective test flows. If Y_{SD} is very high (i.e., 99%), then TF6 is the best as it tests only for interconnect. However, in case $Y_{SD} = 91\%$, TF8 performs better, since it tests for dies during the mid-bond phase.

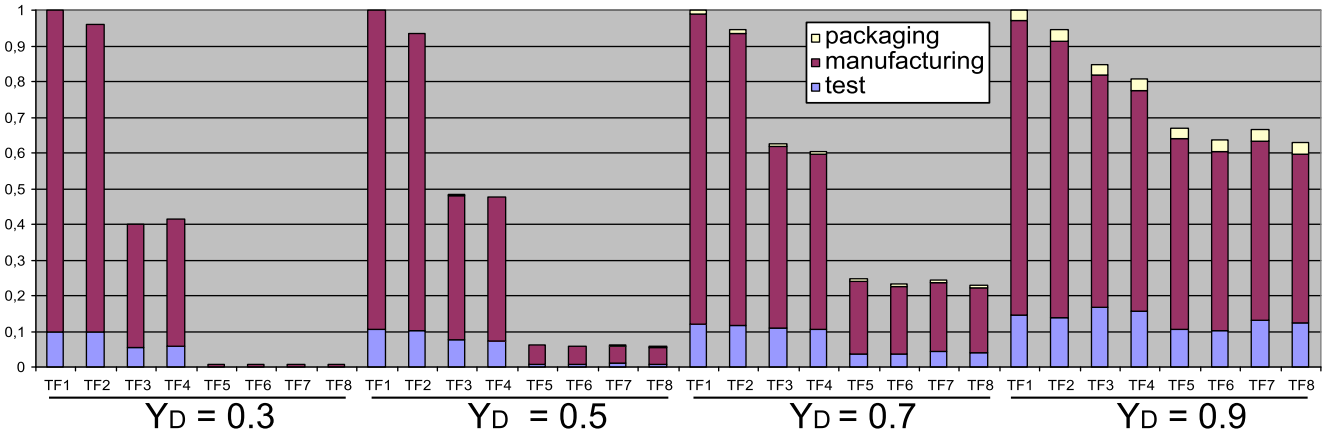

Fig. 9 Cost breakdown for variable die yield

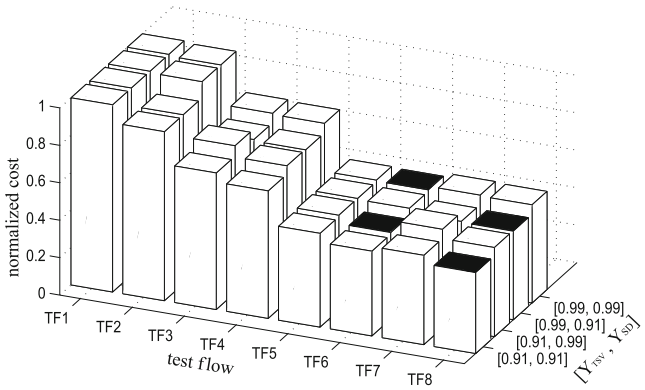

Fig. 10 Normalized overall cost for different stack yields

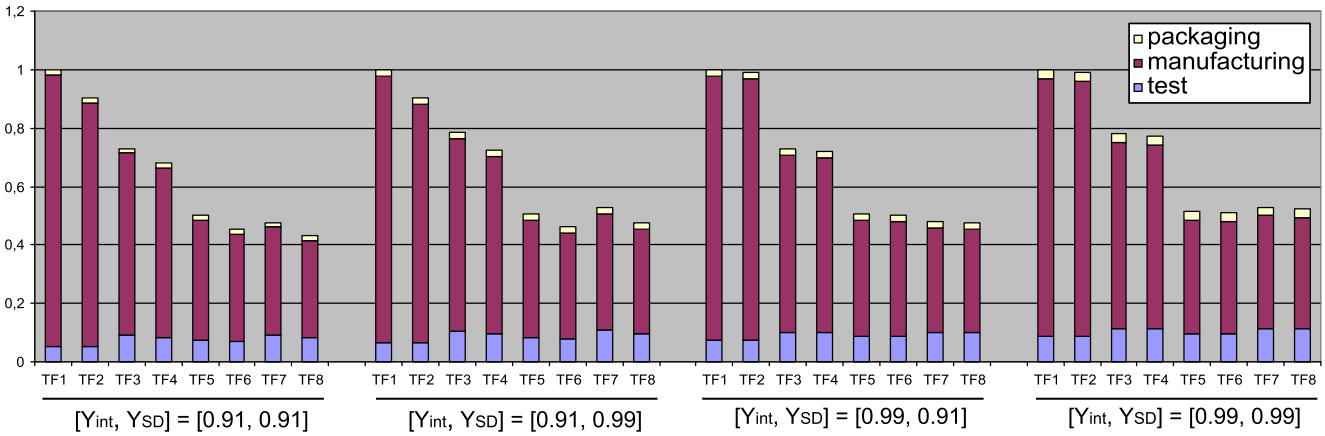

Fig. 11 Cost breakdown for variable die stack yield

Therefore, it is able to prevent unnecessary stacking of dies in faulty partial stacks.

Figure 11 shows the breakdown of the 3D cost. The higher the stack yield, the higher the test and packaging shares. For example, for TF8 the test and packaging shares are 19 and 4% respectively for a stack yield $[Y_{INT}, Y_{SD}] = [91, 91\%]$, while this increases to 21 and 6% for a stack yield of $[Y_{INT}, Y_{SD}] = [99, 99\%]$.

6 Conclusion

This paper investigated the impact of several 3D test flows on the total 3D cost in D2W stacking. It introduced a framework of test flows for 3D testing; each flow is based on a combination of tests applied at four test moments, i.e., the pre-bond wafer test, the mid-bond stack test, the post-bond test and the final test. A cost model that considers manufacturing, test and packaging cost is presented in order to evaluate the impact of different test flows on the overall cost.

The simulation results showed that the manufacturing cost is the most dominant in 3D stacking and strongly depends on the selected test flow. In addition, they revealed that test flows with pre-bond testing significantly reduced the overall cost. Mid-bond tests contributed to further cost savings. Although the share of test cost increases for such flows, the overall cost is significantly reduced. The cost saving increase with lower die yields and larger stack sizes. The conclusion of the paper indicates that in order to manufacture 3D-ICs at optimum cost, any DFT has to consider not only the infrastructure for pre-bond tests, but also for mid-bond tests for both dies and interconnects.

References

1. Beyne E (2008) 3D Integration Crossing IC technology, Packaging and Design Barriers, Semicon West, TechXPOT, Test Assembly & Packaging. http://www.semiconwest.org/cms/groups/public/documents/web_content/ctr_024376.pdf. Accessed 2010
2. Boschman Technology (2011) http://www.boschman.nl/. Accessed 2011
3. Bushnell M, Agrawal V (2000) Essentials of electronic testing for digital. Memory and mixed-signal VLSI circuits. Springer
4. Chappell J (2002) What costs most in 300 mm? As materials management becomes more complex, FOUP becomes first line of defense, http://findarticles.com/p/articles/mi_m0EKF/is_24_48/ai_87145967/. Accessed 2011
5. Chen P, Wu C, Kwai D (2009) On-chip TSV testing for 3D IC before bonding using sense amplification. Asian test symposium, pp 450–455
6. Davis WR et al (2005) Demystifying 3D ICs: the pros and cons of going vertical. IEEE Des Test Comput 22(6):498–510
7. de Vries DK (2005) Investigation of gross die per wafer formulas. IEEE Trans Semicond Manuf 18(1):136–139
8. Delft Institute of Microsystems and Nanoelectronics (2011) DIMES. http://www.dimes.tudelft.nl/. Accessed 2011
9. Garrou P (2008) Christopher Bower and Peter Ramm. Handbook of 3D Integration, Wiley-VCH
10. Lee H-HS, Chakrabarty K (2009) Test challenges for 3D integrated circuits. IEEE Des Test Comput 25(5):26–35
11. Loh G et al (2007) Processor design in 3D die-stacking technologies. IEEE Micro 27(3):31–48
12. Marinissen EJ (2010) Testing TSV-based three-dimensional stacked ICs. Design, automation and test in Europe, pp 1689–1694
13. Marinissen EJ, Zorian Y (2009) Testing 3D chips containing through-silicon vias. International test conference, pp 1–11
14. Patti RS (2006) Three-dimensional integrated circuits and the future of system-on-chip designs. Proc IEEE 94(6):1214–1224
15. Puttaswamy K et al (2007) Processor design in 3D die-stacking technologies. IEEE Trans Comput 27(3):31–48
16. Puttaswamy K et al (2009) 3D-integrated SRAM components for high-performance microprocessors. IEEE Trans Comput 58(10):1369–1381
17. Sematech Wafer Cost Comparison Calculator (2011) http://ismi.sematech.org/modeling/agreements/wafercalc.htm. Accessed 2011
18. Siblerud P (2008) Emc-3d consortium develops process and cost model for interconnect thru-silicon-via or (iTSV^{TM}) structures. http://emc3d.org/documents/pressReleases/2008/EMC3D_iTSV_CoO_PressRelease_final_Sept4_2008.pdf. Accessed 2011
19. Taouil M et al (2010) Test cost analysis for 3D die-to-wafer stacking. Asian Test Symposium, pp 435–441
20. Thorolfsson T et al (2009) Comparative analysis of two 3D integration implementations of a SAR processor. IEEE international conference on 3D system integration, pp 1–4
21. Tsai Y-F et al (2008) Design space exploration for 3-D cache. IEEE Trans Very Large Scale Integr (VLSI) Syst 16(4):444–455
22. Velenis D et al (2009) Impact of 3D design choices on manufacturing cost. IEEE international conference on 3D system integration, pp 1–5
23. Verbree J et al (2010) On the cost-effectiveness of matching repositories of pre-tested wafers for wafer-to-wafer 3D chip stacking. IEEE European test symposium, pp 269–274

Mottaqiallah Taouil received his MSc with honors in Computer Engineering from the Delft University of Technology (TUDelft), Delft, the Netherlands. He is currently pursuing a PhD at the same university in the Dependable Nano-computing group. His research interests include Reconfigurable Computing, Embedded Systems, VLSI Design & Test, Built-In-Self-Test, 3D stacked ICs, 3D Architectures, (3D) Design for Testability, (3D) Yield analysis and 3D Memory Test structures.

Said Hamdioui received the MSEE and PhD degrees (both with honors) from the Delft University of Technology (TUDelft), Delft, The Netherlands. He is currently a Associate Professor

at the Computer Engineering Lab. of TUDelft. Prior to joining TUDelft, Hamdioui worked for Microprocessor Products Group at Intel Corporation (in Santa Clara and Folsom, Califorina), for IP and Yield Group at Philips Semiconductors R&D (Crolles, France) and for DSP design group at Philips/ NXP Semiconductors (Nijmegen, The Netherlands). He is the recipient of European Design Automation Association (EDAA) Outstanding Dissertation Award 2001, for his work on memory test techniques that have a wide-spread proliferation in the chip design industry; he is also the winner of IEEE Nano and Nano Korea award at IEEE NANO 2010—Joint Symposium with Nano Korea 2010. He was nominated for The Young Academy (DJA) of the Royal Netherlands Academy of Arts and Sciences (KNAW) in 2009. His research interests include dependable nano-computing and VLSI Design & Test (defect/fault tolerance, reliability, security, nano-architectures, Design-for-Testability, Built-In-Self-Test, 3D stacked IC test, etc). He has published one book and over 100 technical papers. He serves on the editorial board of the Journal of Electronic Testing: Theory and Applications (JETTA).

Kees Beenakker was born in Leiden in 1948. After the gymnasium he studied chemistry and physics at Leiden university. In 1971 he got his M. Sc. and joined as an Ph. D. student the FOM-Institute for Atomic and Molecular Physics in Amsterdam. After he obtained his Ph. D. in 1974 he joined Philips Research Laboratories in Eindhoven. There he was involved in various research projects related to IC technology. In 1982 he moved to the Philips Semiconductor Division in Nijmegen to become head of the corporate assembly process and equipment development. In that position first intensive contacts were established with the microelectronics industry in the Far East. In 1987 he resigned at Philips and became cofounder of Eurasem, a European hi-rel IC assembly company. In 1989 Kees Beenakker joined Dimes and is since 1990 full professor at the faculty of EEMCS (Electrical Engineering, Mathematics and Computer Science). From 1990 till 2004 he was chairman of the ECTM laboratory. In 1999 he was appointed chairman of the department of Microelectronics and Computer Engineering. He is a member of the national Medea advisory committee, member of the scientific board of the Debije Institute, the ENIAC scientific council and board member of Boschman Technologies. He is a founder of the Else Kooi Foundation, the SAFE conference, the Tsing Hua-TU Delft training centre of microelectronics technology in Beijing and the Fudan-TU Delft International school of microelectronics in Shanghai. Since March 2006 he holds a honorary guest professorship at the Tsinghua University in Beijing. In March 2007 he was appointed scientific director of DIMES, the Delft institute of microsystems and nanoelectronics. Since June 2008 he is elected chaiman of the academic council of Point-One, the national initiative on nanoelectronics and embedded systems. His specific research interests include technology for thin films and integrated circuits.

Erik Jan Marinissen is Principal Scientist at IMEC vzw in Leuven, Belgium. Previously, he worked at NXP Semiconductors and Philips Research, both in Eindhoven, The Netherlands. Marinissen holds an MSc degree in Computing Science (1990) and a PDEng degree in Software Technology (1992), both from Eindhoven University of Technology. Marinissen's research interests include all topics in the domain of test and debug of micro-electronics. He is co-author of over 150 journal and conference papers and co-inventor on eight granted US and EP patent families. Marinissen is recipient of the ITC 2008 and ITC 2010 Most Significant Paper Awards and Best Paper Awards at the Chrysler-Delco-Ford Automotive Electronics Reliability Workshop 1995 and the IEEE International Board Test Workshop 2002. He served as Editor-in-Chief of IEEE Std. 1500. He is a founder of workshops on 'Diagnostic Services in Network-on-Chips' (DSNOC), '3D Integration', and 'Testing of Three-Dimensional Stacked Integrated Circuits' (3D-TEST). He serves on numerous conference committees, including ATS, ETS, DATE, ITC, and VTS, and on the editorial boards of IEEE Design & Test of Computers, IET Computers and Digital Techniques, and Springer's Journal of Electronic Testing: Theory and Applications (JETTA). Marinissen is a Fellow of IEEE and Golden Core Member of Computer Society.