ANALYSIS OF ANALOG TO DIGITAL CONVERTER BASED ON SINGLE-ELECTRON TUNNELING TRANSISTORS

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ABSTRACT

An Analog to Digital Converter (ADC) based on single-electron tunneling transistors (SETTs) is proposed and analyzed. The novel scheme fully utilizes Coulomb oscillation effect, can properly operate at T >0K and only a capacitive divider (built with 2n-2 capacitors) and n pairs of complementary SETTs are required for an n-bit ADC implementation. Using this scheme, a 4-bit ADC is demonstrated at 10K by means of simulation.

1. INTRODUCTION

Single-electron tunneling (SET) circuits are promising for future large-scale integrated-circuits (LSIs) because they have ultra-small size and dissipate ultra-low power. Several SET circuits have been proposed in the literature, see for example [1][2][3]. However, only a few circuits fully explore the inherent SET characteristics such as Coulomb blockade and Coulomb oscillation so far, and temperature effect is usually ignored in the design. In this paper, we first analyze the complementary SET transistors (CSETTs) structure and implement a 50% duty ratio of square-wave-like output. The proposed implementation fully utilizes Coulomb oscillation effect, can properly operate at the temperature T >0K. Based on this structure, we propose a novel Analog to Digital Converter (ADC) architecture. Only a capacitive divider (built with 2n-2 capacitors) and 2n SET transistors (SETTs) are required for an n-bit ADC implementation. Using this scheme, a 4-bit ADC is demonstrated at 10K by means of simulation.

The remainder of this paper is organized as follows: Section 2 briefly describes the SETT structure and its characteristics. Section 3 analyzes the CSETTs structure, and the influence of T >0K on its behavior. Section 4 presents the novel ADC scheme, simulation results and a comparison. Finally, Section 5 concludes the paper.

2. BACKGROUND

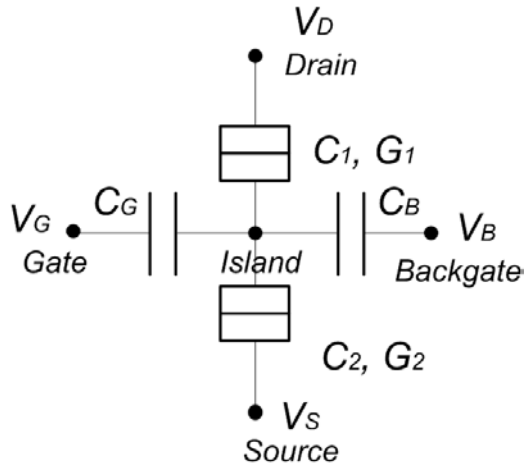

Fig. 1. Schematic of a SETT

SETT is reminiscent of a usual metallic-oxide-semiconductor field-effect-transistor (MOSFET), but with a small conducting island embedded between two tunnel junctions [2], instead of the traditional inversion channel. For the SETT in Fig.1, the tunnel conductance is G_1 and G_2, the junction capacitance is C_1 and C_2, respectively, and the gate and backgate capacitance is C_G and C_B, respectively. The drain, source, gate and backgate voltage is V_D, V_S, V_G and V_B, respectively. For the proper operation of the SETT, both G_1 and G_2 should be much smaller than $1/R_Q$, where $R_Q = h/e^2 \approx 25.8\text{k}\,\Omega$ is the quantum unit of resistance. Furthermore, we assume that the charge energy is dominant to the thermal fluctuation, that is $e^2/2C >> k_B T$, where C is the total capacitance between the island and environment and it is equal to the sum of C_1, C_2, C_G and C_B.

For 0K approximation, we can easily get the stability diagram of a SETT [2], depicted in Fig.2 (a), where $q_0 = 0$ (q_0 is the background charges in the island) and $V_B = 0$V are assumed. The diamond shadow areas are stable region, where n stands for the number of electrons present in the

island. The boundaries between stability and instability can be described by the following equations:

$$-e(n+1/2)+q_0 = C_G(V_D - V_G) + C_2 V_D + C_B(V_D - V_B) \quad (1)$$

$$e(n-1/2)-q_0 = C_G(V_G - V_D) - C_2 V_D + C_B(V_B - V_D) \quad (2)$$

$$e(n-1/2)-q_0 = C_G V_G + C_1 V_D + C_B V_B \quad (3)$$

$$-e(n+1/2)+q_0 = -C_G V_G - C_1 V_D - C_B V_B \quad (4)$$

where V_S is assumed to be zero.

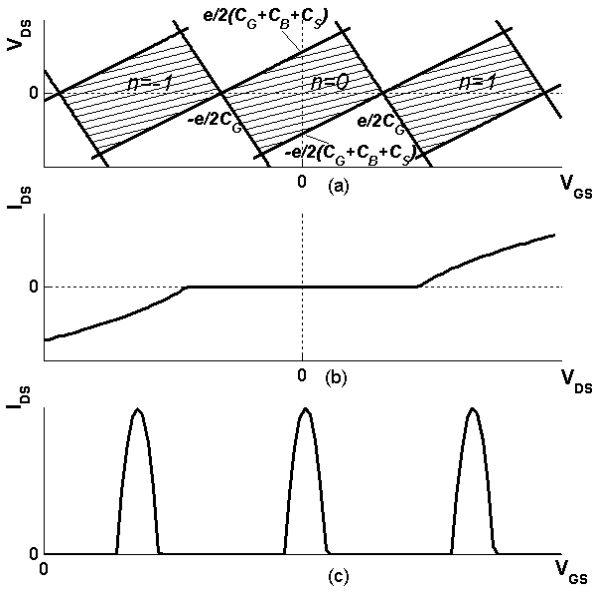

Fig. 2. (a) Stability diagram of a SETT. (b) I_{DS} -V_{DS} characteristics of a SETT. (c) I_{DS} -V_{GS} characteristics of a SETT

The I_{DS}-V_{DS}, I_{DS}-V_{GS} characteristics of a SETT are depicted Fig.2(b), Fig.2(c) respectively, where the Coulomb blockade effect is shown in Fig.2(b) and the periodic Coulomb oscillation with the period e/C_G is shown in Fig.2(c). In the next section, we utilize the Coulomb oscillation effect and propose a CSETTs structure with a square-wave-like output with 50% duty ratio.

3. ANALYSIS OF CSETTS

A complementary structure with 2 SETTs was first proposed by Tucker in [1]. This is similar to a complementary MOS (CMOS) inverter circuit in structure, and the work in [1] is focused on the inverter behavior of such a structure. This topology however can produce more than an inverter function. In this section, we explore the inherent periodic oscillation characteristic of the SETT and derive the circuit parameters corresponding to the CSETTs structure having a square-wave-like output signal with about 50% duty ratio. We achieve this mainly by modifying the backgate bias mode. In Tucker inverter, the backgate bias mode is $V_{BL} = V_D$ and $V_{BU} = 0$V. To implement CSETTs having about 50% duty ratio of square-wave-like output, we firstly analyze the CSETTs structure (see Fig.3), whose backgate bias mode is as follows: $\Delta V_B = V_{BL} - V_{BU} = e/2C_B$. V_{BU} value was chosen to adjust the initial phase of the transfer characteristic of the CSETTs. V_D value was chosen to make the upper SETT open in one half period and closed in the other half period when the V_{DS} keeps constant, and the lower SETT has a half-period phase shift of Coulomb oscillations for the backgate bias mode (see Fig.4). In this way, for the CSETTs structure, in the first half period, when $q_{out} = e$ (q_{out} is the stored charges in the output capacitor) in the initial state, the lower SETT will turn on and one electron is transported to ground and the transportation of more electrons is prohibited by the Coulomb blockade. When $q_{out} = 0$, the output will keep stable by the Coulomb blockade. In the other half period, when $q_{out} = 0$ in the initial state, the upper SETT will turn on and one electron is transported to output capacitor and the transportation of more electrons is prohibited by the Coulomb blockade. When $q_{out} = e$, the output will keep stable by the Coulomb blockade. Therefore, it is possible to get a square-wave-like output signal having about 50% duty ratio (the period is e/C_G) by using the CSETTs structure. By solving the upper SETT boundary conditions for $n = 0$, from Equations (2) and (4), we obtain,

$$V_D = \frac{C_G V_G}{C_G + C_B + C_2} + \frac{e}{2(C_G + C_B + C_2)} \quad (5)$$

$$V_D = \frac{-C_G V_G}{C_1} + \frac{e}{2C_1} \quad (6)$$

Then, to keep the upper SETT closed in one half period and open in the other half period when the V_{DS} keeps constant, V_D has to be set to,

$$V_D = \frac{C_G V_G}{C_G + C_B + C_2} + \frac{e}{2(C_G + C_B + C_2)} = \frac{-C_G(V_G + e/2C_G)}{C_1} + \frac{e}{2C_1} \quad (7)$$

By solving Equation (7), we can get

$$V_D = \frac{e}{2(C_G + C_B + C_1 + C_2)} \quad (8)$$

For the lower SETT, $V_D \approx e/C_L$, where C_L/C_1, C_L/C_2 are required to be much larger than 1. So,

$$C_L \approx e/V_D = 2(C_G + C_B + C_1 + C_2) \quad (9)$$

Then we use V_{BU} to adjust the initial phase of the CSETTs:

$$V_{BU} = -\frac{e}{2C_B} \cdot \frac{C_1}{C_G + C_B + C_1 + C_2} \quad (10)$$

$$V_{BL} = \frac{e}{2C_B} + V_{BU} \quad (11)$$

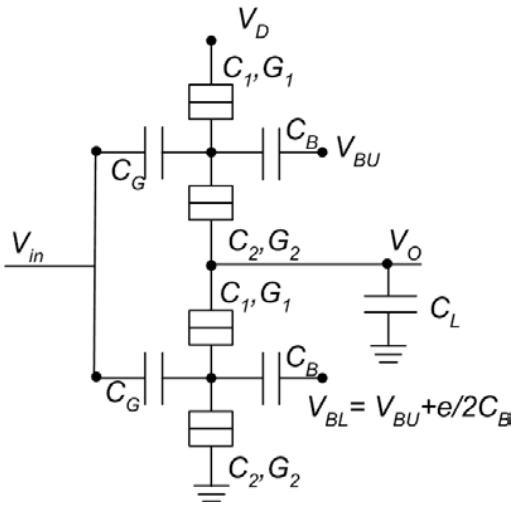

Fig. 3. Schematic of the CSETTs structure.

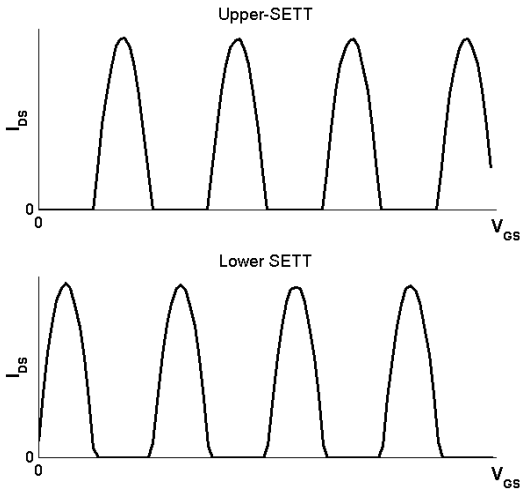

Fig.4. Separate I_{DS} –V_{GS} characteristics of the upper SETT and lower SETT of the CSETTs

According with Equations (8-11), we derived the proper parameters for a 50% CSETTs structure as follows: C_1 =C_2 =C_0, C_G =C_B =20C_0, C_0 =0.1aF, G_1 =G_2 =G_0 =1μS, V_D =$e/2(C_1+C_2+C_B+C_G)$ =0.019V, C_L =e/V_D =84C_0, V_{BU} ≈0V, and V_{BL} =V_{BU}+$e/2C_B$ ≈0.04V. We simulated the design with SIMON [2].

If T =0K, there is hysteresis of about $2V_D$ in the transfer characteristic (see Fig.5). The phenomenon can be explained as follow. For the case of T =0K, the turn-on region of the gate voltage for the upper SETT is [$e/2C_G$+V_D+ne/C_G, e/C_G+ne/C_G] when q_{out} =0 in the initial state and the turn-on region of the gate voltage for lower SETT is [ne/C_G, $e/2C_G$ -V_D+ne/C_G] when q_{out} = e in the initial state [4]. However, when the temperature increases the hysteresis range decreases, until almost vanishes (see Fig. 5). This can be explained by the fact that, when the temperature increases to a certain extent, both the upper SETT and lower SETT have no strict turn-off region or Coulomb blockade region, but have different turn-on probabilities. In the region of [$e/2C_G$+ ne/C_G, e/C_G+ne/C_G], the circuit turn-on behavior is dominated by the upper SETT for its bigger turn-on probability, so the output is high; in the region of [ne/C_G, $e/2C_G$+ne/C_G], the circuit turn-on behavior is dominated by the lower SETT for its bigger turn-on probability, so the output is low. The simulations indicate that the 50% CSETTs structure has a square-wave-like output without hysteresis from 0.5K to 20K (see Fig. 5). If the temperature increases further, the periodic oscillation becomes less sharp, but this problem can be alleviated by the addition of a comparator to the output stage.

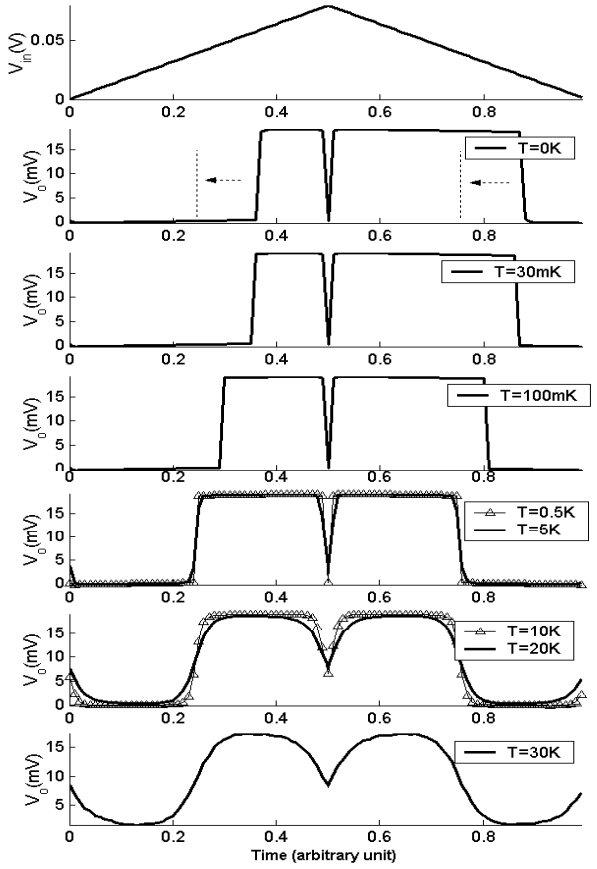

Fig. 5. Transfer characteristic of the CSETTs at T =0K, 30mK, 100mK, 0.5K, 5K, 10K, 20K, 30K.

4. SETT-BASED ADC

Based on the above CSETTs structure, we propose an *n*-bit ADC architecture as depicted in Fig. 6. It consists of a capacitive divider and *n* pairs of complementary SETTs with the same circuit parameters. In the capacitive divider, the effect of each of the input capacitance of the CSETTs can be compensated as $2C_G$ [5]. First, the input signal V_{in} is divided into $V_{in}/2^i$, i =0, 1, 2 … *n*-1, by the capacitive divider, then it is encoded into the corresponding binary output signals by the CSETTs. Using this scheme, we simulated a 4-bit ADC based on the CSETTs having the parameters in Section 3. The simulation results at T =10K are shown in Fig. 7, which clearly displays ADC behavior. The extension of the n-bit ADC design to a higher number of bits is straightforward and doesn't require redesigning the parameters of CSETTs structure and capacitive divider.

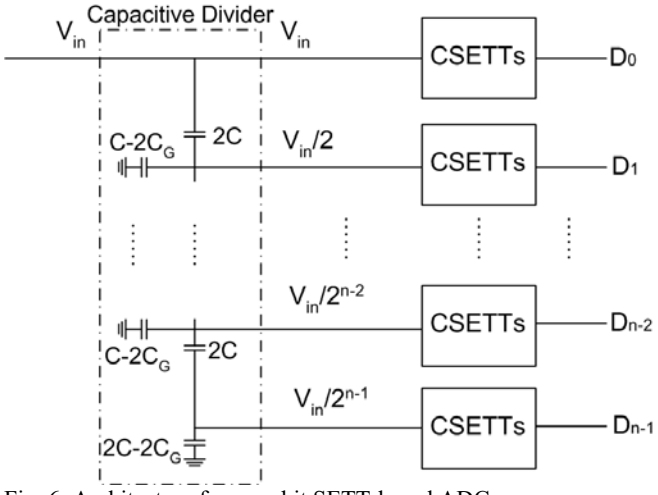

Fig. 6. Architecture for an *n*-bit SETT-based ADC

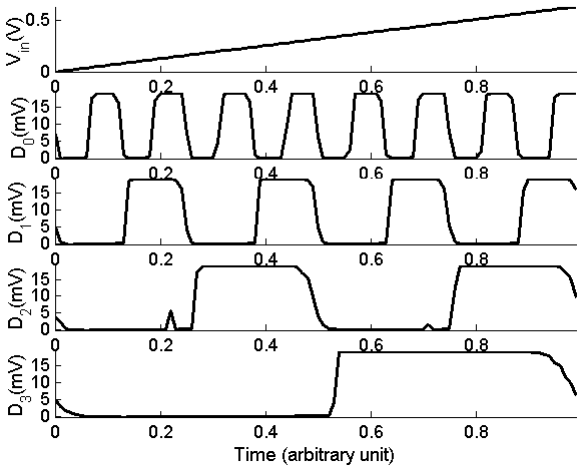

Fig. 7. Simulation results for the 4-bit SETT-based ADC at T =10K.

When compared with previous proposed SET-based ADC [6][7][8], our proposal is compact and requires less circuit elements (area). In particular, it doesn't require the sample-and-hold & discharge circuit and a sign reverser circuit like the one in [6]. Besides, no structures for coding the analog input signal into pulse-width modulation or voltage ramp circuit are necessary like the one in [7]. When compared with the ADC proposed in [8], our proposal doesn't need the quantizer. For an *n*-bit ADC, the one in [8] needs *n*+1 SETTs, 2*n*+3 MOSFETs and 2*n*-2 capacitors, whereas our proposal only needs 2*n* SETTs and 2*n*-2 capacitors. Moreover, our proposal can operate at T >0K, whereas the ones in [6][7] require 0K for the proper operation. Finally, due to a lower network depth, our proposal has a potential advantage in speed when compared with [6][7][8].

5. CONCLUSION

In summary, an ADC based on SETTs is proposed and analyzed. The novel scheme fully utilizes Coulomb oscillation effect, can properly operate at T >0K and only a capacitive divider (built with 2*n*-2 capacitors) and 2*n* SETTs are required for an *n*-bit ADC implementation. Using this scheme, a 4-bit ADC was demonstrated at 10K by means of simulation.

6. REFERENCES

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