

ReverseAge: An Online NBTI Combating Technique using Time Borrowing

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Abstract—As semiconductor manufacturing has entered into the nanoscale era, Negative Bias Temperature Instability (NBTI) has become one of the most significant aging mechanisms leading to reliability issues. This paper presents ReverseAge, a technique that detects delay due to NBTI and utilizes design timing margins to ensure reliable circuit operation. First, it presents a scheme to detect the NBTI induced delay. Second, it presents a technique to tolerate the errors; the technique exploits the available design timing margins to compensate for the NBTI induced delay. The evaluation of ReverseAge has been performed by integrating it in an ISCAS-89 benchmark circuit. The simulation results show $3\times$ reliability improvements with respect to state-of-the-art. The improvement comes at the cost of 3.77% area and 1.4% power overheads.

I. INTRODUCTION

With the relentless pursuit for smaller CMOS process technologies, timing errors due to aging mechanisms have become a limiting factor for transistor/circuit reliability [1]. Industrial data reveal that as oxide thickness reached 4nm, Negative Bias Temperature Instability (NBTI) has become one of the most significant aging mechanisms [2,3]. NBTI degrades the performance of a PMOS transistor under a negative gate stress at elevated temperature [4,5]. The effects of NBTI on a PMOS transistor include: (a) threshold voltage increment, (b) drain current degradation, and (c) delay increment [4,6]. These effects show up themselves at the circuit level by increasing circuit delays and in turn circuit timing errors.

In recent years, there is an escalation of interest in two aspects of NBTI: (a) modeling and monitoring, and (b) mitigation and design for reliability. NBTI modeling has been done both at the transistor [4,5,7,8] as well as at the circuit [6,9,10] levels. The NBTI monitoring schemes proposed so far can be classified as follows.

- **Transistor parameter monitoring:** These schemes are based on monitoring the parameters of some *selected* transistors to measure the NBTI impact on the circuit. For instance, Denias et al. in [11] monitored the transistor drain current, threshold voltage, and transconductance to quantify the impact. Kang et al. in [12] monitored the leakage current to characterize NBTI.
- **Circuit parameter monitoring:** These schemes are based on monitoring the circuit parameters to measure the NBTI impact. For instance, Kim et al. in [13] monitored

the beat frequency of two ring oscillators (which is a special structure used on the chip), one stressed and the other unstressed, to characterize the impact. Agarwal et al. in [14] monitored NBTI using a stability checker circuit. Keane et al. in [15] characterized NBTI in terms of the control voltage of the two delay locked loops.

Although all the above proposed schemes measure NBTI impact, they require significant area overhead and/or do not give realistic measure of NBTI impact. For example, transistor parameters monitoring schemes [11,12] require enormous area overhead when it is applied to a larger group of PMOS transistors that degrade at different rates. Similarly, the circuit parameter monitoring schemes [13,15–17] are not realistic because the monitoring circuits are activated for a *selected* period of time. *Therefore, a scheme that incurs lower area overhead and realistically measure NBTI impact on the circuit is required; this is one of the topics addressed in this paper.*

Apart from NBTI monitoring, researchers have focused on NBTI mitigation and design for reliability techniques. Research has been conducted to tolerate NBTI impacts at transistor/circuit levels [4,9,18]. The techniques proposed so far can be classified as:

- **Pre-manufacturing techniques:** These techniques are based on the process optimization or design optimization. Scarpa et al. in [19] suggested several process optimization techniques (e.g. oxide nitridation, adding fluorine to gate oxide etc.) and Islam et al. in [18] proposed a uniaxial strained silicon transistor (with SiGe source/drain and contact etch stop layer) to mitigate NBTI degradation. Similarly, Paul et al. in [9] suggested 8.7% gate oversizing at the design stage to mitigate NBTI.
- **Post-manufacturing techniques:** These techniques are based on the contents flipping, input vectors control and parameters tuning. Kumar et al. in [20] proposed a technique to flip the contents of SRAM cells to mitigate the NBTI impact. Wang et al. in [21] proposed a technique to control the input vectors of a node during its standby mode to reduce the probability of stress and hence NBTI. Wang et al. in [10] suggested a set of techniques including: V_{th} tuning, V_{dd} tuning and temperature reduction to compensate for the NBTI impacts.

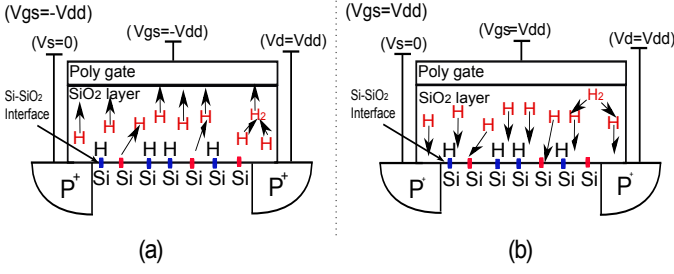


Fig. 1. Schematic view of (a) Si-H bond breaking, H and H₂ diffusions toward poly gate and their interconversion at Si/SiO₂ interface and inside oxide dielectric under negative gate stress (b) H and H₂ diffusions toward the Si-SiO₂ interface and ≡Si- bond recovery under positive gate stress

Although the above proposed techniques are able to mitigate NBTI impacts at transistor/circuit levels, all of them imply overheads in term of process steps/area/power/time or design complexity. For example, process optimization adds expensive process steps. Gate oversizing adds a significant area and power overheads. Input vector control comes with a significant design complexity. Finally, parameter tuning demands complex power grid. *Therefore, a technique that does not add significant overheads, yet utilize the timing margins of the circuit to tolerate NBTI is needed, as proposed in this paper.*

This paper addresses the two shortcomings in NBTI research mentioned above and proposes ReverseAge; a technique to monitor and tolerate NBTI in the circuits. The idea of ReverseAge is motivated from the distribution of NBTI induced timing errors in the circuits and the available timing margins. From NBTI induced timing errors point of view, it is found that at a given time, the error spans only a single stage of the circuit. The successive stages suffer from lower additional delays and timing margins are available. Therefore, the error in a stage is tolerated it by borrowing time from the successive stages. Simulation results of the ReverseAge show 3× reliability improvements with respect to the state-of-the-art. The improvement comes at the cost of 3.77% area and 1.4% power overheads.

The rest of the paper is organized as follows. Section II presents gate level NBTI analysis. Section III presents motivation for ReverseAge. Section IV presents the ReverseAge architecture. Section V presents simulation results and their analysis. Finally, Section VI concludes the paper.

II. GATE LEVEL NBTI ANALYSIS

NBTI is characterized by the threshold voltage increment of the PMOS transistor under the negative gate stress. NBTI originates from Silicon Hydrogen bonds (≡Si-H) breaking that occur at Silicon-Silicon dioxide (Si-SiO₂) interface as shown in Fig. 1(a). The broken Silicon bonds (≡Si-) act as interface traps at the Si-SiO₂ interface and the H atoms/molecules diffuse toward the poly gate. The *number of interface traps* (N_{IT}) depends on ≡Si-H bond breaking rate (k_f) and ≡Si-bond recovery rate (k_r).

In recent times, exhaustive efforts have been put to understand NBTI at the device level [4,5,7]. Kackzer et al. in [7] have analyzed NBTI at the device level reasonably well but

have not extended their analysis to deal with NBTI at a higher level. Alam et al. in [4] have modeled NBTI at the device level and presented the overall dynamics of NBTI as a reaction diffusion process. The model is usable at a higher level such as circuit level. Since in this work, NBTI analysis is done at the circuit level, model of [4] will be used that relates N_{IT} with time (t) as follows:

$$N_{IT}(t) = \left(\frac{k_f N_o}{k_r} \right)^{2/3} \left(\frac{k_H}{k_{H_2}} \right)^{1/3} (6D_{H_2}t)^{1/6}, \quad (1)$$

where N_o , k_H , k_{H_2} , and D_{H_2} represent initial bond density, H to H₂ conversion rate, H₂ to H conversion rate, and H₂ diffusion rate inside SiO₂ layer, respectively.

Interface traps are assumed to be positive charges remaining at the Si-SiO₂ interface that oppose the applied gate stress resulting in the threshold voltage increment (ΔV_{th}). The relation between N_{IT} and ΔV_{th} is given by [9]:

$$\Delta V_{th} = (1 + m)qN_{IT}/C_{ox}, \quad (2)$$

where m , q , and C_{ox} are the holes mobility degradation that contribute to the V_{th} increment [6], electron charge, and oxide capacitance, respectively. On the other hand, NBTI annealing takes place under the positive gate stress; in this case, the H atoms anneal back towards the Si-SiO₂ interface as shown in Fig. 1(b). The H atoms/molecules anneal the ≡Si- bonds at Si-SiO₂ interface resulting in lower N_{IT} and hence lower ΔV_{th} .

The NBTI induced ΔV_{th} of PMOS transistors causes additional gate delay which is given by [9]:

$$\Delta D = \gamma \cdot \frac{n \cdot \Delta V_{th}}{(V_{gs} - V_{th})} \quad (3)$$

where n is the velocity saturation index and γ represents the distribution of stress and recovery -negative and positive gate stresses- durations. The γ dependence of the additional delay reveals that transistors in circuit having different stress/recovery duration will suffer from different delays, resulting in the circuit delay variation.

A simple CMOS inverter was synthesized using 45nm Predictive Technology Model (PTM) transistor models [30] and simulated using HSPICE for 10 years operation. To focus on NBTI, it is assumed that process variations and the other failure mechanisms, e.g. Hot Carrier Degradation, Electro-migrations and Time Dependent Dielectric Breakdown are not affecting the inverter. Throughout the simulation, $\gamma=50\%$ and NBTI parameters used to get ΔV_{th} are, $k_f=8 \times 10^{-4} s^{-1}$, $k_r=3 \times 10^{-18} cm^3 s^{-1}$, $N_o=5 \times 10^{16} cm^{-2}$, $D_{H_2}=4 \times 10^{-21} cm^2 s^{-1}$ and $T=125^\circ C$ [8]. Fig. 2(a) gives the ΔV_{th} increment of PMOS transistor due to NBTI; it shows that ΔV_{th} approaches 47.81mV after 10 years of operation. The curve follows 1/6 trend and have a good match with the experimental results presented in [3]. Fig. 2(b) shows ΔD i.e. the percentage increment of the inverter delay that approaches 12.37%. Paul et al. in [9] has suggested the same ΔD trend due to NBTI for the other gates of a circuit.

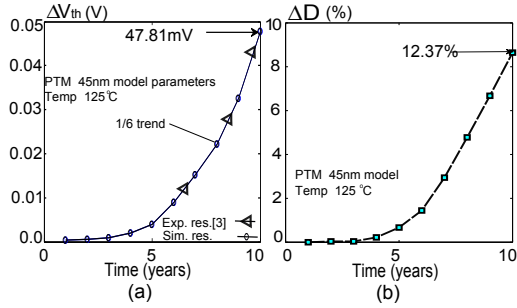


Fig. 2. (a) NBTI induced (ΔV_{th}) increment of a PMOS transistor as a function of time (b) Inverter delay ΔD increment as function of time

III. REVERSEAGE MOTIVATION

This section analyzes the distribution of NBTI impact in a circuit and explores the available timing margins of the circuits for tolerating NBTI. Usually in circuits there are a number of combinational logic clusters (CLCs) along with the sequential elements (e.g. FF's). Fig. 3 presents a conceptual representation of a synthetic circuit with four stages (i.e. four CLC's and five FF's); the circuit is sufficient enough to illustrate the distribution of NBTI and the available timing margins. All CLC's are customized such that they have nearly the same critical path delay just like an industrial design that balance all the stages as close as possible to reduce power and area of the design.

First, simulation has been done to explore NBTI induced delay distribution. Fig. 4 summarizes the delay distribution of the four stages. Three input sets -set1, set2, and set3- are considered. Each set of the four bars for each input set represents NBTI induced delay in the four stages. The figure shows that the input signals which causes enough delay in one stage of the circuit produce far less delays in the neighboring stages. For example, the input -set3- causes 19.09% additional delay in stage C1355 while it produce only 13.88% delay in stage C1908.

Second, the maximum allowable delay of a stage is defined for the expected worst operating conditions (e.g. high temperature and voltage droop) [25]. However, under normal operating conditions the parameter is unnecessarily strict and the setup margin (discussed in the next section) available will never be used [27]. The margin can be used to tolerate delays due to aging or process variations. The black portion of each bar in Fig. 4 represents the available margin in each stage under the given input set. For example, stage C1908 suffers from only 19.74% delay under input -set2- and have about 1.35% setup margin available -with respect to the worst effected stage C880- for the preceding stages. The setup margin can be used by the

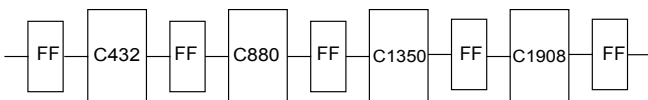


Fig. 3. Schematics of a synthetic pipeline circuit with ISCAS-85 circuits and flip flop.

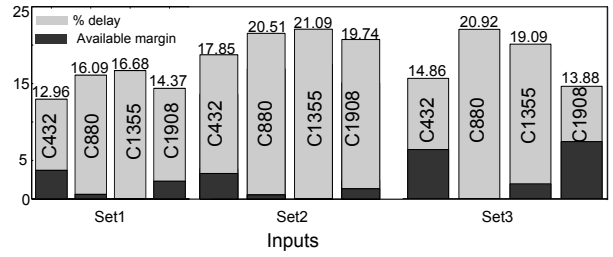


Fig. 4. NBTI induced delay distribution among four stages of the circuit

preceding stage without causing any error in the circuit.

To summarize the distribution of NBTI and the available timing margin, it is argued that NBTI in a stage can be tolerated by borrowing time from the succeeding stage. The time borrowing will not affect timings of the next stage (details will be discussed in the next section). However, if NBTI causes timing errors in multiple adjacent stages then the time borrowing from the next stage will not be effective and may cause timing error. Under such conditions the timing error is tolerated by dynamically adjusting the clock frequency at system level [25].

IV. REVERSEAGE: ARCHITECTURE

This section describes an NBTI monitoring scheme along with a tolerating technique. The monitoring scheme detects the NBTI induced delay and produces an error signal. Circuitry of the error tolerance responds to the error signal and borrows time from the succeeding stage. After lending time to preceding stage, the succeeding stage operates in its own timing limits.

A. NBTI Monitoring

Fig. 5 shows an example circuit to illustrate the NBTI monitoring concept. The monitor is augmented to the flip-flop (FF) that is connected to the combinational logic cluster (CLC) output (C_{out}) as shown in Fig. 5(a). Without considering NBTI, C_{out} approaches FF2 well before its setup margin that results in sensor output is *low* as shown in Fig. 5(b). However, with NBTI, delay of the CLC increases significantly and C_{out} creep into the setup margin. It is important to not that the FF2 will still capture correct value at rising edge of the clock (due to the available setup needed). However, the monitor predicts the setup time violation and produce an error signal as shown

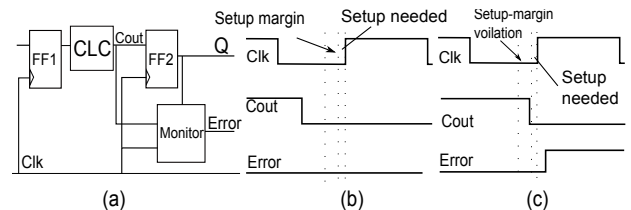


Fig. 5. NBTI monitoring circuit (a) High level view of NBTI monitor, (b) Signal wave forms without NBTI in the CLC (c) Signal wave forms with NBTI in the CLC

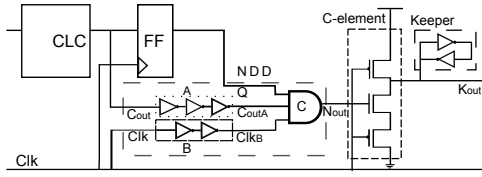


Fig. 6. Schematics of NBTI monitoring circuit with NBTI Delay Detector (NDD), C-element and the Keeper circuit

in Fig. 5(c). The scheme predicts- NBTI in the circuit and has lower overhead as compared to Razor [28] and Canary logic [16] that has shadow FF and canary FF augmented to the normal FF, respectively.

Fig. 6 shows the implementation and Fig. 7 shows signal waveforms at the internal nodes of the monitor. The monitor consists of an NBTI Delay Detector (NDD), a C-element, and a keeper circuit. NDD detects the NBTI in the CLC in a transient form, C-element sensitizes the transient and then the keeper circuit converts it to a stable signal. The NDD design is simple that consists of two delay elements (A and B) and a three inputs AND gate (C). The CLC output (C_{out}) and Clk are inputs to the delay elements A and B, respectively. Without considering NBTI in the CLC, C_{out} arrives earlier than the clock (Clk) edge and FF output (Q). Element A delays and inverts C_{out} (C_{outA}) while B delays the Clk ($ClkB$) such that $ClkB$ goes low before C_{outA} and Q goes high, as a result output of the gate C remains *low* as shown in Fig. 7(a). However, by considering NBTI in the CLC, the output C_{out} will be delayed and there will be an interval when all the three inputs (C_{outA} , $ClkB$ and Q) of the AND gate are *high* that results in *high* output N_{out} as shown in Fig. 7(b).

The NDD output signal N_{out} is high for a small duration, a transient with a width equivalent to the NBTI induced delay in the CLC. The output of NDD may or may not activate the NBTI tolerating circuitry (discussed in the next subsection). The C-element and the keeper circuit shown in Fig. 6 are similar to the one presented [27]. The C-element senses transient output of the sensor during low as well as high clock cycles. Sensitivity of the C-element is adjusted so that it is turned on by NBTI induced delays and have a very

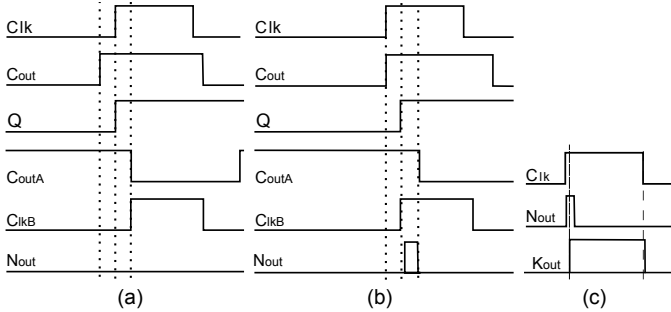


Fig. 7. Signal waveforms of the NBTI monitor for (a) NDD without considering NBTI in CLC, (b) NDD with considering NBTI in CLC, (c) C-element and Keeper circuit

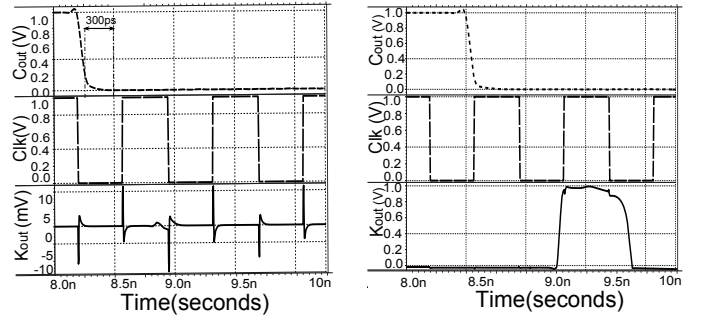


Fig. 8. Simulation waveforms of the NBTI monitor (a) without considering NBTI in CLC, (b) with considering NBTI in CLC

small response time. Fig. 7(c) shows that N_{outA} arrives the C-element at the beginning of the clock high. Output of the C-element is input to the keeper circuit of Fig. 6. The keeper circuit comprises cross-coupled inverters that are turned on by the momentary *on* state of the C-element and maintains a stable output (K_{out}) signal.

The monitor design is verified using HSPICE simulation. An inverter chain that act as CLC, FF's and the monitor circuit are synthesized using 45nm PTM transistor models [30]. Transistors in the monitor are optimally sized to have smaller response time (40ps). Fig. 8 shows the CLC output (C_{out}), Clk and the monitor output (K_{out}) signals. The figure shows that without considering NBTI in the CLC, the C_{out} approaches well before the Clk (about 300psec). Under this condition C_{out} is beyond the FF setup margin as a result the monitor output remains *low*. However, by considering NBTI and after 10 years of operation, C_{out} and Clk approaches the monitor/FF nearly at the same time (with only 29psec time difference). The monitor sensitizes the setup time violation of the FF and produce a *high* K_{out} signal.

B. NBTI Tolerance

Once the NBTI induced delay is detected by the monitor circuit, the next step is to tolerate it by utilizing design timing margin of the circuit. In ReverseAge, first the possibility of utilizing time margin of flip flops in succeeding or preceding stages of the circuit is explored and then a technique to tolerate NBTI is proposed.

Delay of a stage is determined by delays of the CLC and adjacent FF's. To be in timing limits delays of the CLC and FF should be less than clock period and the input signal must pass through the stage in one cycle. Fig. 9(a) shows a stage delay with the maximum allowable delays in the CLC and FF of the stage. The figure shows that delay in the CLC is limited by hold and setup times constraints of the the adjacent FF's.

Relaxing either the hold time of the preceding FF or setup time of the succeeding FF increases the maximum allowed delay to the CLC. However, relaxing the hold time of the preceding FF requires complex clocking schemes and implies significant performance loss [27]. Therefore, the delay portion of the CLC is increased by relaxing the setup time of the succeeding FF i.e. shifting the rising edge later as shown in

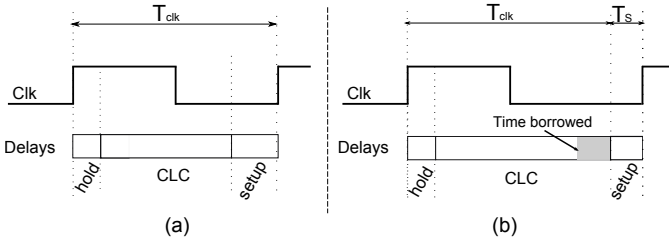


Fig. 9. A stage delay with (a) maximum allowable delay of the CLC and FF, (b) Time stealing by a CLC using setup margin of FF in the next stage

Fig. 9(b). The time (T_s) represented by the shaded block is the *time borrowed* from the succeeding stage and is achieved by shifting (i.e. delaying) the clock rising edge into the FF of the next stage.

Implementation of the time borrowing concept is simple that augments a Specialized Clcking Scheme (SCS) to the Flip-Flop as shown in Fig.10(a). FF has the conventional master and slave latches. However, the master latch has clock input from the SCS. Fig. 10(b) illustrates schematics of the SCS. In the given figure, when the monitor output K_{out} -of the previous stage monitor- is low, the PMOS transistor turns on to select Clk as SClk to the master latch of Fig. 10(a). However, at the high K_{out} at the monitor output, the NMOS transistor turns on and DCIk is the input to the master. DCIk is in same phase with Clk however delayed by a duration approximately equivalent to the setup margin of the flip flop.

Timing stealing in the is implemented by augmenting SCS's to the FF's to the circuit of NBTI monitoring. Fig. 11(a) shows that in absence of NBTI in the preceding CLC, with the low monitor output, SCIk to the FF is same as Clk. The circuit behave in a normal manner, i.e. master and slave latch data on positive and negative edges of the clock, respectively. In presence of NBTI in the preceding CLC, K_{out} becomes high and SCIk rising edge the FF is is delayed as shown in Fig. 11(b). Delaying the clock to master latch allows more time for signal to pass through the CLC. However, impact of the technique does not propagate to the succeeding stages, because output of the FF appears on falling edge to the slave latch that have the normal timings.

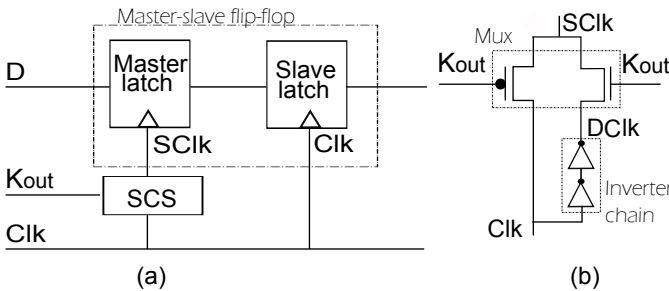


Fig. 10. Schematic of Time stealing technique: (a) Master slave flip flop with a Specialized Clcking Scheme, (b) Specialized Clcking Scheme for the master latch

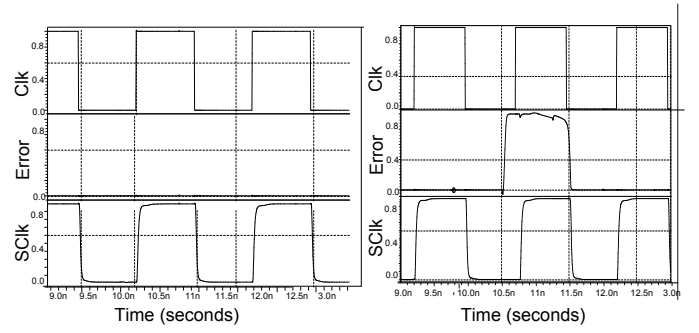


Fig. 11. Signal waveforms of the time borrowing: (a) Clock to the master latch without error indication of monitor, (b) Clock to the master latch with error indication of monitor

V. CASE STUDY AND ANALYSIS

A five stage 4×4 add shift multiplier circuit (S349 in ISCAS-89 benchmarks) is taken as a case study to illustrate effectiveness of ReverseAge technique. Predictive Technology Model (PTM) cards of 45nm technology nodes are used to synthesize the circuit. The clock (Clk) used is 10ns ($Clk=0.1GHz$) with 50% duty cycle. NBTI induced delay degradation is injected into the circuit by using a Verilog-A module under the conditions ($V_{DD}=1.0V$ and $T=125^\circ C$). First, the circuit is simulated for 10 years operation to get temporal degradation due to NBTI degradation. The simulation identified five critical flip-flops among the total 15 FF's of the circuit. Thereafter, proposed elements -monitor and tolerating circuitry- of the ReverseAge are integrated into the benchmark.

Effectiveness of the ReverseAge along with the area and power overheads are discussed below.

ReverseAge Effectiveness

The effectiveness of ReverseAge is illustrated by varying the NBTI induced delay in the CLC and observing the error signal in the monitors attached to the critical FF's of the circuit. The monitor outputs are used to define failure probability of the technique. For comparison the simulations are carried out under four different cases:

- V_{dd} reduction: as suggested in [10]
- Temperature reduction: as suggested in [10]
- Gate Oversizing: as suggested in [12]
- Time borrowing: as proposed in this paper

Fig.12 shows a comparison of the failure probability observed under the four considered cases. The figure shows that ReverseAge ensures $4.5 \times$ more reliability as compared to temperature tuning proposed in [10] and $3.0 \times$ lower failure probability than transistor sizing suggested by [12]. This means that the ReverseAge improves NBTI tolerance in the circuit by $3 \times$ with respect to the state-of-the-art. This improvement proves the effectiveness of the proposed ReverseAge technique.

ReverseAge Overhead

Overheads of the ReverseAge includes area and power consumed by the monitor and tolerance circuit. The area

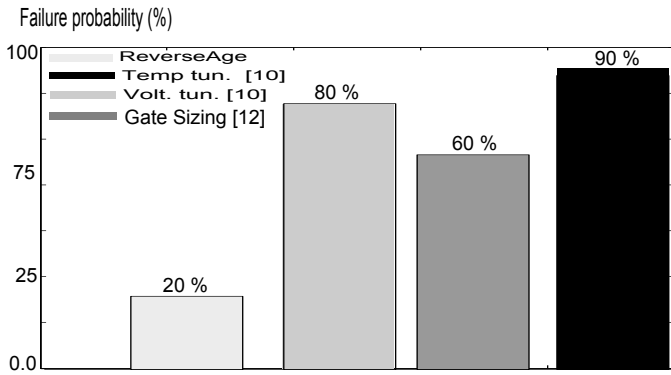


Fig. 12. Comparison of ReverseAge with other state-of-the-art NBTI tolerating techniques

overhead is obtained in percent i.e. the area of the added monitor and tolerance circuit with respect to the original circuit. Fig. 13(a) shows percent the area overhead for multiple monitors in the circuit. Fig. 13 shows that the ReverseAge adds only 3.77% area overhead in comparison to the 8.7% overhead proposed in [12]. Similarly, the power overhead of ReverAge is only 1.8% and is very low in comparison to the power consumed by the NBTI mitigating techniques proposed in [12,21].

VI. CONCLUSION

This paper presented ReverseAge, an online technique to tolerate NBTI induced delays by utilizing design time margin. ReverseAge proposes an NBTI monitoring scheme along with a technique to tolerate NBTI induced delay. The monitor detects NBTI induced delay and generate a timing error signal. Thereafter, the timing error of the stage is tolerated by borrowing time from the successive stages. Simulation result from benchmark circuit shows that ReverseAge ensures 3× reliability improvement at the cost of 3.77% area and 1.4% power overheads.

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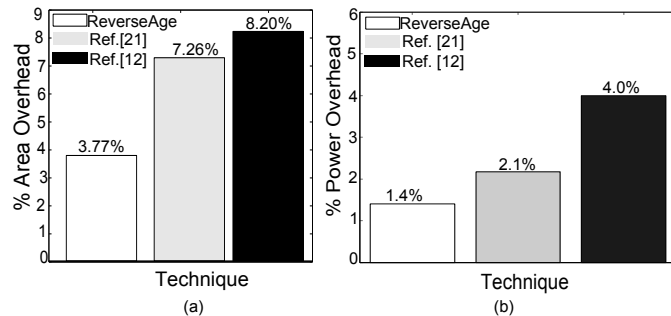


Fig. 13. Area and power overheads comparisons of the ReverseAge with other NBTI monitoring and tolerating approaches

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