Effects of Bit Line Coupling on the Faulty Behavior of DRAMs

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Abstract: *With the shrinking dimensions of manufactured structures on memory chips and the increase in memory size, bit line coupling is becoming ever more influential on the memory behavior. This paper discusses the effects of bit line coupling on the faulty behavior of DRAMs. It starts with an analytical evaluation of coupling effects, followed by a simulation-based fault analysis using a Spice simulation model. Two bit line coupling mechanisms are identified, pre-sense and post-sense coupling, and found to have a partly opposing effect on the faulty behavior. In addition, the impact of neighboring cells on these coupling mechanisms is investigated.*

Keywords: *DRAMs, bit line coupling, faulty behavior, data backgrounds, Spice simulation.*

1 Introduction

The long, narrow bit line (BL) structures running in parallel on the surface of a memory chip are particularly prone to relatively large amounts of capacitive coupling (or crosstalk) noise from adjacent BLs. As the integration density of memory devices increases, the problems associated with BL coupling noise become more significant because of the weak cell signals that must be sensed reliably on these lines [Redeker02].

The issue of crosstalk in logic circuits has received much attention and was investigated in depth in the literature [Deutsch01]. There is also some research on BL coupling in memory devices that investigates its effect on memory operations in current and future fabrication technologies [Redeker02]. However, there is no published work of the impact of BL coupling noise on memory faults, nor of the way neighboring cells influence the faulty behavior for a specific victim cell.

This paper investigates the impact of BL coupling on the faulty behavior of DRAMs. We start with a theoretical analysis and then employ simulation-based fault analysis techniques of a defective Spice simulation model to evaluate the behavior. Two BL coupling effects are identified and the way a neighborhood of cells influences BL coupling is investigated.

This paper begins with a description of the Spice simulation model in Section 2. Section 3 gives a theoretical analysis of BL coupling on the faulty behavior. Section 4 introduces the fault analysis method used to evaluate the faulty behavior. Then, Section 5 discusses the simulation-based fault analysis results of BL coupling. Finally, Section 6 ends with the conclusions.

2 Spice simulation model

The simulation model used in this paper is based on a design-validation model of an actual DRAM produced by Infineon Technologies. In order to limit the needed simulation time, the model has been reduced in complexity, while electrically compensating removed components.

Figure 1 shows a block diagram of the folded BL pair to be simulated. This simplified simulation model contains a 2×2 cell array with nMOS access transistors, in addition to a sense amplifier and precharge devices. The removed memory cells are compensated for by load cells and parasitic components of different values distributed along the BLs. External to the BL pair, the simulation model contains one data output buffer needed to examine data on the output, and a write driver needed to perform write operations. The memory model employs Spice BSIM3v3 device parameters for the simulations.

The model contains three BL pairs, denoted as BLt for top, BLm for middle, and BLb for bottom, as shown in Figure 2. Figure 1 shows both the true (BTm) and complementary (BCm) bit lines of BLm, only the complementary (BCt) bit line of BLt, and only the true (BTb) bit line of BLb.

The different BLs influence each other by a number of distributed coupling capacitances ($C_{bb1} + C_{bb2} + C_{bb3} = C_{bb}$). Note that BL coupling capacitances are the same whether coupling takes place within a given BL pair or between different BL pairs. This is true since all BLs on a chip are manufactured in the same way, using the same

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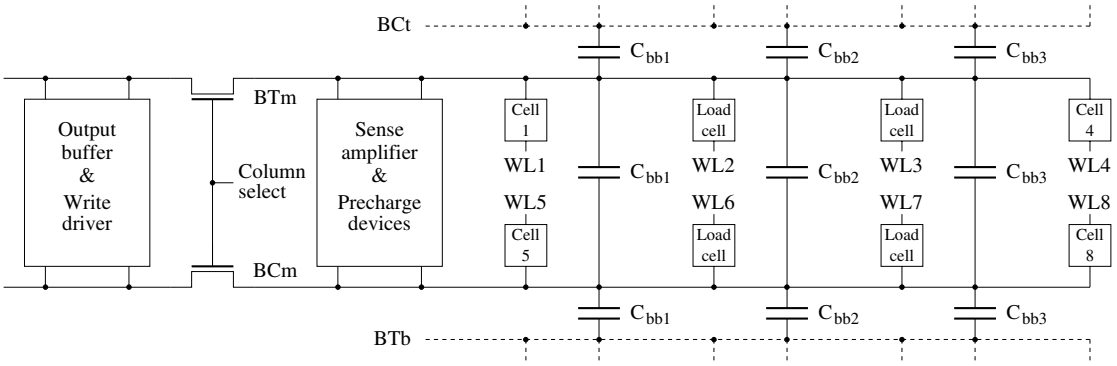

Figure 1. Block diagram of the BL pair used for simulation.

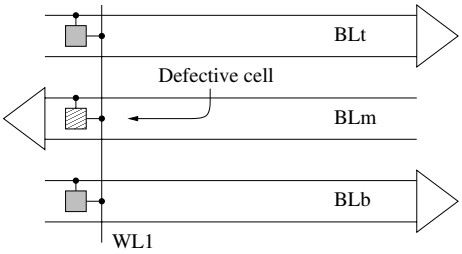

Figure 2. Three BL pairs implemented in the simulation model.

materials, having the same dimensions, and at the same distances from each other. Identifying a given BL as BT or BC depends solely on the way that BL is connected to the sense amplifier and not on the way it is manufactured.

The total BL capacitance (C_b) is made up of the sum of the BL coupling capacitance (C_{bb}), and the remaining capacitance (C_{br}) not related to BL coupling, but to word line (WL) coupling, substrate coupling, etc. In the simulation model of Figure 1, these capacitances are related as follows:

$$C_b = C_{bb} + C_{br} = 10 \times C_{bb} \tag{1}$$

These are typical cell array capacitances in Megabit DRAMs with a folded BL pair arrangement [Konishi89, Itoh01]. As a result of C_{bb}, two different kinds of coupling effects may take place: *pre-sense coupling* and *post-sense coupling* [Aoki88].

Pre-sense coupling (ΔV_1) is generated after the WL is activated and cells are accessed, but before the sense amplifier is activated. The noise on a given floating BL results from coupling to two BLs, above and below the victim BL, on which cells are accessed. The amount of coupling noise depends on the background data stored in the accessed cells. The worst case background here is when both neighboring cells contain the same data (either both 1 or both 0)[1]. The amount of worst case ΔV_1 developing on the floating BL relative to the full voltage V_1 developing on neighboring BLs can be approximated as [Hidaka89]:

$$\frac{\Delta V_1}{V_1} \approx \frac{1}{2 + (C_{br}/C_{bb})} \tag{2}$$

This relation indicates that the amount of pre-sense coupling noise increases with increasing C_{bb} from 0 V for $C_{bb} = 0$ to $\frac{1}{2}$ as C_{bb} approaches ∞. For the used simulation parameters in (1), the worst case $\frac{\Delta V_1}{V_1} \approx \frac{1}{11}$.

Post-sense coupling (ΔV_2) is generated after the sense amplifier is activated and the BLs are pulled either to 0 or 1 according to the logic value sensed by the sense amplifier. The main reason for this type of noise is the time difference between sense amplifier activation and the instant the sense amplifier decides to sense a 1 or 0 (Δt). The amount of ΔV_2 can be approximated according to the following relation [Aoki88]:

$$\Delta V_2 \approx \alpha \frac{C_{bb}}{C_b^2} (\Delta t)^3 \tag{3}$$

Where α is a constant that depends on a number of sense amplifier related parameters and has a value in the order of $10^{12} \sim 10^{13} \frac{\mathrm{FV}}{\mathrm{s}^3}$. The relation shows the strong dependence of ΔV_2 on the time delay until the sense amplifier pulls the BLs either up or down. This means that even small delays in the sense amplifier operation can cause a relatively large amount of post-sense coupling noise.

The total amount of BL coupling noise ΔV is equal to the sum of pre-sense and post-sense coupling ($\Delta V_1 + \Delta V_2$). Whether ΔV_1 or ΔV_2 constitutes the dominant factor in ΔV depends heavily on design specific parameters that generally cannot be evaluated analytically, which leaves circuit simulation as the only analysis option [Itoh01].

[1] This worst case background induces the largest amount of BL coupling noise, but it is not the worst case background for the faulty behavior of a victim cell, as discussed later in Section 3

3 Effects of coupling

BL coupling results in developing small coupling voltages on adjacent BLs, which influences proper sense amplifier operation. From a testing point of view, it is important to understand how a specific initialization of a neighborhood of cells affects the sensing of a given victim, so that the worst case values can be written in the neighboring cells.

The model considered here [see Figure 2] consists of 3 BL pairs, each with 2×2 cells, which means that the defective cell (Cell 1 on BLm) has a neighborhood of 3×2×2 = 12 cells with a possible influence on the behavior. But since the precharge operation functions properly (because cell opens do not influence the precharge voltage on the BLs), the history of operations performed on any cell other than the defective cell does not influence the faulty behavior of the memory[2]. Therefore, the only cells able to influence the faulty behavior are those sharing the same WL with the defective cell. This means that the neighborhood consists of two cells, each containing either 0 or 1, which results in $2^2 = 4$ different data backgrounds.

The effects of BL coupling on the faulty behavior can be divided into pre-sensing effects, and post-sensing effects. Figure 3 gives graphical representations for both cases, when Cell 1 on BTt contains a logic 1 and Cell 1 on BTb contains a logic1.

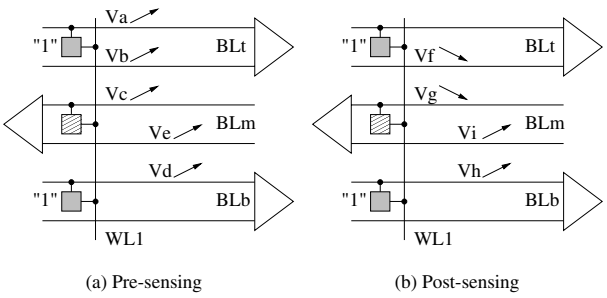

Figure 3. Effects of (a) pre-sense and (b) post-sense coupling.

Pre-sensing effects. As soon as WL1 is accessed, Cell 1 on BTt starts to pull the voltage on BTt by an amount of V_a to a higher level; this is indicated by the up-arrow next to V_a in the figure. As a result of C_{bb}, the voltage on BCt is also pulled by an amount of V_b to higher level; this is indicated by the up-arrow next to V_b in the figure. Finally, as a result of C_{bb} between BCt and BTm, the voltage on BTm is pulled higher by an amount of V_c, which promotes sensing a *logic 1* in the victim; this is indicated by the up-arrow next to V_c in the figure[3]. From Equations (1) and (2), the amount V_c is related to V_a by the relation $\frac{V_c}{V_a} = \frac{V_b}{V_a}\frac{V_c}{V_b} \approx \frac{1}{11^2}$. In the same way, as soon as WL1 is accessed, Cell 1 on BTb starts to pull the voltage on BTb by an amount of V_d to a higher level, which in turn pulls the voltage on BCm by an amount of V_e higher. This increase in the voltage on BCm promotes sensing a *logic 0* in the victim cell. The values of V_d and V_e are related by $\frac{V_e}{V_d} \approx \frac{1}{11}$, which means that the cell on BTb has a much higher influence on the faulty behavior than the cell on BTt. In conclusion:

1. The worst case pre-sensing background for a cell with an open defect which has a stored value x is $\bar{x}x$ (i.e., Cell 1 on BTt contains $\bar{x}$ and Cell 1 on BTb contains x).

2. Cell 1 on BTb has a much higher pre-sensing influence (first-order effect) on the faulty behavior than Cell 1 on BTt (second-order effect).

Post-sensing effects. Once the sense amplifier is activated, and since Cell 1 on BTt contains 1, the sense amplifier pulls the voltage on BTt high while the voltage on BCt is pulled low by an amount of V_f [see Figure 3(b)]. As a result of C_{bb}, the voltage on BTm is pulled low by an amount of V_g, which promotes sensing a logic 0 in the victim cell. In a similar way, once the sense amplifier is activated, and since Cell 1 on BTb contains a 1, the sense amplifier pulls the voltage on BTb high by an amount of V_h as indicated in Figure 3. As a result of C_{bb}, the voltage on BCm is also pulled high by an amount of V_i, which promotes sensing a logic 0 in the victim cell. Both neighboring cells have a first-order effect on the victim. In conclusion:

1. The worst case post-sensing background for a cell with an open defect which has a stored value x is xx (i.e., Cell 1 on BTt contains x and Cell 1 on BTb contains x).

2. Both cells have a comparable first-order effect on the faulty behavior.

Comparing the two results of pre and post-sensing, we find that each requires a different background to ensure the worst case sensing condition. It is possible to use a memory test that covers both backgrounds to ensure covering the worst case condition. But to reduce test time, a single worst case background is needed, and therefore we should identify whether pre-sensing or post-sensing is more dominant.

[2] On the other hand, a defective precharge circuitry would mean that the read/write history affects the faulty behavior and should be simulated

[3] The increase in the voltage on BTm further results in an increase in the voltage on BCm, but this effect is an order of magnitude less and is therefore negligible

4 Fault analysis method

This section describes the method to be used for analyzing a cell defect in a DRAM [Al-Ars02]. The analysis performed here corresponds to BLs with *no* coupling. This means that the coupling capacitances shown in Figure 1 are all set to zero: $C_{bb1} = C_{bb2} = C_{bb3} = 0$

Consider the defective DRAM cell shown in Figure 4, where a resistive open (R_{op}) between BT (true bit line) and the access transistor limits the ability to control and observe the voltage across the cell capacitor (V_c). The open is injected into Cell 1 and simulated as part of the reduced memory model shown in Figure 1. The reasons for choosing this specific cell defect to analyze BL coupling include the following.

1. This defect models a strap connection between the drain of the pass transistor and the cell capacitor that is difficult to manufacture and may have resistive values that are higher than normal [Adler95].

2. Gradually increasing the resistive value of this defect results in the gradual reduction of the differential BL signal needed for proper sensing. Therefore, this defect is ideal for analyzing the impact of BL coupling on the faulty behavior.

3. The relative simplicity of the defect model and the required fault analysis.

The analysis takes a range of possible open resistances (10 kΩ $\leq$ R_{op} $\leq$ 10 MΩ) and a range of possible cell voltages (GND $\leq$ V_c $\leq$ V_{dd}) into consideration.

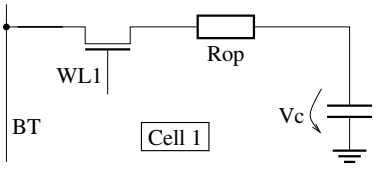

Figure 4. Open injected into Cell 1.

Two different (V_c, R_{op}) result planes are generated, one for the $w0$ operation on a cell initialized to one ($1w0$) and one for the $w1$ operation on a cell initialized to 0 ($0w1$). These result planes describe the impact of successive $w0$ and successive $w1$ operations on V_c (denoted as $(n)w0$ and $(n)w1$, respectively), for a given value of R_{op}. Write operations described here refer to single-cycle operations, where a cell is accessed, written, then disconnected, and followed by a memory precharge. Figure 5 shows an automatically generated result plane corresponding to $(n)w0$ operations, while Figure 6 shows the result plane corresponding to $(n)w1$ operations, for the open R_{op} shown in Figure 4.

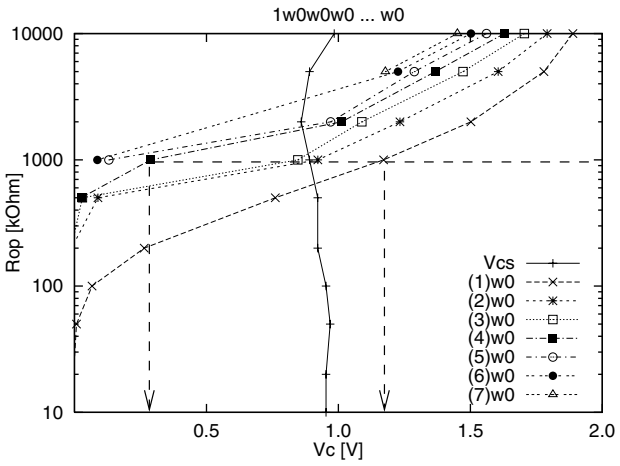

Figure 5. Result plane corresponding to $w0$.

Plane of $w0$: This result plane is shown in Figure 5. To generate this figure, the floating cell voltage V_c is initialized to V_{dd} (because a $w0$ operation is performed) and then the operation sequence $1w0w0...w0$ is applied to the cell (i.e., a sequence of $w1$ operations to a cell initialized to 1). The net result of this sequence is the gradual decrease (depending on the value of R_{op}) of V_c towards GND. The voltage level after each $w0$ operation is recorded on the result plane, resulting in a number of curves. The curves are numbered as $(n)w0$, where n is the number of $w0$ operations needed to get to the curve. For example, the arrows in the figure indicate that, for R_{op} = 1000 kΩ, a single $w0$ operation represented by $(1)w0$ pulls V_c from $V_{\rm dd}$ to about 1.2 V, while four $w0$ operations represented by $(4)w0$ pull V_c to about 0.3 V. We stop performing the $w0$ sequence when the voltage change ΔV_c, as a result of $w0$ operations, becomes $\Delta V_c \leq$ 0.05 V, which results in identifying up to 7 different $w0$ curves in the plane. Initially, an arbitrary small value for ΔV_c is selected, which can be reduced afterwards if it turns out that more than 7 $w0$ operations are needed to describe the faulty behavior. The *sense threshold cell voltage (V_{cs})*, shown as a solid line that runs across the center of the figure, is the cell voltage *above* which the sense amplifier reads a 1, and *below* which the sense amplifier reads a 0. This curve is generated by performing a read operation for a number of V_c values and iteratively identifying the V_c border that distinguishes a 1 and a 0 on the output. V_{cs} is almost independent of R_{op} here because there is no BL coupling considered in

this simulation since all BL coupling capacitances are set to zero ($C_{bb1} = C_{bb2} = C_{bb3} = 0$). The small deviation V_{cs} has from the center of the figure is due to sense amplifier imbalance and other types of coupling, such as WL-BL coupling.

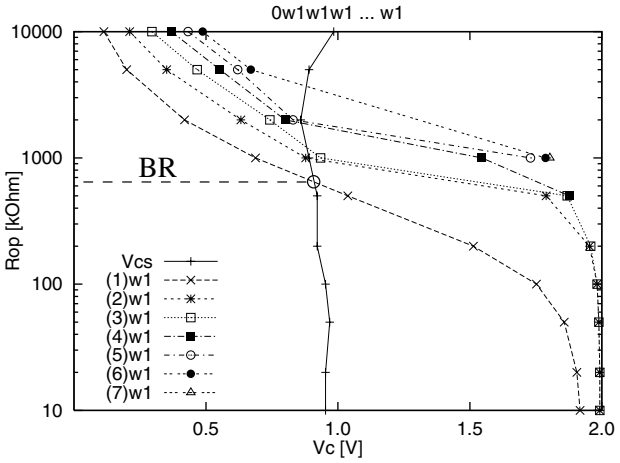

Figure 6. Result plane corresponding to $w1$.

Plane of $w1$: This result plane is shown in Figure 6. This result plane is generated in the same way as the result plane of $w0$. First, V_c is initialized to GND and then the operation sequence $0w1w1...w1$ is applied to the cell. The result is a gradual increase of V_c towards V_{dd}. The voltage level after each $w1$ operation is recorded on the result plane, which gives a number of curves in the plane. We stop the $w1$ sequence when ΔV_c becomes small enough (0.05 V in this example). V_{cs} is also shown in the figure as a solid line.

It is possible to use the result planes to analyze a number of important aspects of the faulty behavior such as: the resistive value of the defect where the memory starts to fail, and the test needed to detect the faulty behavior resulting from the open defect [Al-Ars02].

5 Simulation results

This section presents the simulation results of the effects of BL coupling on the faulty behavior of the memory model shown in Figure 1, having the cell open shown in Figure 4. The analysis method used here is the same as that outlined in Section 4. Four different simulations are performed, one for each data background (BG): BG 00 (both cells are 0), BG 01 (cell on BTt is 0 and on BTb is 1), BG 10 (cell on BTt is 1 and on BTb is 0) and BG 11 (both cells are 1).

The analysis results show that the write curves are very similar in all BGs, and are also similar to the $(n)w0$ curves shown in in Figure 5 and the $(n)w1$ curves shown in Figure 6. Therefore, they are not significantly influenced by BL coupling, and are not discussed further.

The effects of BL coupling on the faulty behavior are evident in the way the V_{cs} curve is influenced. This is expected since the V_{cs} curve is closely associated with the amount of differential voltage developing on a given BL pair. Figure 7 shows four different V_{cs} curves for the simulated BGs, plus the one resulting in the case of zero coupling (no coup.) [see Figure 5].

The figure shows that for a victim with a stored 0, the worst case coupling is generated with BG 10, then with BG 00, followed by the case with no coupling, then BG 11 and finally BG 01. For a victim with a stored 1, the worst case coupling is generated with BG 01, then BG 11, no coupling, BG 00, and finally BG 10. This means that the worst case condition for a victim containing value x corresponds to BG $\bar{x}x$. Comparing these results with the theoretical analysis of Section 3 indicates that the dominant BL coupling effect in the simulations of Figure 7 is pre-sense coupling.

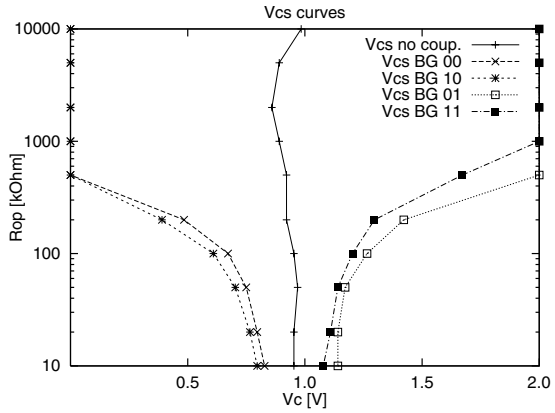

Figure 7. Different V_{cs} curves showing effects of BL coupling.

The figure also shows that the most influential cell on the behavior is the one on BTb, which is expected since it generates cooperating pre-sense and post-sense coupling effects. The cell on BTt has a limited impact on the behavior since it generates opposing pre-sense and post-sense coupling effects. It is interesting to note that, for a given victim value, some BGs actually *help* the faulty behavior to produce the correct read output, which indicates the importance of selecting the worst case background values.

In order to check the correct correspondence between simulation results and the theoretical analysis of Section 3, one could ask the question: Is it possible to modify the sim-

ulation model in such a way that would make post-sensing more dominant than pre-sensing?

Referring to (2) and (3), ΔV_1 and ΔV_2 are related as follows:

$$\frac{\Delta V_1}{\Delta V_2} \sim \frac{(C_{br} + C_{bb})^2}{C_{br} + 2C_{bb}} \quad (4)$$

where we consider Δt as a constant. This relationship indicates that in order to increase the relative impact of ΔV_2 compared to ΔV_1, the ratio in (4) should be reduced, which in turn can be done by reducing C_{br}. Figure 8 shows four new V_{cs} curves corresponding to a modified simulation model with $C_{br2} = \frac{C_{br}}{2}$. The figure shows that for a victim containing a 0, the worst case condition is ensured by BG 00, then BG 10, BG 11, and finally BG 01. On the other hand, the worst case condition for a cells containing a 1 is ensured with BG 01, then BG 11, BG 10, and finally BG 00. This represents a mixed behavior where the post-sensing effects are dominant when sensing a 0 in the victim, while pre-sensing effects are dominant when sensing a 1 in the victim [see Section 3]. Reducing C_{br} further did not change this mixed behavior.

It is worth noting that post-sensing effects are also able to dominate both sensing a 0 and a 1 in the victim, since this behavior has been observed in another simulation model for a different DRAM fabrication technology. In conclusion, depending on the specific memory design and fabrication technology, either pre-sensing or post-sensing effects (or both) may dominate the resulting faulty behavior. This, in turn, means that unless an analysis is done to identify the exact coupling effects for a specific memory, then all possible worst case data backgrounds have to be considered during testing.

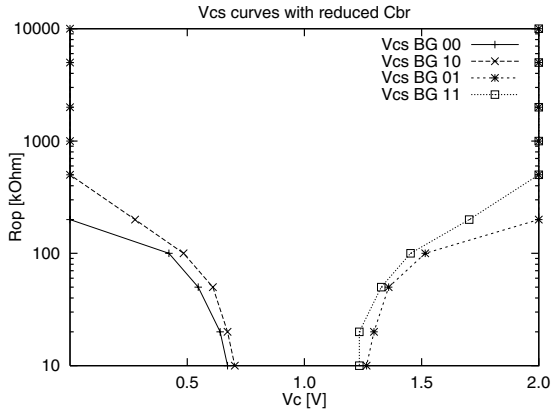

Figure 8. Different V_{cs} curves showing effects of BL coupling.

6 Conclusions

This paper analyzed the effects of bit line coupling on the faulty behavior of DRAMs. Two different coupling mechanisms were identified, pre-sense and post-sense coupling, and the effects of both were analyzed, first using the capacitive coupling equations, and then using a Spice memory simulation model. The results show that the two coupling mechanisms have a partly opposing effect on the faulty behavior, something that is important to take into consideration when designing DRAM tests. In addition, the impact of neighboring cells on the coupling mechanisms was investigated, and the corresponding worst case backgrounds were given. The fact that different worst case backgrounds exists indicates that, unless the coupling behavior of the memory is known, multiple data backgrounds are needed to ensure the worst case test conditions. This may explain why the same test if applied with different data backgrounds results in a different fault coverage.

References

[Adler95] E. Adler *et al.*, "The Evolution of IBM CMOS DRAM Technology," *in IBM J. of Research and Development*, vol. 39, no. 1–2, 1995, pp. 167–188.

[Al-Ars02] Z. Al-Ars and A.J. van de Goor, "Approximating Infinite Dynamic Behavior for DRAM Cell Defects," *in Proc. IEEE VLSI Test Symp.*, 2002, pp. 401–406.

[Aoki88] M. Aoki *et al.*, "A 60-ns 16-Mbit CMOS DRAM with a transposed data-line structure," *in IEEE J. Solid-State Circuits*, vol. 23, no. 5, 1988, pp. 1113–1119.

[Deutsch01] A. Deutsch *et al.*, "On-Chip Wiring Design Challenges for Gigahertz Operation," *in Proc. IEEE*, vol. 89, no. 4, 2001, pp. 529–555.

[Hidaka89] H. Hidaka *et al.*, "Twisted Bit-Line Architectures for Multi-Megabit DRAMs," *in IEEE J. Solid-State Circuits*, vol. 24, no. 1, 1989, pp. 21–27.

[Itoh01] K. Itoh, *VLSI Memory Chip Design*, Springer-Verlag, Berlin, Germany, 2001.

[Konishi89] Y. Konishi *et al.*, "Analysis of Coupling Noise between Adjacent Bit Lines in Megabit DRAMs," *in IEEE J. Solid-State Circuits*, vol. 24, no. 1, 1989, pp. 35–42.

[Redeker02] M. Redeker, B.F. Cockburn and D.G. Elliott, "An Investigation into Crosstalk Noise in DRAM Structures," *in Proc. IEEE Int'l Workshop Memory Technology, Design and Testing*, 2002, pp. 123–129.