Evaluation for Intra-Word Faults in Word-Oriented RAMs

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Abstract

This paper presents an industrial evaluation of tests for intra-word faults in word oriented memories, applied to big arrays with bit-interleaved organization as well as to small arrays with bit-adjacent organization, in order to investigate the influence of the memory organization on the intra-word faults. The test results show that the intra-word faults are also significantly important for interleaved memories, even though that the cells within a single word are not physically adjacent.

1 Introduction

Random access memories can be organized as *bit-oriented* memories (BOMs) or as *word-oriented* memories (WOMs). WOMs contain more then one bit per word; i.e., $B > 2$, where B represents the number of bits per word, and usually is a power of 2. Traditionally, WOMs have been tested by repeated application of BOM tests [3, 11, 12, 14, 16], where different data backgrounds are used during each iteration. The disadvantages of this methodology are test time inefficiency and limited fault coverage of coupling faults between cells within the same word, which are called *intra-word coupling faults*.

In our previous work [6], all possible *intra-word coupling faults* has been presented. The *data-background sequences* required for the detection of each of these faults have been established, and compiled into six tests detecting the targeted faults. This paper presents the result of an experiment evaluating such six tests together with a set of well known tests. It is organized as follows: Section 2 gives briefly the six new tests introduced in [6] to cover all intra-word coupling faults. Section 3 describes the used stress combinations and tests during the test experiment. Section 4 presents the test results; Section 5 ends with conclusions.

2 Tests for intra-word faults

Fault models for WOMs can be divided into the *single-cell* faults and *faults between memory cells (i.e., coupling faults (CFs))*. In addition faults between cells can be further divided, based on the location of the *aggressor cell (a-cell)* and the *victim cell (v-cell)*, into:

1. **Inter-word coupling faults**: These are faults where the a-cell and the v-cell belong to *different* words.
2. **Intra-word coupling faults**: These are faults where the a-cell and the v-cell belong to the *same* word.

Testing of single-cell and inter-word coupling faults can be done using BOM tests. Therefore, the BOM tests can be converted into WOM tests by replacing the single bit operations with a B-bit wide *data-background (DB)*. However, the detection of intra-word coupling faults cannot be guaranteed with BOM tests [6, 12, 14].

In [6], all possible intra-word coupling faults have been presented. The DBs required for the detection of each of these faults have been established, and compiled into six tests detecting the targeted faults. These consist of the following tests:

1. Test CFds to detect intra-word *disturb* CF.
2. Test CFtr to detect intra-word *transition* CF.
3. Test CFwd to detect intra-word *write disturb* CF.
4. Test CFdr to detect intra-word *deceptive read destructive* CF.
5. March SAM detecting all possible intra-word CF.
6. March SAMopt: an optimized version of March SAM assuming that intra-word CFs can only occur between physically adjacent cells within a single word.

In addition, it has been shown in [6], that any test detecting one of the above intra-word CFs also detects intra-word *state* CF, *incorrect read* CF, and *read destructive* CF. Table 1 gives the intra-word tests for $B = 2$; the way to extend such tests for any B is given in [6].

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Table 1. Intra-word tests for B=2

Test	Description
Test CFds	$\{\Updownarrow(w00); \Updownarrow(w11, r11, w11, r11, r11, w00, r00, w00, r00, r00);$ $\Updownarrow(w01); \Updownarrow(w10, r10, w10, r10, r10, w01, r01, w01, r01, r01)\}$
Test CFdr	$\{\Updownarrow(w00); \Updownarrow(w11, r11, r11, w00, r00, r00); \Updownarrow(w10, r10, r10, w01, r01, r01)\}$
Test CFwd	$\{\Updownarrow(w00); \Updownarrow(w11, w11, r11, w00, w00, r00); \Updownarrow(w10, w10, r10, w01, w01, r01)\}$
Test CFtr	$\{\Updownarrow(w00); \Updownarrow(w01, r01, w11, r11, w10, r10, w00, r00); \Updownarrow(w10, r10, w11, r11, w01, r01, w00, r00)\}$
March SAM	$\{\Updownarrow(w00); \Updownarrow(w01, r01, w01, r01, r01, w11, r11, w11, r11, r11);$ $\Updownarrow(w10, r10, w10, r10, r10, w00, r00, w00, r00, r00); \Updownarrow(w10, r10, w11, r11, w01, r01, w00, r00)\}$

3 Used tests and stresses

This section gives the used tests and stresses during the experiment. The used tests consist of *Inter-Word* base tests (i.e., test algorithms) and *Intra-Word* base tests.

3.1 Inter-word base tests (Inter-BTs)

The Inter-BTs consist of the known industrial memory test algorithms; the tests are listed in Table 2. For Hammer, the notation e.g., $10{*}w1$ means that the 'write 1' operation is performed 10 times successively to the same cell. For GalRow and GalColumn, the notation e.g., $row(r0, r1_b)$ means apply 'read 0' ($r0$) operation in an incrementing order to the cells of the row of the base cell, and apply 'read 1' ($r1$) operation to the base cell after each $r0$ operation; a similar explanation applies to $col(r0, r1_b)$. Similarly, for WalkRow and WalkColumn, the notation e.g., $row(r0)$ ($col(r0)$) means apply a $r0$ operation using an incrementing address order to the row (column) of the base cell, and skip the base cell.

The inter-word base tests has been applied using different *stress combinations (SCs)*. Two types of stresses have been used; namely *addressing* and *data-background* stresses. The used addressing stresses consist of two types of addressing:

1. **Fast X (fx)**: Fast X addressing is simply incrementing or decrementing the address in such a way that each step goes to the next row.
2. **Fast Y (fy)**: Fast Y addressing is simply incrementing or decrementing the address in such a way that each step goes to the next column.

A *data-background (DB)* is the pattern of ones and zeros as seen in an array of memory cells. The most common types of data-background are four:

1. Solid (s): All 0s, all 1s.
2. Checkerboard (c): 0101.../ 1010.../0101.../ 1010...
3. Column strip (cs): 0101.../ 0101.../0101.../ 01010...
4. Row strip (rs): 0000.../ 1111.../ 0000.../ 1111...

3.2 Intra-word base tests (Intra-BTs)

The Intra-BTs consist of the six new tests introduced in our previous work [6], namely: Test CFds, Test CFdr, Test CFtr, Test CFwd, March SAM and its optimized version (March SAMopt). In addition, and in order to have a reference for the comparison within intra-word tests, Intra-word MATS+ (denoted Intra-Mats+) will be used; it is the same as MATS+ except that the test is repeated with 1+$\lfloor log_2 B \rfloor$ different DBs; where B is the word size. For example for B=4, the DBs will be: 0000, 0101, 1100. Table 3 gives the list of the used intra-word BTs together with the required number of operations [6]. To find the test length of each BT, the required number of operations has to be multiplied with $\frac{n}{B}$, where n is the size of the memory array. The intra-word BTs of Table 3, which use predefined DBs, has been applied using the two addressing types: Fast X and Fast Y.

Table 3. List of used Intra-word BTs

#	Test	# of operations
1	Test CFds	10+11$*\lfloor log_2 B \rfloor$
2	Test CFdr	6+6$*\lfloor log_2 B \rfloor$
3	Test CFtr	16* $\lfloor \log_2 B \rfloor$
4	Test CFwd	6+6$*\lfloor log_2 B \rfloor$
5	March SAM	28*$\lfloor log_2 B \rfloor$)
6	March SAMopt	28
7	Intra-Mats+	5+5*$\lfloor log_2 B \rfloor$

4 Test results

This section gives the test results for caches with big size as well as with small size, followed with the discussion and the comparison of the results.

4.1 Test results for big arrays

In the experiment done at Intel, a set of more than 70 tests was used. A *test* consists of a *base test (BT)* (i.e., test algorithm) applied using a particular *stress combination (SC)*. A SC consists of a combination of values of different *stresses*; e.g., addressing, data-backgrounds, etc.

All tests were applied to embedded caches with a size of 1MByte, which have an *interleaved* bit-organization; the testing has been performed at high voltage and high speed. From a huge number of tested chips, 344 chips failed all SCs, while 33569 chips failed only some SCs. We will concentrate on the 33569 chips since they are the most important.

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Table 2. List of the used Inter-word Base Tests (Inter-BTs)

#	BT name	Description
1	SCAN [1]	$\{\Uparrow (w0); \Uparrow (r0); \Uparrow (w1); \Uparrow (r0)\}$
2	MATS+ [9]	$\{\Updownarrow (w0); \Uparrow (r0, w1); \Downarrow (r1, w0)\}$
3	MATS++ [2]	$\{\Updownarrow (w0); \Uparrow (r0, w1); \Downarrow (r1, w0, r0)\}$
4	March C- [8, 13]	$\{\Updownarrow (w0); \Uparrow (r0, w1); \Uparrow (r1, w0); \Downarrow (r0, w1); \Downarrow (r1, w0); \Updownarrow (r0)\}$
5	PMOVI [4]	$\{\Downarrow (w0); \Uparrow (r0, w1, r1); \Uparrow (r1, w0, r0); \Downarrow (r0, w1, r1); \Downarrow (r1, w0, r0)\}$
6	March SR [7]	$\{\Downarrow (w0); \Uparrow (r0, w1, r1, w0); \Uparrow (r0, r0); \Uparrow (w1); \Downarrow (r1, w0, r0, w1); \Downarrow (r1, r1)\}$
7	March SS [7]	$\{\Updownarrow (w0); \Uparrow (r0, r0, w0, r0, w1); \Uparrow (r1, r1, w1, r1, w0); \Downarrow (r0, r0, w0, r0, w1); \Downarrow (r1, r1, w1, r1, w0); \Updownarrow (r0)\}$
8	March G [10]	$\{\Updownarrow (w0); \Uparrow (r0, w1, r1, w0, r0, w1); \Uparrow (r1, w0, w1); \Downarrow (r1, w0, w1, w0); \Downarrow (r0, w1, w0); \Uparrow (r0, w1, r1); \Uparrow (r1, w0, r0)\}$
9	March RAW [5]	$\{\Updownarrow (w0); \Uparrow (r0, w0, r0, r0, w1, r1); \Uparrow (r1, w1, r1, r1, w0, r0); \Downarrow (r0, w0, r0, r0, w1, r1); \Downarrow (r1, w1, r1, r1, w0, r0); \Updownarrow (r0)\}$
10	Hammer [15]	$\{\Uparrow (w0); \Uparrow (r0, 10 * w1, r1); \Uparrow (r1, 10 * w0, r0); \Downarrow (r0, 10 * w1, r1); \Downarrow (r1, 10 * w0, r0)\}$
11	GalColumn [2]	$\{\Uparrow (w0); \Uparrow_b (w1_b, col(r0, r1_b), w0_b); \Uparrow (w1); \Uparrow_b (w0_b, col(r1, r0_b), w1_b)\}$
12	GalRow [2]	$\{\Uparrow (w0); \Uparrow_b (w1_b, row(r0, r1_b), w0_b); \Uparrow (w1); \Uparrow_b (w0_b, row(r1, r0_b), w1_b)\}$
13	WalkColumn [2]	$\{\Uparrow (w0); \Uparrow_b (w1_b, col(r0), r1_b, w0_b); \Uparrow (w1); \Uparrow_b (w0_b, col(r1), r1_b, w0_b)\}$
14	WalkRow [2]	$\{\Uparrow (w0); \Uparrow_b (w1_b, row(r0), r1_b, w0_b); \Uparrow (w1); \Uparrow_b (w0_b, row(r1), r1_b, w0_b)\}$

Table 4. The union and the intersection of Intra-BTs for big arrays (total FC=559)

#	BT Name	SC	FC	UFs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	Test CFdr	fx	239	0	**239**	288	347	337	307	315	270	266	289	305	376	–	347	–
2	Test CFdr	fy	217	0	168	**217**	324	314	291	296	246	245	264	275	355	–	324	–
3	Test CFds	fx	281	0	173	174	**281**	339	344	355	305	303	313	330	375	–	364	–
4	Test CFds	fy	271	1	173	174	213	**271**	334	343	287	290	305	313	362	–	349	–
5	Test CFtr	fx	218	0	150	144	155	155	**218**	282	235	240	281	300	361	–	313	–
6	Test CFtr	fy	231	0	155	152	157	159	167	**231**	251	244	292	307	368	–	319	–
7	Test CFwd	fx	132	1	101	103	108	116	115	112	**132**	155	230	251	336	–	250	–
8	Test CFwd	fy	127	0	100	99	105	108	105	114	104	**127**	226	247	329	–	247	–
9	March SAMopt	fx	194	0	144	147	162	160	131	133	96	95	**194**	257	338	–	297	–
10	March SAMopt	fy	215	0	149	157	166	173	133	139	96	95	152	**215**	345	–	314	–
11	March SAM	fx	312	1	175	174	218	221	169	175	108	110	168	182	**312**	–	383	–
12	March SAM	fy	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
13	Intra-Mats+	fx	212	1	104	105	129	134	117	124	94	92	109	113	141	–	**212**	–
14	Intra-Mats+	fy	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Figure 1 shows the *Venn-diagram* of the *fault coverage (FC)* of the Inter-BTs as compared with the FC and Intra-BTs. Apparently 33010 out of 33569 faults are detected with Inter-BTs; 31241 faults are detected with Inter-BTs *only*. On the other hand, 2328 faults are detected with Intra-BTs; 559 faults are detected with Intra-BTs *only*. Note that 1769 faults are detected with both Inter-BTs and Intra-BTs.

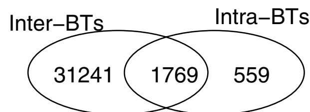

Figure 1. The FC of the used BTs for big arrays

Based on the Venn-diagram, one can conclude that the percentage of detected faults with Inter-BTs is very high as compared with those detected with Intra-BTs. Further, the percentage of faults detected with Intra-BTs *only* (i.e., 559/33569=1.67%) cannot be ignored. Therefore intra-word faults have to be taken into consideration or leave a substantial number of faults undetected. Considering a high volume production and the low DPM level driven by the market requirements, the percentage of such (intra-)word faults (e.g., 1.67% in our case) can translate in high DPM level ending up in selling defective chips to the customers.

Analysis of intra-word specific BTs

This section compares the six new intra-word tests (introduced in [6]) with each others, including Intra-Mats+. Our analysis will be focused only on faults detected with the intra-BTs only (i.e., the 559 faulty chips); see Figure 1.

Table 4 shows the *union* and the *intersections* of the Intra-BTs. A die belongs to the union of two BTs if at least one of the two BTs found the die to be faulty, and belongs to the intersection of two BTs if *both* BTs found the die to be faulty. The first column in the table gives the BT number; the second column the name of the BT. The column 'SC' gives the addressing the BT is used with; note that each BT is applied with fx and fy addressing[1]. The column 'FC' lists the fault coverage of the corresponding BT; the column 'UFs' gives number of *unique faults (UFs)* each BT detects. Unique faults are faults that are *only* detected once with a single test.

The union and the intersection of each pair of BTs is shown in the rest of the table. The numbers on the diagonal give the FC of the BTs, which are also listed in the column 'FC'. The part above the main diagonal shows the union for each BT pair, while the part under the diagonal lists the in-

[1] Except fy for March SAM and Intra-Mats+; these tests were unfortunately incorrectly implemented

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tersection of each BT pair; e.g., the union of Test CFdr-fx (i.e., using fx) and March SAMopt-fx is 289 and their intersection is 144. Based on the test result data-base, Table 4 and the Venn-diagram of Figure 1, we conclude that:

- The total number of faulty chips detected with all Intra-BTs is 2328 (see Figure 1); i.e., 6.93% of the total 33569 faulty chips.
- The total number of faulty chips detected with Intra-BTs *only* is 559; i.e., 1.67% of the total 33569 faulty chips; see Figure 1. 558 of such 559 faults are detected with the six *new* introduced Intra-BTs only (i.e., Test 1 through test 6 in Table 3) as Figure 2 shows.

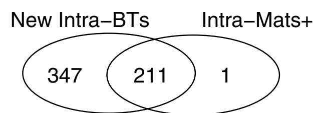

Figure 2. The FC of the Intra-BTs for big arrays

- The total number of faulty chips detected with the *new* introduced Intra-BTs *only* is 347 (see Figure 2); i.e.:
  - 62.20% of the 559 faulty chips detected with Intra-BTs *only* ; see Figure 2.
  - 14.90% of the of the total of 2328 faulty chips detected with *all* Intra-BTs;
  - 1.03% of the total 33569 faulty chips detected with all used tests (i.e., Inter-BTs and Intra-BTs).
- The best three intra-word BTs in terms of FC are: March SAM-fx with FC=312, Test CFds-fx with FC= 281, and Test CFds-fy with FC= 271.
- The best union pair in terms of the FC is 383, achieved with Intra-Mats+ using fx and March SAM-fx. However, all detected faults by intra-Mats+ are detected with the new introduced Intra-BTs except one fault, as Figure 2 shows.
- There are four UFs detected by four tests; see column 'UFs' in Table 4.
- An analysis (not shown here) reveals that in order to achieve the same FC as that achieved with all used Intra-BTs, only the following Intra-BTs are required: Test CFds-fx, Test CFwd-fx, March SAM-fx, and Intra-Mats+ using fx. These tests are the tests detecting UFs; see Table 4.
- A test with the lowest FC is Test CFwd with FC=132 for fx and FC=127 for fy.
- None of the Intra-BTs detects supersets of faults of other Intra-BTs.

4.2 Test results for small arrays

A similar experiment has been done for small arrays with a size of 25 KBytes, and with an *adjacent* bit-organization. The same tests at the same test conditions (i.e., high voltage and high speed) as for big arrays have been applied. From a huge number of tested chips (which is *1.5 times more* than the number of big array chips tested in the previous experiment), 2490 chips failed all SCs, while 6039 chips failed only some SCs. We will concentrate on the 6039 chips since they are the most important.

Figure 3 shows the Venn-diagram of the FC of the Inter-BTs as compared with the FC and Intra-BTs. Apparently 5982 out of 6039 faults are detected with Inter-BTs; 475 faults can be detected with Inter-BTs *only*, while 57 faults are detected with Intra-BTs *only*

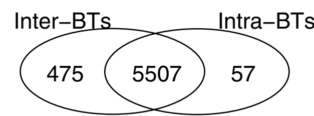

Figure 3. The FC of the BTs for small arrays

Based on the Venn-diagram one can conclude that the percentage of the faults detected with Intra-BTs *only* is very small (about 0.94%) as compared with those detected with Inter-BTs (about 99.06%).

Analysis of intra-word specific BTs

Table 5 shows the *union* and the *intersections* of the Intra-BTs. The table focuses only on faults detected with the intra-BTs (i.e., the 57 faulty chips; see Figure 3). The representation used in Table 5 is similar to that used in Table 4. Based on the test result data-base, Table 5 and the Venn-diagram of Figure 3, we conclude the following:

- The total number of faulty chips detected with all Intra-BTs is 5564 (see Figure 3); i.e., 92.13% of the total 6039 faulty chips.
- The total number of faulty chips detected with Intra-BTs *only* is 57; i.e., 0.94% of the total 6039 faulty chips (see Figure 3). 53 of such 57 faults are detected with the *new* introduced Intra-BTs (Test 1 through test 6 in Table 3) as Figure 4 shows.

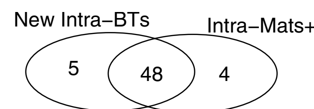

Figure 4. The Intra-BTs FC for small arrays

- The total number of faulty chips detected with the *new* introduced Intra-BTs *only* is 4 (see Figure 4); i.e.:
  - 7.01% of the 57 faulty chips detected with Intra-BTs *only* ; see Figure 4.

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Table 5. The union and the intersection of Intra-BTs for small arrays (total FC=57)

#	BT Name	SC	FC	UFs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	Test CFdr	fx	51	0	**51**	51	52	52	53	52	51	51	52	51	51	–	56	–
2	Test CFdr	fy	51	0	51	**51**	52	52	53	52	51	51	52	51	51	–	56	–
3	Test CFds	fx	51	0	50	50	**51**	51	52	51	52	51	51	51	51	–	55	–
4	Test CFds	fy	51	0	50	50	51	**51**	52	51	52	51	51	51	51	–	55	–
5	Test CFtr	fx	52	1	50	50	51	51	**52**	52	53	52	52	52	52	–	56	–
6	Test CFtr	fy	51	0	50	50	51	51	51	**51**	52	51	51	51	51	–	55	–
7	Test CFwd	fx	51	0	51	51	50	50	50	50	**51**	51	52	51	51	–	56	–
8	March CFwd	fy	50	0	50	50	50	50	50	50	50	**50**	51	50	50	–	55	–
9	March SAMopt	fx	51	0	50	50	51	51	51	51	50	50	**51**	51	51	–	55	–
10	March SAMopt	fy	50	0	50	50	50	50	50	50	50	50	50	**50**	50	–	55	–
11	March SAM	fx	50	0	50	50	50	50	50	50	50	50	50	50	**50**	–	55	–
12	March SAM	fy	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
13	Intra-Mats+	fx	52	4	47	47	48	48	48	48	47	47	48	47	47	–	**52**	–
14	Intra-Mats+	fy	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

  - 0.95% of the of the total of 5564 faulty chips detected with *all* Intra-BTs;
  - 0.88% of the total 6039 faulty chips detected with all used tests (i.e., Inter-BTs and Intra-BTs).

- The best intra-word tests in terms of FC are: Intra-Mats+ using fx with FC=52, and Test CFtr using x with FC= 52. However, the FC of all Intra-BTs varies between 50 and 52; note that this variation is very small as compared with that of big arrays, for which the FC varies between 127 and 312 (see Table 4).
- The best union pair in terms of the FC is 55, achieved with Intra-Mats+ using fx and one of the following tests: Test CFdr (using fx or fy), CFtr using fx, or CFwd using fx.
- There are 5 UFs detected with two tests: Test CFtr-fx with UFs=1 and Intra-Mats+-fx with UFs=4; see column 'UFs' in Table 5.
- By inspecting Table 5, we can see that the Intra-BTs can be divided into four groups; each group consists of BTs that have *exactly the same* FC. The four groups are given in the next table.

Groups	Tests
G1	CFdr-fx, CFdr-fy, CFwd-fx
G2	CFds-fx, CFds-fy, CFtr-fy, SAMopt-fx
G3	CFwd-fy, SAMopt-fy, SAM-fx
G4	CFtr-fx
G5	Intra-Mats+-fx

Table 5 can be now presented in a compact form without losing of information. The compact presentation is given in Table 6; a similar representation is used.

From Table 6 one can clearly see that G4 detects all faults detected by G2 and G3. Therefore, using one test from G1 (e.g., Test CFdr-fx), the test of G4 and the test of G5 will achieve the same FC as that achieved by the initial used Intra-BTs.

Table 6. Compact representation of Table 5

Group	FC	UFs	G1	G2	G3	G4	G5
G1	51	0	**51**	52	51	53	56
G2	51	0	50	**51**	51	52	55
G3	50	0	50	50	**50**	52	55
G4	52	1	50	51	50	**52**	56
G5	52	4	47	48	47	48	**52**

4.3 Comparison and analysis of the test results

From theoretical point of view, one can expect that intra-word coupling faults for small memories with an adjacent bit-organization will be more important than for big arrays with interleaved bit-organization. However, our (limited) experiment results show the contrary result as will be described below.

Table 7 summarizes the test results for the big and the small arrays. The small arrays have an adjacent bit-organization while the big arrays have an interleaved one; the two arrays have similar layouts. As the table shows, the number of small array chips tested is 1.5 times more than that of big arrays. However, the number of detected faults for big array is about 4 times more than that of small arrays. This indicates that as the size of the memory increases, the sensitivity to the faults also increases. In addition, the percentage of the detected faults with *all* tests (i.e., the intersection of all tests) is $\frac{344}{33913} = 0.01\%$ of the faults for big array, while this is $\frac{2490}{8529} = 29.92\%$ for small arrays. The common faults detected by all tests are the traditional well known (easy to detect) faults like stuck-at fault, transition faults, etc. These faults are probably the dominant ones for small arrays. However, for big arrays, the faults manifest themselves in a more complicated and different ways; this is indicated by the small percentage of common faults detected with all tests (i.e., 0.01%).

Table 8 compares the numbers of faults detected with Inter-BTs and Intra-BTs for the two arrays; only the faults that do not fail *all* tests are considered. The percentage of

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Table 7. Summary of the test results

	Big arrays	Small arrays
Size	1MB	25KB
number of chips tested	X	$1.5{*}X$
# chips failed	33913	8529
# chips failing *all* tests	344	2490
# chips failing *some* tests	33569	6039

the detected faults with Intra-BTs *only* (i.e., unique faults for Intra-BTs) is about 1.67% of the total faults for big arrays, and 0.94% for small arrays. If we assume that the (main) targeted faults by Intra-BTs are intra-word coupling faults, then we can conclude that occurrence probability of such faults for big arrays (with an interleaved bit-organization) is much higher than for small array (with adjacent bit-organization); this conclusion is contrary with what would have expected from theoretical point of view. The explanation of this conclusion is given next.

The intra-word coupling faults can occur between cells belonging to the same word (adjacent) as well as between I/O data paths. Such paths are the signals with high fanout like word lines, bit lines and address decoder pre-select lines. The lines carrying those signals run across the memory area and therefore have, in addition to high load, also a high capacitance coupling and cross talk effect with other signal, power and ground lines. It is evident that a big array has a long lines and therefore a higher capacitive coupling between those lines than for a small array. This means that big arrays are more sensitive for intra-word faults between these lines than for small arrays. Based on our experiment we can conclude that intra-word faults between I/O paths are more important than between adjacent memory cell within a word.

5 Conclusions

In this paper, an industrial evaluation of six new tests for intra-word coupling faults have been presented and compared with 15 known memory tests. The tests were applied to memories with bit-adjacent as well as with bit-interleaved organization. The following conclusions can be drawn for the memories considered in the experiment.

- The sensitivity of the memory to faults increases with the increase in its size. In our experiment, the number of detected faults for a big array (with an interleaved bit-organization) is about 4 times more than that for a small array (with an adjacent bit-organization). The big array is about 40 times bigger than the small one, and the number of the tested small arrays was 1.5 times more than that of tested big arrays.
- That the adjacent memory arrays are more sensitive for intra-word coupling faults than interleaved memory arrays is a wrong statement. Our experiment shows the contrary. This is possibly due to the fact that intra-word coupling faults do not only occur due to the coupling faults between cells of a single word, but also due to the coupling between adjacent lines running across the memory array like the bit line and the word lines.
- Intra-word coupling faults should be considered for any serious test purpose of leave substantial faults undetected. The percentage of detected unique faults with Intra-BTs *only* (which is about 1.67% for big arrays) cannot be ignored, especially when considering high volume production and a very low DPM level.

Table 8. Comparison of the test results

Faulty chips detected with	Big arrays		Small arrays	
	#	%	#	%
Inter and Intra BTs	33569	100.00	6039	100.00
Inter-BTs	33010	98.33	5982	99.06
Intra-BTs	2328	6.93	5564	92.21
Intra-BTs *only*	559	1.67	57	0.94
The new Intra-BTs	558	1.66	53	0.88
The new Intra-BTs *only*	347	1.03	5	0.08

The above results are, of course, design-dependent. For other memory designs and/or implementations, different results may be expected. Also, because the size of the experiment was limited, some effects may not have been noticed.

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