Analog-to-Digital Converter Based on Single-Electron Tunneling Transistors

Chaohong Hu, *Student Member, IEEE*, Sorin Dan Cotofana, *Senior Member, IEEE*, Jianfei Jiang, *Senior Member, IEEE*, and Qiyu Cai

***Abstract*—A novel single-electron tunneling transistors (SETTs) based analog-to-digital converter (ADC) is proposed in this paper. The scheme we propose fully utilizes Coulomb oscillation effect, can properly operate at $T > 0\ K$, and only a capacitive divider (built with $2n - 2$ capacitors) and n pairs of complementary SETTs are required for an n-bit ADC implementation. When compared with other state-of-the-art SET based ADCs our method provides the most compact solution measured in terms of circuit elements and has a potential advantage in terms of conversion speed. To illustrate the operation of the proposed scheme, a 4-bit ADC is demonstrated at 10K by means of simulation.**

***Index Terms*—Analog-to-digital conversion (ADC), circuit modeling, semiclassical method, single-electron tunneling.**

I. Introduction

SINGLE-ELECTRONICS, a new field of solid-state science and technology, has been developed rapidly in both theory and experiments because the essential nanofabrication techniques have become available during the past two decades [1]–[3]. The fundamental principle of single-electronics is the Coulomb blockade, which was first observed and studied by Gorter [4]. Single-electron tunneling (SET) circuits appear to be a promising candidate for future large scale integrations (LSIs) due to their ultralow power, ultrasmall size, and rich functionality. Several SET circuits have been proposed in the literature, e.g., SET memories [5], SET inverters [1], [6], SET pumps [7], SET majority gates [8], and SET threshold gates [9], etc. Furthermore, some hybrid SET/FET circuits have also been proposed, e.g., hybrid SET/FET memories [3], multiple-valued logic [10], etc. However, only a few circuits fully explore the inherent SET characteristics such as Coulomb blockade and Coulomb oscillation so far, and temperature effect is usually ignored in the design.

In this paper, we first investigate complementary SET transistors (SETTs) based implementation of periodic symmetric functions (PSFs) [11]. The proposed PSF implementation is based on a two-SETT complementary structure, fully utilizes Coulomb oscillation effect, and can properly operate at the temperature $T > 0\ K$. Efficient implementation of PSFs is of premium importance in practice as numerous computer arithmetic operations, e.g., parity, counting, and addition, etc., belong to this class of functions [11]. Moreover, analog to digital converter (ADC) behavior can be described as a PSF and this makes our scheme an ideal candidate for ADC compact implementations. Based on this PSF structure, we propose a novel ADC architecture that requires a capacitive divider (built with $2n - 2$ capacitors) and n PSFs (built with $2n$ SETTs) for an n-bit ADC implementation. Using this scheme, a 4-bit ADC is demonstrated at 10 K by means of simulation.

The remainder of this paper is organized as follows: Section II briefly describes SETT, PSF, and their characteristics. Section III introduces the PSF structure, analyzes it, and discusses the influence of $T > 0\ K$ on its behavior. Section IV presents the novel ADC scheme, simulation results, and comparisons. Finally, Section V concludes the paper with some final remarks.

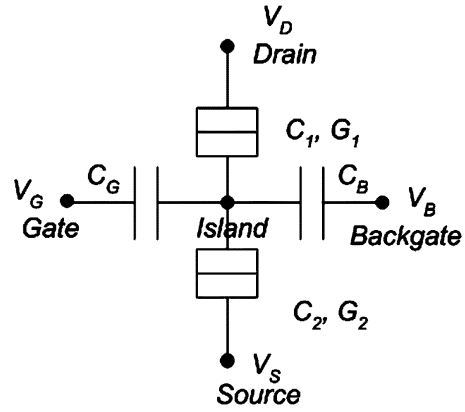

Fig. 1. SETT schematic.

II. Background

SETT is reminiscent of the usual metallic-oxide-semiconductor field-effect-transistor (MOSFET), but with a small conducting island embedded between two tunnel junctions [2], instead of the traditional inversion channel. For the tunnel junctions composing the SETT in Fig. 1, the tunnel conductance is G_1 and G_2, the junction capacitance is C_1 and C_2, respectively, and the gate and backgate capacitance is C_G and C_B, respectively. The drain, source, gate, and backgate voltage is V_D, V_S, V_G, and V_B, respectively. For the proper operation of the SETT, both G_1 and G_2 should be much smaller than $1/R_Q$, where

Manuscript received December 15, 2002; revised March 11, 2004.

C. Hu is with the Research Institute of Micro and Nanometer Science and Technology, Shanghai Jiao Tong University, Shanghai 200030, China. He is also with the Computer Engineering Laboratory, Delft University of Technology, Delft, 2628 AA, The Netherlands (e-mail: huchaohong@yahoo.com.cn).

S. D. Cotofana is with the Computer Engineering Laboratory, Delft University of Technology, Delft, 2628 AA, The Netherlands (e-mail: S.D.Cotofana@EWI.tudelft.nl).

J. Jiang and Q. Cai are with the Research Institute of Micro/Nanometer Science and Technology, Shanghai Jiao Tong University, Shanghai 200030, China.

Digital Object Identifier 10.1109/TVLSI.2004.836313

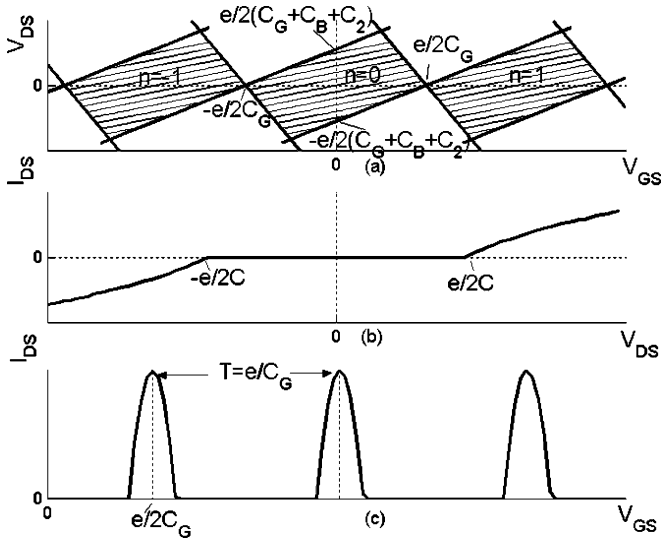

Fig. 2. (a) SETT stability diagram. (b) SETT $I_{DS} - V_{DS}$ characteristics. (c) SETT $I_{DS} - V_{GS}$ characteristics.

$R_Q = h/e^2 \approx 25.8\ k\Omega$ is the quantum unit of resistance. Furthermore, we assume that the charge energy is dominant to the thermal fluctuation, that is, $e^2/2C \gg k_B T$, where C is the total capacitance between the island and environment, and it is equal to $C_1 + C_2 + C_G + C_B$.

When assuming an operation temperature around 0 K, one can easily get the SETT stability diagram depicted in Fig. 2(a), where $q_0 = 0$ (q_0 is the background charge in the island) and $V_B = 0\ V$ are assumed. The diamond shadow areas are stable regions, where n stands for the number of electrons present in the island. If V_S is assumed to be zero, the boundaries between stability and instability can be described by the following equations:

$$-e\left(n+\frac{1}{2}\right) + q_0 = C_G(V_D - V_G) + C_2 V_D + C_B(V_D - V_B) \quad (1)$$

$$e\left(n-\frac{1}{2}\right) - q_0 = C_G(V_G - V_D) - C_2 V_D + C_B(V_B - V_D) \quad (2)$$

$$e\left(n-\frac{1}{2}\right) - q_0 = C_G V_G + C_1 V_D + C_B V_B \quad (3)$$

$$-e\left(n+\frac{1}{2}\right) + q_0 = -C_G V_G - C_1 V_D - C_B V_B. \quad (4)$$

The $I_{DS}-V_{DS}$, $I_{DS}-V_{GS}$ SETT characteristics are depicted in Fig. 2(b) and (c), where the Coulomb blockade effect is shown in Fig. 2(b) and the periodic Coulomb oscillation with the period e/C_G is shown in Fig. 2(c).

A PSF $F_p(X)$ is a symmetric function that satisfies $F_p(X) = F_p(X + T_p)$, where T_p is the function's period. Such a PSF is graphically depicted in Fig. 3, where a, b are corresponding to the first positive transition and the first negative transition, respectively [11]. Also, we can define $k = (b-a)/T_p$ as the duty ratio of the PSF. In this way, a PSF can be characterized by k, a, and T_p.

The periodic behavior in Fig. 2(c) clearly indicates that SETT is an ideal candidate for the implementation of PSFs. In the next section, we utilize the Coulomb oscillation effect and propose a SETT-based PSF implementation structure with $k = 50\%$ and $a = T_p/2$.

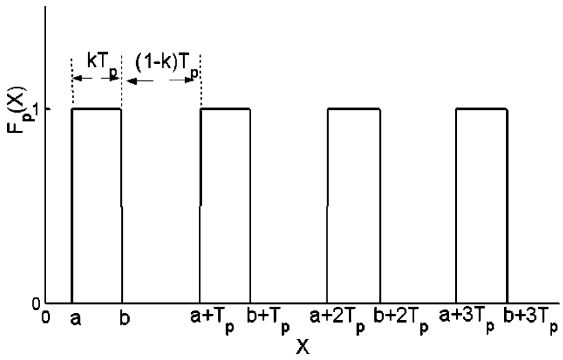

Fig. 3. Periodic symmetric functions.

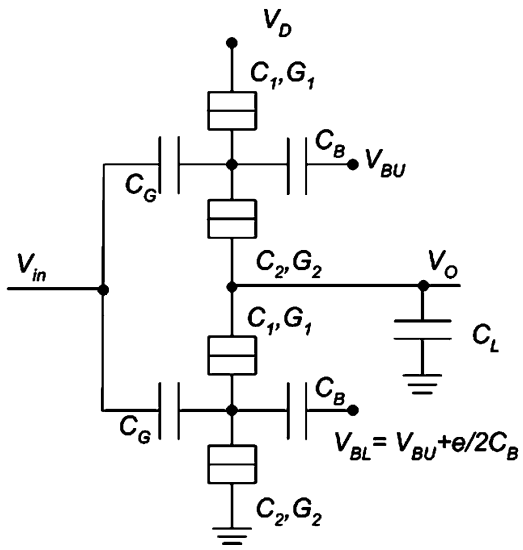

Fig. 4. Schematic of PSF structure.

III. Analysis of SET-Based PSF

A two-SETT based complementary structure was first proposed by Tucker in [1]. This is similar to a complementary MOS (CMOS) inverter circuit in structure and the work in [1] is focused on the inverter behavior of such a structure. This topology, however, can produce more than an inverter function. In this section, we explore the inherent periodic oscillation characteristic of the SETT and derive the circuit parameters corresponding to a PSF structure with $k = 50\%$ and $a = T_p/2$. We achieve this mainly by modifying the backgate bias mode. In Tucker's inverter, the backgate bias mode is $V_{BL} = V_D$ and $V_{BU} = 0\ V$. To implement a PSF having about 50% duty ratio of square-wave-like output with $a = T_p/2$, we have to derive the appropriate bias and device parameters for the structure in Fig. 4 such that when $V_{\text{in}} = X$, $V_O = F_p(X)$. This requires a backgate bias mode is as follows: $\Delta V_B = V_{BL} - V_{BU} = e/2C_B$. V_{BU} value was chosen to adjust the first PSF positive transition at $a = T_p/2$. V_D value was chosen to make the upper SETT open in one half period and closed in the other half period, and

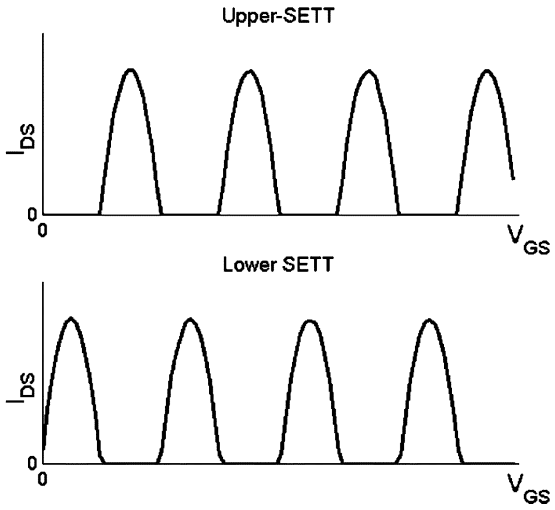

Fig. 5. Separate $I_{DS} - V_{GS}$ characteristics of the upper SETT and lower SETT of the PSF structure.

the lower SETT has a half-period phase shift of Coulomb oscillations for the backgate bias mode (see Fig. 5). In this way, for the PSF structure, in the first half period, when $q_{\text{out}} = e$ (q_{out} is the stored charges in the output capacitor, $q_{\text{out}} = e$ (or $V_O = e/C_L$) stands for logic "1" and $q_{\text{out}} = 0$ (or $V_O = 0$) for logic "0") in the preceding state, the lower SETT will turn on, and as a consequence, one electron is transported to ground and the transportation of more electrons is prohibited by the Coulomb blockade. When $q_{\text{out}} = 0$, the output will be kept stable by the Coulomb blockade. In the other half period, when $q_{\text{out}} = 0$ in the preceding state, the upper SETT will turn on and one electron is transported to output capacitor and the transportation of more electrons is prohibited by the Coulomb blockade. When $q_{\text{out}} = e$, the output will be kept stable by the Coulomb blockade. Although the discussion only covers the first period, the same rule follows in other periods because SETT has the inherent Coulomb oscillation with the period e/C_G. To adjust the oscillation period to the targeted T_p value, one has to change the C_G value accordingly. Therefore, it is possible to get a square-wave-like output signal having about 50% duty ratio (the period is e/C_G) by using the structure in Fig. 4. By solving the upper SETT boundary conditions for $n = 0$, from (2) and (4), we obtain

$$V_D = \frac{C_G V_G}{C_G + C_B + C_2} + \frac{e}{2(C_G + C_B + C_2)} \tag{5}$$

$$V_D = \frac{-C_G V_G}{C_1} + \frac{e}{2C_1}. \tag{6}$$

Then, to keep the upper SETT closed in one half period and open in the other half period when the V_{DS} is kept constant, V_D has to be set to

$$\begin{cases} V_D = \frac{C_G V_G}{C_G + C_B + C_2} + \frac{e}{2(C_G + C_B + C_2)} \\ V_D = \frac{-C_G\left(V_G + \frac{e}{2C_G}\right)}{C_1} + \frac{e}{2C_1}. \end{cases} \tag{7}$$

By solving (7), we can get

$$V_D = \frac{e}{2(C_G + C_B + C_1 + C_2)}. \tag{8}$$

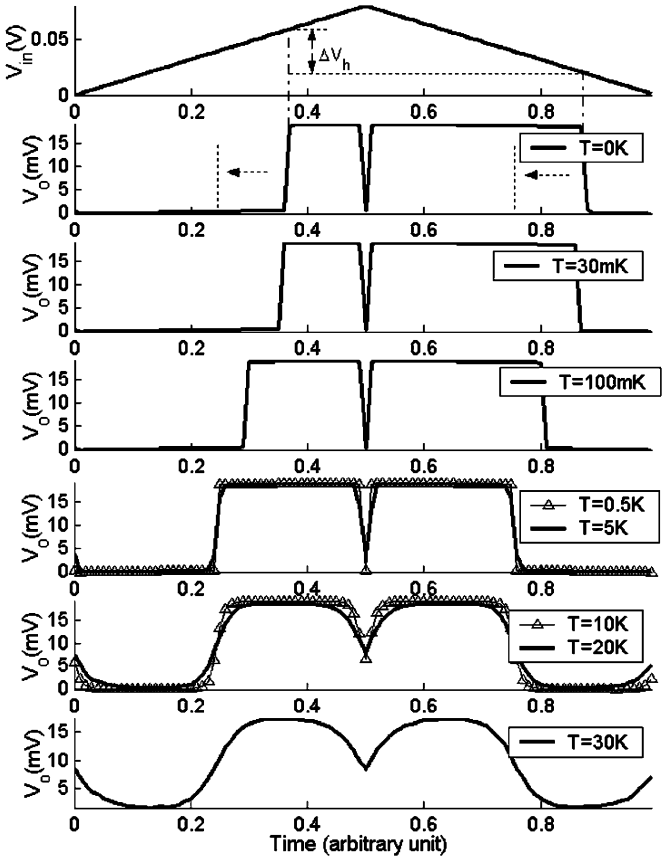

Fig. 6. PSF transfer characteristic at $T = 0$K, 30 mK, 100 mK, 0.5 K, 5 K, 10 K, 20 K, 30 K.

For the lower SETT, $V_D \approx e/C_L$, where $C_L/C_1, C_L/C_2$ are required to be much larger than 1, and this leads to

$$C_L \approx \frac{e}{V_D} = 2(C_G + C_B + C_1 + C_2). \tag{9}$$

Finally, we use V_{BU} to adjust the first PSF positive transition to $a = T_p/2$

$$V_{BU} = -\frac{e}{2C_B} \cdot \frac{C_1}{C_G + C_B + C_1 + C_2} \tag{10}$$

$$V_{BL} = \frac{e}{2C_B} + V_{BU}. \tag{11}$$

If we assume that $C_1 = C_2 = C_0$, $C_G = C_B = 20C_0$, $C_0 = 0.1$ aF, $G_1 = G_2 = G_0 = 1\ \mu S$, according to (8)–(11), we derive the proper parameters for a 50% PSF structure with $a = T_p/2$ as follows: $V_D = e/2(C_1 + C_2 + C_B + C_G) = 0.019\ V$, $C_L = e/V_D = 84C_0$, $V_{BU} \approx 0\ V$, and $V_{BL} = V_{BU} + e/2C_B \approx 0.04\ V$. We note here that the method we discussed in this section is general and can be utilized for the instantiation from the generic structure in Fig. 4 of any PSF with a duty ratio of k and $a = T_p/2$.

We simulated the 50% PSF design with SIMON [12], one of most popular SET circuit simulators, and the simulation results at various operation temperatures are depicted in Fig. 6. Because SETT has the inherent Coulomb oscillation with the period e/C_G, the simulations only cover the PSF transfer characteristic in one period. The diagrams in Fig. 6 clearly indicate the presence of output's hysteresis when $T = 0\ K$. This phenomenon is induced by the fact that for $T = 0\ K$, the turn-on

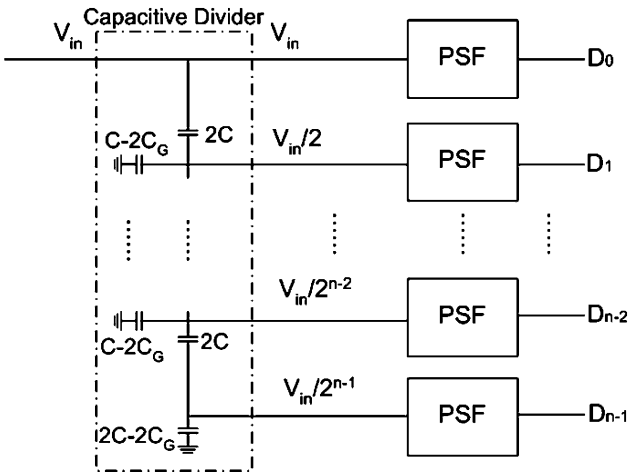

Fig. 7. Architecture for an n-bit SETT-based ADC.

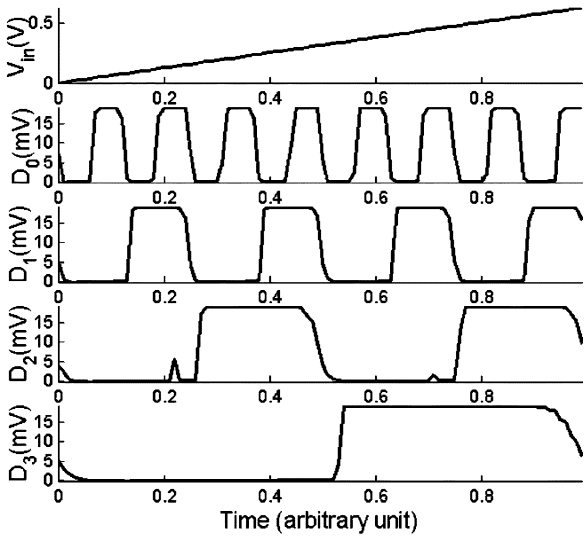

Fig. 8. Simulation results for the 4-bit SETT-based ADC at $T = 10\ K$.

region of the gate voltage for the upper SETT is $[e/2C_G+V_D+ ne/C_G, e/C_G+ne/C_G]$ when $q_{\rm out}=0$ in the preceding state, and the turn-on region of the gate voltage for lower SETT is $[ne/C_G, e/2C_G - V_D + ne/C_G]$ when $q_{\rm out} = e$ in the preceding state [13]. However, when the temperature increases the hysteresis range decreases, until it almost vanishes (see Fig. 6). This can be explained by the fact that, when the temperature increases to a certain extent, both the upper SETT and lower SETT have no strict turn-off region or Coulomb blockade region, but have different turn-on probabilities. In the region of $[e/2C_G + ne/C_G, e/C_G + ne/C_G]$, the circuit turn-on behavior is dominated by the upper SETT for its bigger turn-on probability, so the output is high; in the region of $[ne/C_G, e/2C_G + ne/C_G]$, the circuit turn-on behavior is dominated by the lower SETT for its bigger turn-on probability, so the output is low. Our simulation experiments indicate that the 50% PSF structure has a square-wave-like output without hysteresis from 0.5 to 20 K (see Fig. 6). If the temperature increases further, the periodic oscillation becomes less sharp, but this problem can be alleviated by the addition of a comparator to the output stage.

IV. SET-Based ADC

Based on the above 50% PSF structure, we propose an n-bit ADC architecture as depicted in Fig. 7. It consists of a capacitive divider and n PSFs with the same circuit parameters. According to [14], the input capacitance of SETT, $C_{\rm SETT}$, can be estimated as follows: for large amounts of charge transfer in the gate node, the net change in the SETT island is small when compared to the change in V_G and $C_{\rm SETT}$ is estimated by $C_{\rm SETT} \approx C_G$; for small amounts of charge transfer in the gate node, the net change in the SETT island cannot be neglected when compared to the change in V_G, and $C_{\rm SETT}$ is computed as $C_{\rm SETT} = C_G(1 - dV_{\rm island}/dV_G)$. In the case of the proposed ADC scheme, the first situation is applicable and the effect of each of the input capacitance of the SETT-based PSF can be compensated as $2C_G$: two parallel SETTs from the point of view in the capacitive divider.

The proposed ADC operates as follows: first, the input signal $V_{\rm in}$ is divided into $V_{\rm in}/2^i$, $i = 0, 1, 2, \ldots, n-1$, by the capacitive divider; then it is encoded into the corresponding binary output signals by the PSFs. If the ADC input $V_{\rm in} \in [0,\ V_{\rm max}]$, $V_{\rm max} = 2^{n-1}T_p$, the output bit D_i, following the radix-2 counting rule, can be evaluated with 50% PSFs after the input is divided into $V_{\rm in}/2^i$, $i = 0, 1, \ldots, n-1$. This means that when $V_{\rm in} \in (mT_p{\cdot}2^i,\ V_{\rm max}/2^{n-i}+mT_p{\cdot}2^i), m = 0, 1, \ldots, n-i-1$, the output $D_i = 0$, and otherwise, $D_i = 1$ [11]. Using this scheme, we simulated a 4-bit ADC built with PSFs having the parameters in Section III. The simulation results at $T = 10\ K$ are depicted in Fig. 8, which clearly displays ADC behavior. The extension of the 4-bit ADC design to a higher number of bits is straightforward and does not require redesigning the parameters of the PSF structure and/or the capacitive divider.

When compared with conventional flash ADCs, the proposed ADC is more compact because it utilizes the SETTs inherent periodicity. In particular for an n-bit ADC our scheme requires n PSFs, whereas a conventional flash n-bit ADC requires $2^n - 1$ comparators and latches for the encoding function. Asymptotically speaking this means an $O(n)$ area instead of an $O(2^n)$ area. In practice, this means more than reducing the area from an exponential complexity to a linear complexity due to the fact that a comparator and latch is more complex than a PSF block. Additionally, our proposal does not require the thermometer code to binary code encoder in conventional flash ADCs because the outputs of PSF blocks in our proposal are already normal binary code. When compared with previous proposed SET-based ADCs [10], [15], [16] our scheme requires less circuit elements (area). In particular, it doesn't require the discharge circuit and a sign reverser circuit like the one in [15]. No structures for coding the analog input signal into pulse-width modulation or voltage ramp circuit are necessary like the one in [16]. When compared with the ADC proposed in [10], it requires roughly the same amount of basic building blocks but the PSF we use requires two SETTs only, whereas the literal gate in [10] is built with one SETTs and two MOSFETs. Besides, our proposal can operate at $T > 0\ K$, whereas the ones in [15] and [16] require 0 K for the proper operation. Finally, due to a lower network depth, our proposal has a potential advantage in speed when compared with [10], [15], and [16].

V. Conclusion

In this paper, we first investigated the SETT-based implementation of PSFs. The scheme we proposed fully utilizes Coulomb oscillation effect can properly operate at $T > 0\ K$ and only two complementary SETTs are required for a PSF implementation. Based on the proposed PSF structure, we proposed a novel ADC architecture that can properly operate at $T > 0\ K$. Our proposal requires a capacitive divider (built with $2n-2$ capacitors) and n PSFs for an n-bit ADC implementation, and it is the most compact SET based ADC scheme up to date. Additionally, due its shallow network it has a potential advantage in terms of speed when compared with other state-of-the-art SET-based ADC schemes [10], [15], [16]. Using this scheme, a 4-bit ADC was demonstrated at 10 K by means of simulation. Although our work was validated by means of simulation, only existing experiment [10], demonstrating the feasibility of interconnecting SETT with a capacitive divider suggests that our approach utilizing Coulomb oscillation in circuit design can be potentially implemented. Practical validation of our proposal still needs further experimental demonstration and constitutes future work. Last but not least, the PSF implementation we proposed might potentially open new research avenues in SET-based logic and arithmetic circuits.

References

[1] J. R. Tucker, "Complementary digital logic based on the Coulomb blockade," *J. Appl. Phys.*, vol. 72, no. 9, pp. 4399–4413, Nov. 1992.

[2] C. Wasshuber, *Computational Single-Electronics*. New York: Springer-Verlag, 2001.

[3] K. K. Likharev, "Single-electron devices and their applications," *Proc. IEEE*, vol. 87, pp. 606–632, Apr. 1999.

[4] C. J. Gorter, "A possible explanation of the increase of the electrical resistance of thin metal films at low temperatures and small field strengths," *Physica*, vol. 17, no. 8, pp. 777–780, Aug. 1951.

[5] C. Wasshuber, H. Kosina, and S. Selberherr, "A comparative study of single-electron memories," *IEEE Trans. Electron Devices*, vol. 45, pp. 2365–2371, Nov. 1998.

[6] C. P. Heij, P. Hadley, and J. E. Mooij, "Single-electron inverter," *Appl. Phys. Lett.*, vol. 78, no. 8, pp. 1140–1142, Feb. 2001.

[7] T. Altebaeumer and H. Ahmed, "Silicon nanowires and their application in bi-directional electron pumps," *Microelectron. Eng.*, vol. 57–58, pp. 1029–1033, 2001.

[8] H. Iwamura, M. Akazawa, and Y. Amemiya, "Single-electron majority logic circuits," *IEICE Trans. Electron.*, vol. E81-C, no. 1, pp. 42–46, Jan. 1998.

[9] C. R. Lageweg, S. D. Cotofana, and S. Vassiliadis, "A linear threshold gate implementation in single electron technology," in *Proc. IEEE Computer Society Workshop VLSI 2001: Emerging Technologies VLSI Systems*, Orlando, FL, Apr. 2001, pp. 93–98.

[10] H. Inokawa, A. Fujiwara, and Y. Takahashi, "A multiple-valued logic with merged single-electron and MOS transistors," in *IEDM Tech. Dig.*, 2001, pp. 7.2.1–7.2.4.

[11] S. D. Cotofana and S. Vassiliadis, "Periodic symmetric functions, serial addition and multiplication with neural networks," *IEEE Trans. Neural Networks*, vol. 9, pp. 1118–1128, Nov. 1998.

[12] SIMON—Simulation of Nano Structures. Avaliable. [Online]www.lybrary.com/simon/

[13] K. Uchida, K. Matsuzawa, and A. Toriumi, "A new design scheme for logic circuits with single electron transistors," *Jpn. J. Appl. Phys.*, vol. 38, pp. 4027–4032, 1999.

[14] N. M. Zimmerman and M. W. Keller, "Dynamic input capacitance of single-electron transistors and the effect on charge-sensitive electrometers," *J. Appl. Phys.*, vol. 87, no. 12, pp. 8570–8574, 2000.

[15] C. H. Hu, J. F. Jiang, and Q. Y. Cai, "A single-electron-transistor-based analog/digital converter," in *Proc. IEEE NANO*, 2002, pp. 487–490.

[16] S. J. Ahn and D. M. Kim, "Asynchronous analogue-to-digital converter for single-electron circuits," *Electron. Lett.*, vol. 34, pp. 172–173, 1998.

Chaohong Hu (S'02) was born in China in 1978. He received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, Zhejiang Province, China, in July 2000. He is currently pursuing the Ph.D. degree in microelectronics and solid-state electronics at Shanghai Jiao Tong University, Shanghai, China.

From April 2003 to April 2004, he was a Visiting Research Fellow with the electrical engineering, mathematics, and computer science faculty, Delft University of Technology, Delft, The Netherlands. His current research work is focusing on nanoelectronics, computer arithmetic, and computer-aided design.

Sorin Dan Cotofana (SM'00) was born in Mizil, Romania. He received the M.Sc. degree in computer science from the "Politehnica" University of Bucharest, Bucharest, Romania, in 1984, and the Ph.D. degree in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 1998.

For 10 years, he worked with the Research and Development Institute for Electronic Components, Bucharest, where he was involved with structured design of digital systems, design rule checking of ICs layout, logic, and mixed-mode simulation of electronic circuits, testability analysis, and image processing. Currently, he is an Associate Professor with the electrical engineering, mathematics and computer science faculty, Delft University of Technology. His research interests include computer arithmetic, nanoelectronics, parallel architectures, embedded systems, reconfigurable computing, neural networks, computational geometry, and computer-aided design.

Jianfei Jiang (SM'02) received the B.S. degree in applied physics, from Zhejiang University, Hangzhou, Zhejiang Province, China, in 1960.

Currently, he is a Professor with Shanghai Jiao-Tong University, Shanghai, China. From 1990 to 1993, and from September 1995 to November 1995, he was a Guest Professor at Yokohama National University, Yokahama, Japan. He has undertaken long-term research projects on microelectronics, nanoelectronics, and superconductivity electronics. He is the author and editor (including cooperative author) of six published books, and two additional books scheduled for publication. He has published over 120 papers on the famous domestic and international journals. His current research focus is nanoelectronics and mesoscopic systems.

Prof. Jiang was a member of the evaluating group of the Second, Third, Fifth, and Sixth Committee of the National Natural Science Foundation, China, and the commissioner of the First to the Eighth Volumes of the Chinese Integrated Circuits. He is a senior member of CIE, and a member of the Japanese Academy of Applied Physics.

Qiyu Cai received the B.S. degree from the Department of Electronics, Zhejiang University, Hangzhou, Zhejiang Province, China, in 1965, where she majored in semiconductor materials and devices.

Currently, she is an Associate Professor with Shanghai Jiao Tong University, Shanghai, China. She has published and cooperatively published over 30 papers. Her research interests include slice-shaped semiconductor single-crystal, large-scale integrated circuits, semiconductor diamond film, superconductivity electronics and nanoelectronics.