Single-Electron Tunneling Transistor Implementation of Periodic Symmetric Functions

Chaohong Hu, Sorin Dan Cotofana, and Jianfei Jiang

***Abstract*—This paper investigates the implementation of generic periodic symmetric functions (PSFs) with single-electron tunneling transistors (SETTs). The PSF implementation scheme we propose fully utilizes the SETT Coulomb oscillation effect and can properly operate at $T > 0$ K, and only a pair of complementary SETTs is required for the implementation of any PSF. Based on the novel PSF block, we propose an analog-to-digital converter (ADC) scheme that requires n PSFs for an n-bit ADC implementation. To demonstrate our approach, a 4-b ADC and a 7|3 counter were designed and verified at 10 K by means of simulation.**

***Index Terms*—Analog-to-digital converter (ADC), circuit optimization, counters, single-electron tunneling, symmetric functions.**

I. Introduction

SINGLE-ELECTRON tunneling (SET) circuits are promising for future large-scale integrated circuits (LSIs) because they have ultrasmall size and rich functionality and dissipate ultralow power. Several SET circuits have been proposed in the literature (see, for example, [1]–[6]). However, only a few of them have fully explored the inherent SET characteristics such as Coulomb blockade and Coulomb oscillation so far, and the temperature effect is usually ignored in the design.

In this paper, we first investigate SET transistor (SETT)-based implementation of generic periodic symmetric functions (PSFs). This class of functions is of particular interest as numerous computer arithmetic operations belong to it, e.g., parity and addition, counting [thus by implication analog-to-digital conversion (ADC)] [7]. The scheme we proposed fully utilizes the Coulomb oscillation effect and can properly operate at temperatures higher than 0 K, and only a pair of complementary SETTs is necessary for the implementation of any PSF. Subsequently, to demonstrate the application of our proposal, an ADC scheme based on the proposed PSF structure is introduced. Only n PSFs are required for an n-bit SETT-based ADC implementation. Using this scheme, a 4-b ADC and a 7|3 counter are demonstrated at 10 K by means of simulation.

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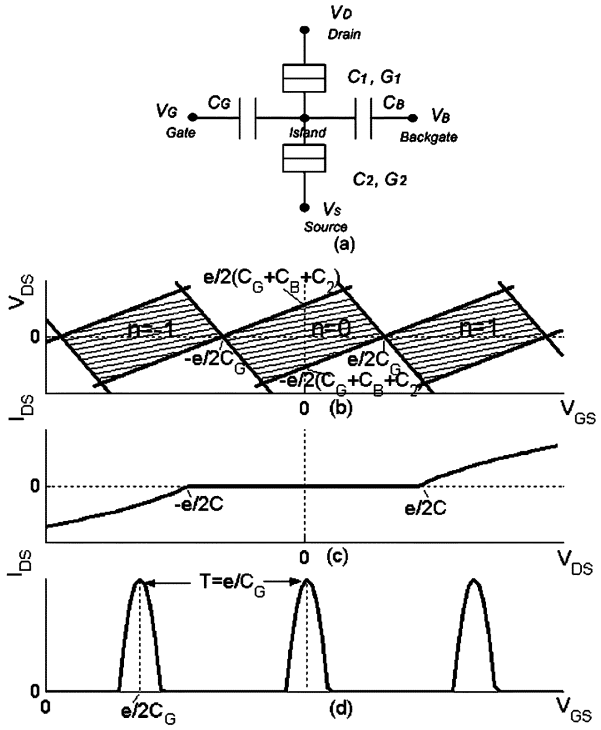

Fig. 1. (a) SETT schematic. (b) SETT stability diagram. (c) SETT $I_{\rm DS} - V_{\rm DS}$ characteristics. (d) SETT $I_{\rm DS} - V_{\rm GS}$ characteristics.

II. Background

When assuming an operation temperature around 0 K, one can easily obtain the stability diagram of an SETT [shown in Fig. 1(a)], depicted in Fig. 1(b), where $q_0 = 0$ (q_0 is the background charge in the island) and $V_B = 0$ are assumed and the diamond shadow areas are the stable region, where n stands for the number of electrons present in the island [2], [3]. The $I_{\rm DS} - V_{\rm DS}$, $I_{\rm DS} - V_{\rm GS}$ SETT characteristics are depicted in Fig. 1(c) and Fig. 1(d), respectively, where the Coulomb blockade effect is indicated in Fig. 1(c) and the periodic Coulomb oscillation with the period e/C_G is shown in Fig. 1(d).

The periodic behavior in Fig. 1(d) suggests that the SETT is an ideal candidate for PSF implementations. A PSF is a symmetric function $F_p(X)$ (a symmetric function is a function in which its output entirely depends on the sum of the inputs $X = \sum x_i$) that satisfies $F_p(X) = F_p(X + T_p)$, where T_p is the function's period. One can define $k = (b-a)/T_p$ as the duty ratio of the PSF, where a and b correspond to the first positive transition and the first negative transition, respectively [7]. In this way, a PSF can be completely characterized by k, a, and T_p.

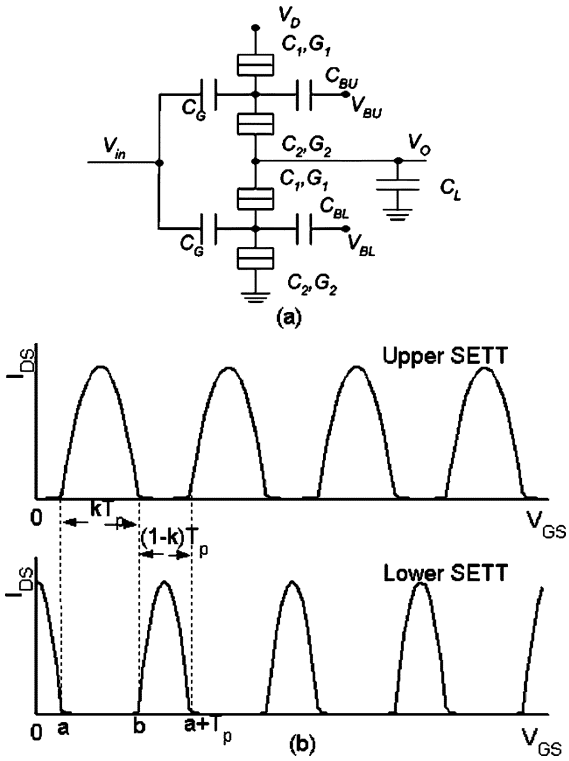

Fig. 2. (a) Schematic of the generic PSF structure. (b) Separate $I_{\rm DS} - V_{\rm GS}$ characteristics of the upper SETT and lower SETT of the generic PSF.

In Section III, we utilize the Coulomb oscillation effect and propose a generic SETT-based PSF implementation structure.

III. SETT-Based PSF

The complementary structure with two SETTs was first proposed by Tucker in [1]. This is similar to a complementary MOS (CMOS) inverter circuit in structure, and the work in [1] focused on the inverter behavior of such a structure. However, this topology can produce more than an inverter function. In this section, we explore the SETT inherent periodic oscillation characteristic and derive a generic implementation of a PSF having the duty ratio of k by modifying the backgate bias mode and the device parameters. In Tucker's inverter, the backgate bias mode is assumed to be $V_{\rm BL} = V_D$ and $V_{\rm BU} = 0$. To implement a PSF, we have to derive the appropriate bias and device parameters for the structure in Fig. 2(a) such that, when $V_{\rm in} = X$, $V_O = F_p(X)$. V_D, $C_{\rm BU}$, and $C_{\rm BL}$ values have to be chosen such that the upper SETT is open in kT_p of a period, and the lower SETT is open in $(1-k)T_p$ of a period. $V_{\rm BL}$, $V_{\rm BU}$ are used to adjust the first positive transition point at the targeted a and to provide a phase difference of kT_p between the lower SETT and the upper SETT [see Fig. 2(b)].

In this way, when $\exists m$, $m \in \{0, 1, 2, \ldots, v\}$, where v is the number of periods covered by the PSF, such that $X \in (b + mT_p, a + (m+1)T_p)$, the generic PSF structure behaves as follows: if $q_{\rm out} = e$ [$q_{\rm out}$ is the stored charges in the output capacitor, $q_{\rm out} = e$ (or $V_O = e/C_L$) stands for logic "1" and $q_{\rm out} = 0$ (or $V_O = 0$) for logic "0"] in the preceding state, the lower SETT will turn on and one electron is transported to the ground and the transportation of more electrons is prohibited by the Coulomb blockade; if $q_{\rm out} = 0$, the output will be kept stable by the Coulomb blockade. Therefore, in both cases, the output is "0," as it should be. When $\exists m$ such that $X \in [a + mT_p, b + mT_p]$, the following holds true: if $q_{\rm out} = 0$ in the preceding state, the upper SETT will turn on and one electron is transported to the output capacitor and the transportation of more electrons is prohibited by the Coulomb blockade; if $q_{\rm out} = e$, the output will be kept stable by the Coulomb blockade. Then, the output is "1," as it should be.

The period T_p is determined by C_G (the period T_p is e/C_G); thus, to adjust the oscillation period to T_p, one has to change the C_G value accordingly. Therefore, the structure in Fig. 2(a) exhibits the basic behavior required in order to construct a k duty ratio PSF implementation. Next we have to derive the circuit parameters that provide the targeted a, k. By solving the upper SETT boundary conditions for $n = 0$ [2], it can be derived that

$$V_D = \frac{C_G V_G}{(C_G + C_{\rm BU} + C_2)} + \frac{0.5e}{(C_G + C_{\rm BU} + C_2)} \tag{1}$$

$$V_D = -\frac{C_G V_G}{C_1} + \frac{0.5e}{C_1}. \tag{2}$$

Then, to keep the upper SETT closed in $(1-k)T_p$ of a period and open in kT_p of a period when the $V_{\rm DS}$ is kept constant, V_D has to be set to

$$\begin{cases} V_D = \dfrac{C_G V_G}{(C_G + C_{\rm BU} + C_2)} + \dfrac{0.5e}{(C_G + C_{\rm BU} + C_2)} \\ V_D = -\dfrac{C_G\left(V_G + \frac{ke}{C_G}\right)}{C_1} + \dfrac{0.5e}{C_1} \end{cases}. \tag{3}$$

By solving (3), the following can be derived:

$$V_D = \frac{k \cdot e}{(C_G + C_{\rm BU} + C_1 + C_2)}. \tag{4}$$

It can be deduced by analogy that, to keep the lower SETT open in $(1-k)T_p$ of a period and closed in kT_p of a period, when the $V_{\rm DS}$ is kept constant, V_D is required to satisfy

$$V_D = \frac{(1-k) \cdot e}{(C_G + C_{\rm BL} + C_1 + C_2)}. \tag{5}$$

For the lower SETT, it can be assumed that $V_D \approx e/C_L$, where C_L/C_1 and C_L/C_2 are required to be much larger than 1. Thus,

$$C_L \approx \frac{e}{V_D} = \frac{(C_G + C_{\rm BU} + C_1 + C_2)}{k} = \frac{(C_G + C_{\rm BL} + C_1 + C_2)}{1-k}. \tag{6}$$

By solving (6), the relationship between $C_{\rm BU}$ and $C_{\rm BL}$ can be deduced as

$$C_{\rm BU} = \frac{k(C_G + C_{\rm BL} + C_1 + C_2)}{(1-k)} - (C_G + C_1 + C_2). \tag{7}$$

Then to adjust the targeted a, the following $V_{\rm BU}$, $V_{\rm BL}$ values are required:

$$V_{\rm BU} = \frac{e}{C_{\rm BU}} \cdot \left[\frac{k \cdot (C_G + C_{\rm BU} + C_2)}{C_G + C_{\rm BU} + C_1 + C_2} + \frac{1}{2} - k - \frac{a}{T_p}\right] \tag{8}$$

$$V_{\rm BL} = \frac{e}{C_{\rm BL}} \cdot \left[\frac{(1-k) \cdot (C_G + C_{\rm BL} + C_2)}{C_G + C_{\rm BL} + C_1 + C_2} + \frac{1}{2} - \frac{a}{T_p}\right]. \tag{9}$$

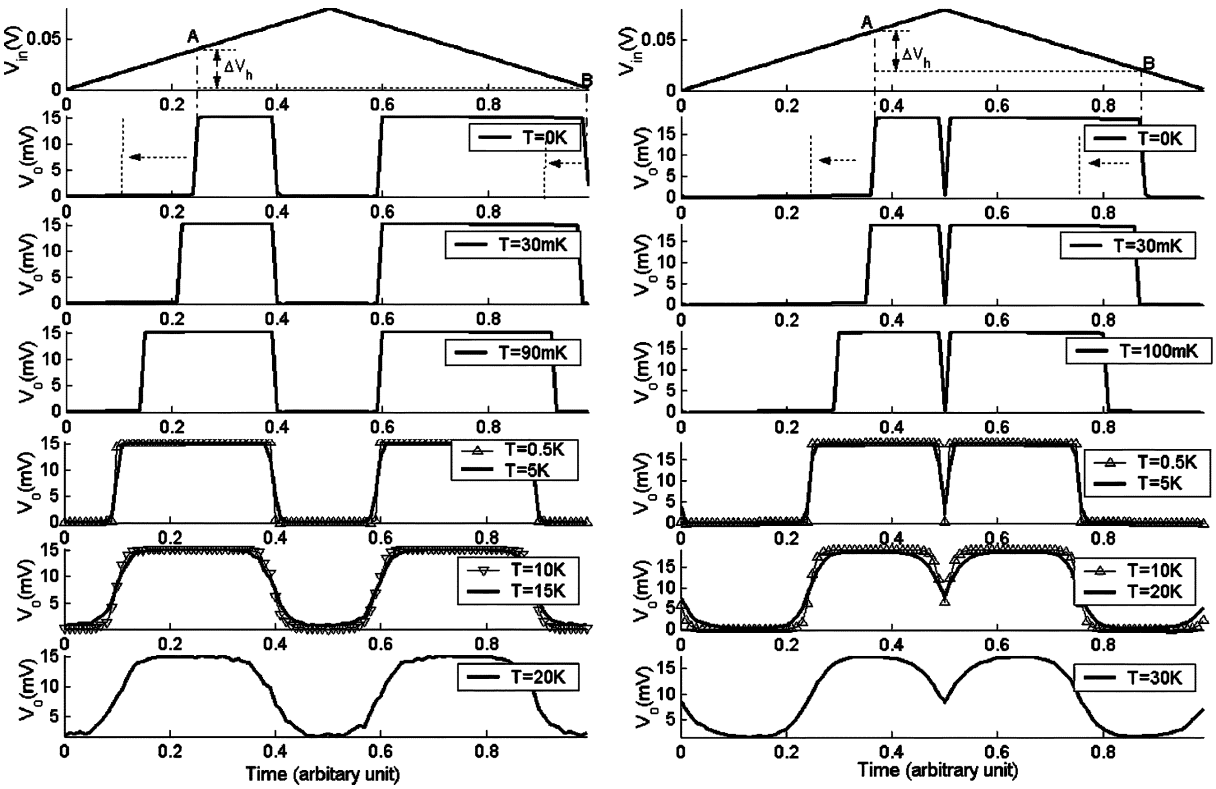

Fig. 3. Transfer characteristic in a period of the PSF structure at different temperatures (left for $a = T_p/5$, $k = 60\%$; right for $a = T_p/2$, $k = 50\%$).

If the V_D value is given (as it might be the case in practice), certain circuit parameters, e.g., C_1 and C_2, have to be adjusted in order to obtain the targeted k.

To demonstrate our approach, we instantiated and simulated a $k = 60\%$ PSF with $a = T_p/5$ and a $k = 50\%$ PSF with $a = T_p/2$. We assumed that $C_1 = C_2 = C_0$, $C_G = C_{\rm BL} = 20C_0$, $C_0 = 0.1$ aF, and $G_1 = G_2 = G_0 = 1$ μS, and, according to (4)–(9), we derived the proper parameters for the $k = 60\%$ PSF structure with $a = T_p/5$ as follows: $V_D = 0.0153$ V, $C_{\rm BU} = 41C_0$, $C_L = 105C_0$, $V_{\rm BU} = 0.0113$ V, and $V_{BL} = 0.0553$ V. In the same way, we deduced that the proper parameters for the PSF with $k = 50\%$, $a = T_p/2$ are: $V_D = 0.019$ V, $C_{\rm BU} = 20C_0$, $C_L = 84C_0$, $V_{\rm BU} = -0.000\,95$ V, and $V_{\rm BL} = 0.0391$ V.

We simulated both designs with SIMON [8] and the results are presented in Fig. 3. Because the SETT has the inherent Coulomb oscillation with the period e/C_G, the simulations only cover one period of the PSF. The diagrams in Fig. 3 clearly indicate the presence of the output's hysteresis when $T = 0$ K. According to our calculations (see the Appendix), the hysteresis width ΔV_h can be expressed as

$$\Delta V_h = |V_{\rm GA} - V_{GB}|. \tag{10}$$

Using (10), we calculated $\Delta V_h = 0.0393$ V for the case of the PSF structure with $a = T_p/5$, $k = 60\%$ and $\Delta V_h = 0.0391$ V for the case of the PSF structure with $a = T_p/2$, $k = 50\%$, and these values are almost identical to the simulation results ($\Delta V_h = 0.0398$ V for the $a = T_p/5$, $k = 60\%$ PSF and $\Delta V_h = 0.0392$ V for the $a = T_p/2$, $k = 50\%$ PSF) in Fig. 3.

However, when the temperature increases, the hysteresis range decreases until it almost vanishes. This can be explained by the fact that, when the temperature is increasing up to a certain extent, both the upper and lower SETTs have no strict turn-off region or Coulomb blockade region, but have different turn-on probabilities.

Thus, the following holds true: if $X \in [a + mT_p, b + mT_p]$, the circuit turn-on behavior is dominated by the upper SETT for its bigger turn-on probability, so the output is high; if $X \in (b + mT_p, a + (m + 1)T_p)$, the circuit turn-on behavior is dominated by the lower SETT for its bigger turn-on probability, so the output is low. The simulations indicate that the PSF structure has a hysteresis-free output for operation temperatures between 0.5 and 15 K for the 60% PSF and between 0.5 and 20 K for the 50% PSF (see Fig. 3). If the temperature increases further, the periodic oscillation becomes less sharp, but this problem can be alleviated by the addition of a comparator to the output stage.

As discussed before, in the proposed scheme, the value of the load capacitance C_L is determined by (6). In practical PSF-based applications, the effective value of C_L may deviate from the computed value due to various fan-outs, wiring lengths, and possible V_D fluctuations. To investigate the sensitivity of our proposal to capacitance and voltage deviations, we simulated various cases for the 60% PSF and the 50% PSF at 10 K by setting $C_L \pm 10\%$ or by setting $V_D \pm 10\%$. Our investigations indicate that when such parameter deviations are present the PSF output stays within 10% of the output simulated with the targeted ideal C_L and V_D values, that is, the PSF scheme does not amplify the effect of circuit parameters deviation at its output.

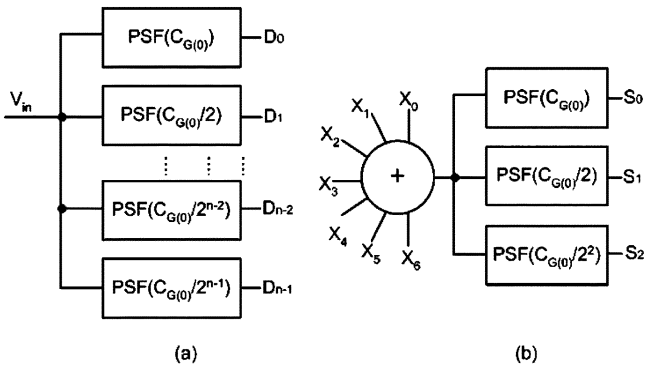

Fig. 4. (a) n-bit SETT-based ADC and (b) $7|3$ counter.

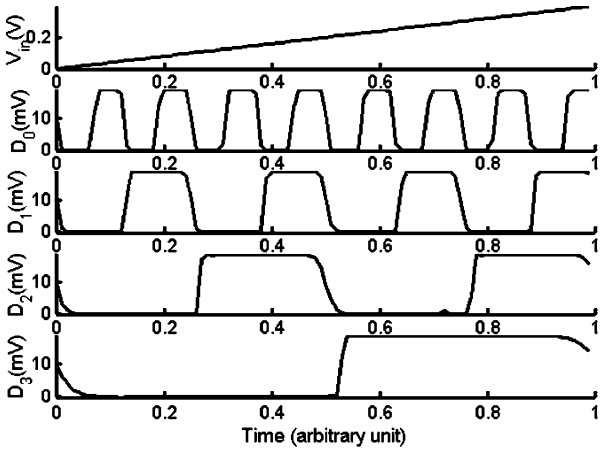

Fig. 5. Simulation results for the 4-bit SETT-based ADC at $T = 10$ K.

IV. PSF Applications

Based on the $k = 50\%$ PSF with $a = T_p/2$ in Section III, we propose an n-bit SETT-based ADC architecture as depicted in Fig. 4(a). The operation principle of the proposed scheme is based on the following observations: if the ADC input $V_{\rm in} \in [0, V_{\max}]$, $V_{\max} = 2^{n-1}T_{p(0)}$, the output bit D_i, $i = 0, 1, \ldots, n-1$, following the radix-2 counting rule, can be evaluated with a 50% PSF with $T_{p(i)} = e/C_{G(i)}$, where $C_{G(i+1)} = C_{G(i)}/2$. This means that, when $V_{\rm in} \in (mT_{p(i)}, V_{\max}/2^{n-i} + mT_{p(i)})$, $m = 0, 1, \ldots, n-i-1$, the output $D_i = 0$, otherwise $D_i = 1$ [7]. Therefore, the input signal $V_{\rm in}$ is directly encoded into the corresponding binary output signals by n 50% PSFs with the period $T_{p(i)} = e/C_{G(i)}$, where $C_{G(i+1)} = C_{G(i)}/2$. Moreover, to keep V_D of all of PSFs as a constant, $C_{G(i)} + C_{BL(i)} = const$ has to be chosen, and then $C_{\rm BU}$, $V_{\rm BU}$, and $V_{\rm BL}$ are determined by (7)–(9), respectively.

Using this scheme, we instantiated and simulated a 4-b ADC constructed with PSFs having the circuit parameters as in Section III except for C_G and $C_{\rm BL}$, $C_{\rm BU}$, where we assumed that $C_{G(0)} = 32C_0$ and $C_{G(i)} + C_{BL(i)} = 40C_0$. The simulation results at $T = 10$ K are presented in Fig. 5, which clearly displays ADC behavior. The extension of the n-bit ADC design to a higher number of bits is straightforward according to the scheme described above.

When compared with a previous proposed SETT-based ADC [5], [6], our proposal is much more compact and requires less

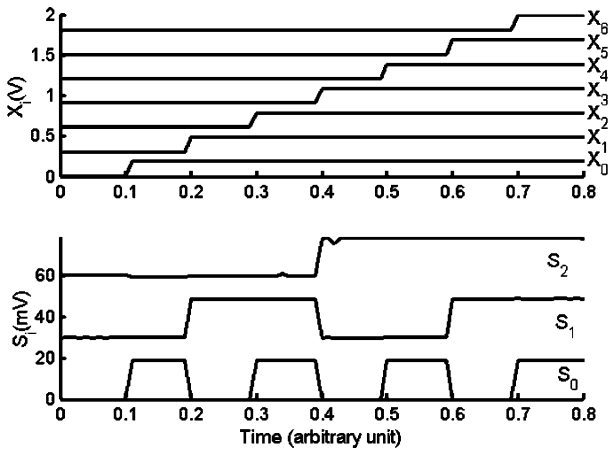

Fig. 6. Simulation results for the SETT-based $7|3$ counter at $T = 10$ K (offset by 0.3 V for X_i and 30 mV for S_i, respectively).

circuit elements (area). In particular, no structures for coding the analog input signal into pulse-width modulation or voltage ramp circuit are necessary like that in [5]. When compared with the ADC proposed in [6], it requires roughly the same amount of basic building blocks but the PSF we use requires two SETTs only, whereas the literal gate in [6] is built with one SETT and two MOSFETs. Additionally, due to the fact that we adjust the circuit parameters for each individual PSF in the ADC, our scheme does not need to include a capacitive divider. In addition, due to a lower network depth, our proposal has a potential advantage in speed when compared with [5] and [6]. Finally, our proposal can operate at $T > 0$ K, whereas the one in [5] requires 0 K for proper operation.

As indicated in [7], PSFs can be utilized as building blocks for the implementation of computer arithmetic circuits, e.g., adders, and multipliers. In particular, PSFs are quite appropriate for efficient implementation [7] of population counters [9] that are elementary cells for larger arithmetic structures such as multipliers. To demonstrate this, we designed a compact architecture for a $7|3$ counter (it calculates the total number of logic "1" over the seven inputs and represents it as a 3-b binary number), as depicted in Fig. 4(b). In our design, the linear sum of the inputs is realized with seven identical capacitors $C_X = 100$ aF, and we have chosen 0.19 V and 0.01 V as the input high level and the input low level, respectively. The simulation results at 10 K for the $7|3$ counter are presented in Fig. 6, and one can clearly observe that the design correctly evaluates the $7|3$ counter function. The output high level and low level we obtained from this approach are 0.019 and 0 V, respectively. The gain is only 0.1, which is in fact an inherent key disadvantage of the SETT, but we can easily acquire input–output compatible levels in the $7|3$ counter-based circuits via a buffering scheme, e.g., the one presented in [10], which successfully amplified a signal from a SETT to a MOSFET with a gain of about 100.

V. Conclusion

We investigated the implementation of PSFs with SETTs and proposed a novel generic PSF implementation scheme. The scheme we introduced fully utilizes the Coulomb oscillation effect and can properly operate at temperatures higher than 0 K and only two complementary SETTs are required for any PSF

implementation. Based on the novel PSF block, we proposed an ADC scheme that requires n PSFs for an n-bit ADC implementation. We demonstrated our approach by designing a 4-b ADC and a 7|3 counter that were verified at 10 K by means of simulation. Therefore, the PSF implementation we proposed might potentially open new research avenues in SET-based logic and arithmetic circuits.

APPENDIX
DERIVATION OF HYSTERESIS

When $T = 0$ K, we observed that an output's hysteresis phenomenon occurs (see Fig. 6) for the proposed PSF structure. To derivate the hysteresis width, first we assume that the PSF can be divided in a linear circuit, and the voltage effect to each tunnel junction from each independent voltage source can be treated separately. Thus, Thevenin's theorem can be utilized for each tunnel junction [2]. Second, we introduce the following notations: for the upper SETT's junction 2, V_{c2U} is the junction's critical voltage, and $V_{j2U}(V_D)$ is the voltage effect of V_D on junction 2. For the lower SETT's junction 1, V_{c1U} is the junction's critical voltage, and $V_{j1U}(Q_O(e))$ is the voltage effect of $q_{\rm out}$ on junction 1. Moreover, according to [11], SETT has two possible carrier transport processes: the single electron process (in which an electron is first transferred from the drain to the island through junction 1 and then transferred to source through junction 2) and single hole process (in which an electron is first transferred from the island to source through junction 2, thus one hole is left, and then occupied by an electron transferred from the drain through junction 1), which are determined by the minimum energy barrier.

At position A in Fig. 3, the preceding state is $q_{\rm out} = 0$, thus the PSF reversing is dominated by the upper SETT. In this case, the single hole process is applicable. Thus, the gate voltage $V_{\rm GA}$ at the position A is

$$V_{\rm GA} = \frac{(V_{c2U} - V_{j2U}(V_D)) \cdot ((C_1 + C_{\rm BU} + C_G)(C_2 + C_L) + C_2 C_L)}{C_G C_L} - \frac{C_{\rm BU} V_{\rm BU}}{C_G} - \frac{e}{C_G}. \tag{A1}$$

At position B in Fig. 3, the preceding state is $q_{\rm out} = e$, thus the PSF reversing is dominated by the lower SETT. In this case, the single electron process is applicable. So the gate voltage $V_{\rm GB}$ at position B is

$$V_{\rm GB} = \frac{(V_{c1L} - V_{j1L}(Q_o(e))) \cdot ((C_1 + C_{\rm BL} + C_G)(C_1 + C_L) + C_1 C_L)}{C_G C_L} - \frac{C_{\rm BL} V_{\rm BL}}{C_G}. \tag{A2}$$

Therefore, ΔV_h can be obtained as follows:

$$\Delta V_h = |V_{\rm GA} - V_{\rm GB}|. \tag{A3}$$

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