A CMOS Semi-Custom Chip for Mixed Signal Designs

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Abstract—**This paper describes a redesign of a Sea-of-Gates chip that was developed at Delft University of Technology more than 10 years ago, and that has extensively been used at laboratory courses since then. The main difference with the original chip is that the new one has several analog cells like OpAmps, comparators, and resistor banks in addition to a large core of Sea-of-Gates transistors. While the Sea-of-Gates transistors are mainly used to implement the digital parts of the design, the analog cells can efficiently be used to create analog sub-systems like amplifiers and digital-to-analog converters. Similar as to the original Sea-of-Gates chip, the designer uses the OCEAN/Nelsis design system to generate two metallization layers to implement the design.**

Keywords— **mixed-signal, semi-custom, IC, Sea-of-Gates, analog cell array.**

I. INTRODUCTION

A Sea-of-Gates chip is a semi-custom chip in which arrays of transistors have been pre-fabricated. The designer only defines the metallization wires to connect the transistors that implement the circuit. As a result, only a short design time and processing time are required to obtain an integrated circuit.

At Delft University of Technology, a Sea-of-Gates (SoG) circuit was developed more than 10 years ago. This chip has extensively been used at laboratory courses since then [1]. In the 2nd year of the bachelor study for electrical engineering, students design a mostly digital integrated circuit (except for some simple analog interfaces) using the SoG chip. The metallization layers are deposited by the university institute DIMES. After that, the students test the chip.

To design the SoG circuit, commercial VHDL simulation and synthesis tools are used for the front-end. For the back-end, the layout tools from the OCEAN/Nelsis design system [2] are used.

During the last decade, advanced programmable devices such as FPGAs have become available. Due to their computational power and flexibility, these devices have overshadowed the application of semi-custom chips like the SoG circuit for digital designs. However, for analog or mixed digital/analog applications, programmable devices do not yet provide a good solution.

In this paper, we describe how we made a redesign of the SoG chip that was developed in Delft, such that also analog or mixed digital/analog circuits can easily be created. The original Sea-of-Gates chip was extended with several (pre-designed) analog components like OpAmps, comparators and resistor ladder networks. Similar as to the original SoG chip, the designer only defines the metallization wires to connect the different components. This facilitates the design of analog sub-systems like amplifiers and digital-to-analog converters, without knowledge about how to create the components of these sub-systems.

The design of the Sea-of-Gates with Analog Ring (SoGAR) chip is done in a similar way as the original SoG chip. The difference is that now (1) also mixed-level simulation is required to simulate the mixed digital/analog parts, and (2) the analog components have a fixed placement on the chip.

This paper is structured as follows. In Section II we give an overview of the layout and possibilities of the SoGAR chip. Section III discusses a design-flow for the chip. In Section IV, a design example is presented. Section V describes the realization of the SoG chip. Finally, Section VI gives some concluding remarks.

II. Chip Overview

An overview of the layout of the SoGAR chip is shown in Figure 1. In the middle, a Sea-of-Gates core that consists of an array of 45,994 pmos transistors and 45,994 nmos transistors occupies most of the chip area. The Sea-of-Gates core is similar to the fishbone image of the original SoG chip and consists of alternating rows of pmos and nmos transistors. Although the transistors on the image can in principle be used to create any type of MOS circuit (with the limitations that the width and length of the transistors are fixed), the Sea-of-Gates core is primarily used to create the digital circuit parts. In addition, the Sea-of-Gates core is the only area where the designer is allowed to define wires to connect the different circuit parts.

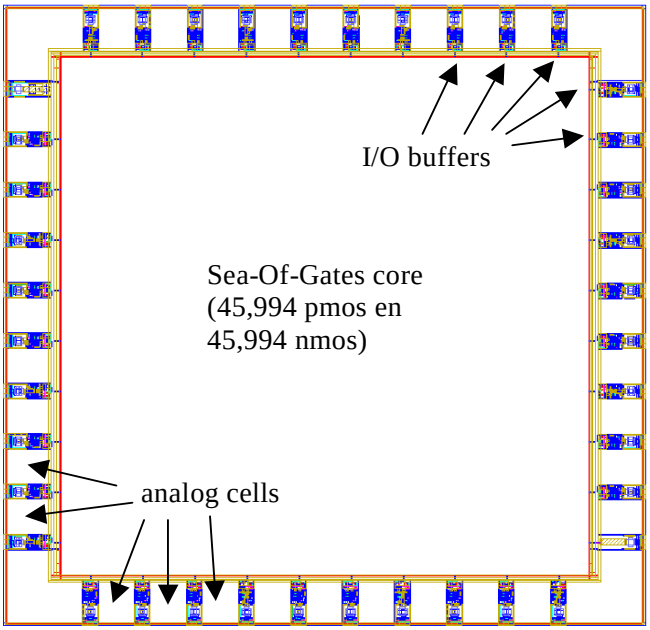

Figure 1 Overview of the layout of the chip.

At the boundary of chip, 40 bonding pads are available. Default, two bonding pads are used for the supply voltages (GND and VDD). The buffers of the other 38 pads can be programmed as input and/or output, using different metallization patterns.

Between the I/O buffers, analog cells are placed as shown in Figure 2. All layers of the cells have been pre-designed but the metal layers are of course deposited only when the final, custom, layers are deposited on the chip. The analog cells can be utilized in the design by connecting to their pins that are positioned at the boundary of the Sea-of-Gates core.

Around the Sea-of-Gates core, 3 separate metal rings are defined that can be used, if necessary, for separate positive supply voltages for the I/O buffers, the analog circuit parts and the digital circuit parts.

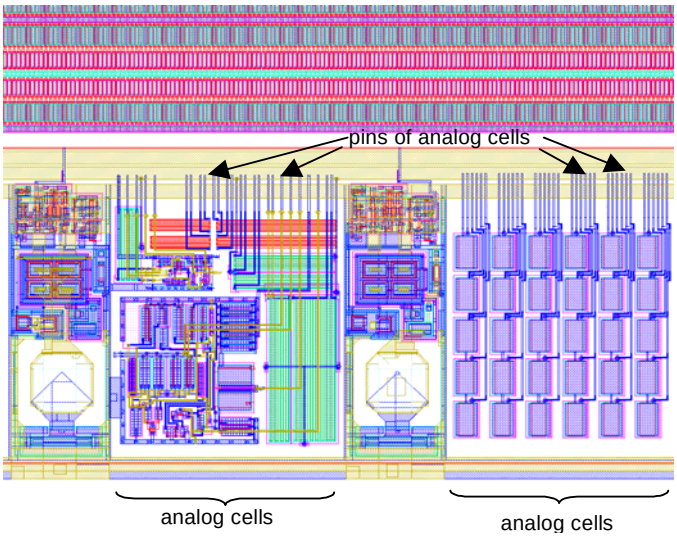

Figure 2 Part of the layout with 2 I/O buffers, analog cells, and (at the top) the Sea-Of-Gates transistor area.

A. Digital Components

As mentioned above, digital components are created on the Sea-of-Gates core by defining a metallization pattern that connects different transistors on the image, as e.g. shown in Figure 3. Already since the original SoG chip, a library of digital cells (nands, nors, exors, multiplexer, selector, flipflops) is available. Using a logic synthesis tool, this library can be used to translate RTL descriptions into netlists that can be mapped directly onto the layout.

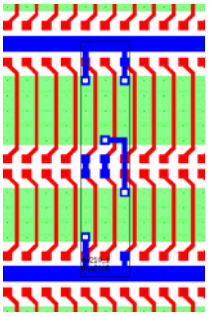

Figure 3 A 2-input nand placed on the Sea-of-Gates image.

B. Analog Components

Table 1 gives an overview of the analog components that are available in the ring around the SoG core.

Table 1 Analog components on the SoGAR chip

component	*number*
OpAmp	16
comparator	16
8 bits resistor ladder network	8
resistors	256
capacitors	72

The OpAmp has a high output current class AB output stage and high slew-rate for driving large capacitive loads. Internal frequency compensation, high bandwidth and large pmos input transistors for low noise. The 8 bits resistor ladder network includes switches and is designed to create a digital-to-analog converter in combination with an OpAmp.

III. Design Flow

In Figure 4, the design flow for the SoGAR chip is shown. The steps "schematic design" and "simulation" and "re-simulation" can be done using any design system that supports schematic entry and mixed-level simulation. The other steps are done using the OCEAN/Nelsis tools.

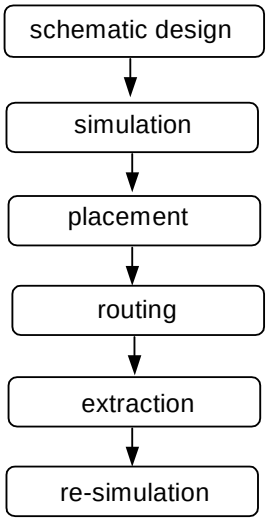

Figure 4 Design Flow

A. *Schematic Design*

The schematic diagram is created using components from the digital cell library and the analog cell library. For digital parts, a logic synthesis tool can be used to convert a high-level VHDL or Verilog description into a gate-level description.

B. *Simulation*

The schematic is simulated at the logic, circuit or mixed level, depending on the type of components that are part of the schematic and depending on the level of simulation detail that is required.

C. *Placement*

For a schematic that contains only digital components, a placement of the components is done on the Sea-of-Gates image (see Figure 3) using the OCEAN placement tool madonna.

For other schematics, the analog components can only be placed in the layout at certain positions along the boundary of the SoG core. To assign the analog components to a position in the layout, the designer specifies an indication for the placement of each analog instance in the schematic. This is done as e.g. shown in Figure 5 by using the parameter "pos".

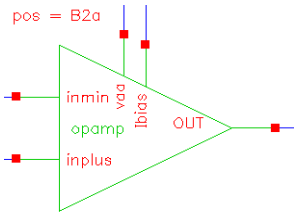

Figure 5 An analog component with a parameter pos to indicate the placement position.

When the schematic is translated into a layout, the analog instance in the schematic is then mapped to an analog instance in the layout as shown in Figure 6. Each analog instance in the layout has a unique position along the boundary of the SoG core. The instance consists of only a few metal wires that connect to the pins of the real layout of the analog cell that is placed somewhere between the I/O buffers.

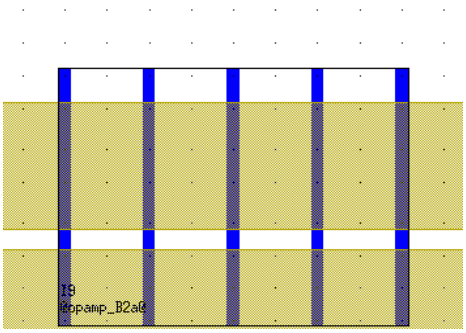

Figure 6 Analog component placed along the boundary of the SoG core.

D. *Routing*

Using only the SoG area, the OCEAN tool trout routes the wires between the digital and the analog instances.

E. *Extraction*

The designed layout on the SoG core is extracted using the OCEAN/Nelsis tool Space. For the analog components, a pre-extracted circuit description is available.

F. *Re-simulation*

The extracted netlist can be input for a final simulation, similar as in step B.

IV. Design Example

In this section we present the design of an analog-to-digital (A/D) converter to illustrate the design process for the SoGAR chip. The schematic of the circuit is shown in Figure 7. The A/D converter uses an 8 bits up/down counter, a D/A converter, and a comparator.

The up/down counter generates an 8 bits digital value to approximate the analog input value. The input "test_result" of the counter indicates if the current value is too high or too low and will let the counter count up or down on the next clock cycle. To prevent an alternating output value on a stable analog input, the counter has a test output vector of which the value is incremented or decremented at every clock cycle, as well as a stable output vector that follows the test vector only when it makes two subsequent increments or two subsequent decrements.

The test output vector of the counter is converted to an analog value using the D/A converter that consists of (1) an OpAmp that generates a low-ohmic voltage half of the value of the supply voltage, (2) an 8 bits resistor ladder network that provides a current proportional to the value of the binary vector, and (3) an OpAmp that transforms the current to a voltage.

The comparator has as inputs the analog input value to be converted and the analog value from the D/A converter, and provides as output the input signal test_result for the counter.

At the top right of the schematic an instance "bond_ring" has been placed to specify how the inputs and outputs of the circuit are connected to the I/O pads of chip. The router will use this information when the layout is created.

Initially the counter is described in a Verilog RTL description. In Figure 8, a simulation result of the circuit is shown. One can see how the analog output for the D/A converter follows the analog input signal, and which digital output values are generated.

After simulation, the next step is to transform the RTL description of the counter into a netlist consisting of instances from the digital cell library. This is done using a logic synthesis tool. Then, this netlist is used to create a layout for the counter using the OCEAN tools madonna and trout, see Figure 9.

To create the layout for the total D/A converter, placement indications are assigned to the resistors, the OpAmps, the comparator and the ladder network shown in Figure 7. The schematic in Figure 7 is then mapped to a layout where the analog instances and the bond_ring

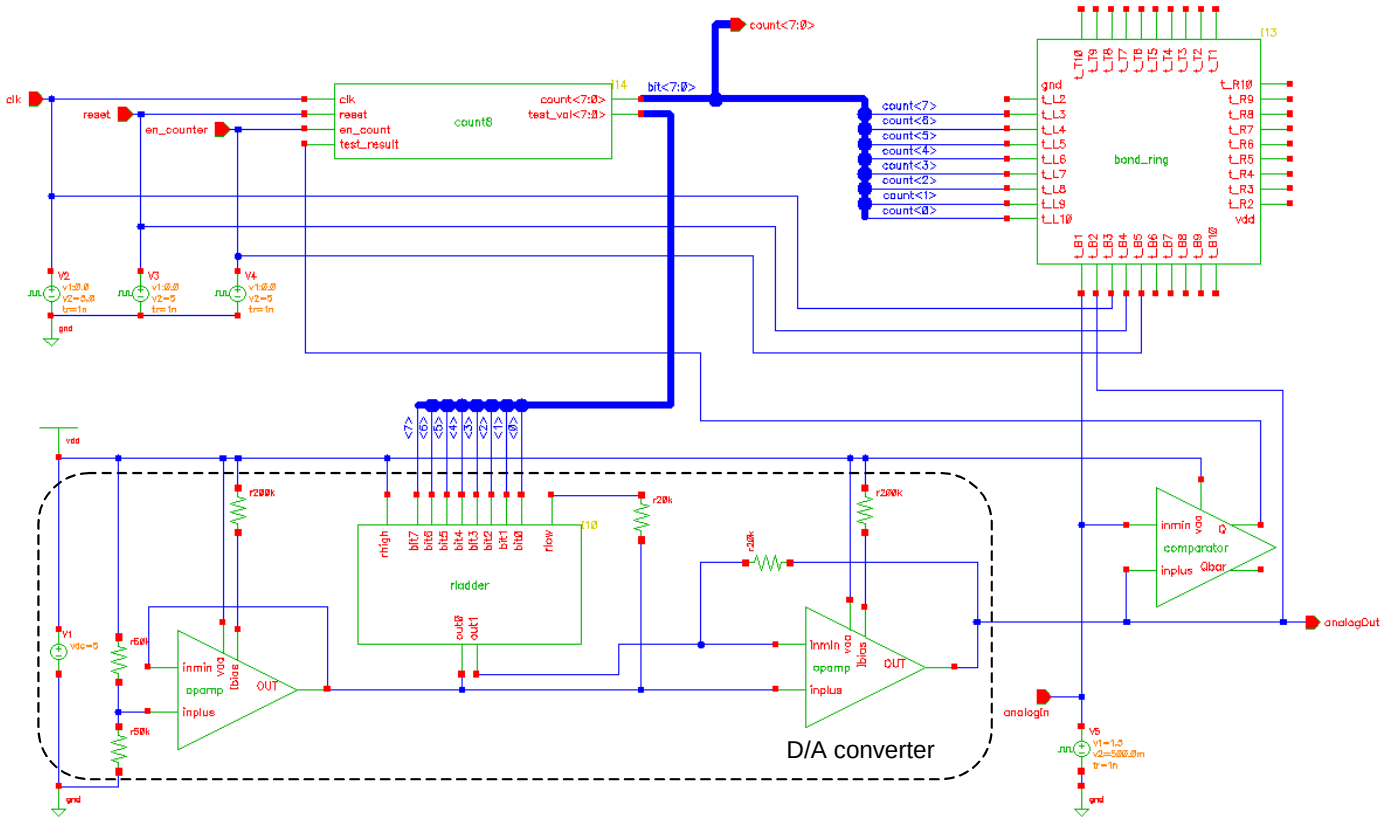

Figure 7 Schematic of an A/D converter.

have a fixed position. The previously created layout instance for the counter is placed manually. After routing the circuit, a layout is obtained as shown in Figure 10. The supply rings of the instance bond_ring give a clear indication of the boundary of the SoG core. One can see that the layout of the A/D converter occupies less than 8 % of the total area available on the Sea-of-Gates core.

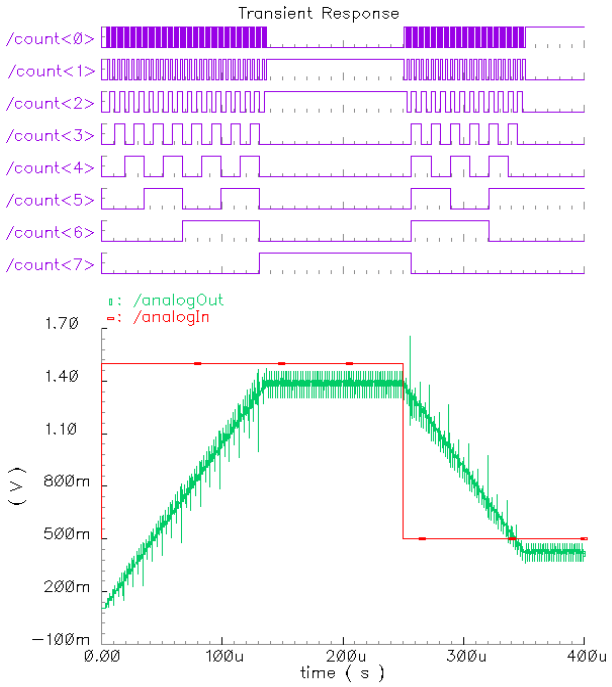

Figure 8 Simulation results for the A/D converter.

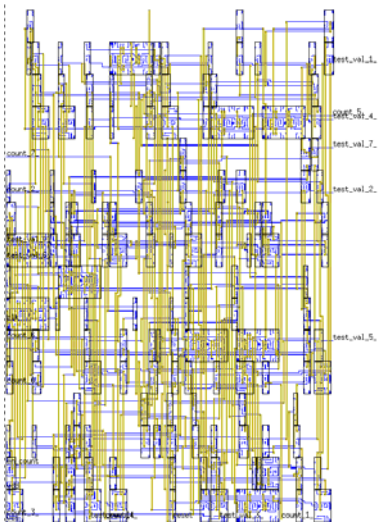

Figure 9 Layout of the counter

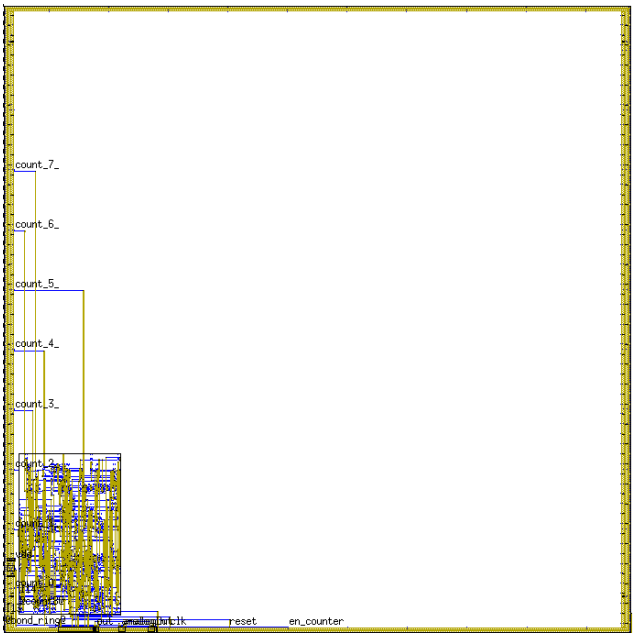

Figure 10 Layout of the complete A/D converter

V. Chip Realization

A first version of the SoGAR chip is planned to be fabricated at the university institute DIMES, 4th quarter 2004. For the technology, a 1.6 µm n-well CMOS technology will be used. For our purpose, education of IC design, high performance is not an essential aspect. Therefore we have chosen a technology that provides us, in the first place, reliability, low cost and easy accessibility.

Most of the components of the SoGAR chip have been part of previous designs in the DIMES 1.6 µm CMOS technology. Based on measurement results from these designs and based on simulation results, the following table lists some performance figures for the SoGAR chip.

Table 2 Some performance figures for the SoGAR chip in DIMES 1.6 µm CMOS technology.

supply voltage	5 V
max clock frequency	100 MHz
typ. gate delay	0.3 ns
OpAmp bandwith	5.5 MHz
OpAmp rise/fall time	90 ns
OpAmp offset	11 mV
comparator prop. delay	100 ns

VI. Concluding Remarks

In this paper we have presented a semi-custom chip, SoGAR, for mixed signal applications. The chip is intended to be used for a 2nd year IC design course during the bachelor study at Delft University of Technology, but may find other applications as well.

The chip combines a Sea-of-Gates design style for digital parts with an analog cell array. The analog cells are placed in a ring around the Sea-of-Gates core between the bonding pads. The analog cells include general purpose OpAmps, comparators, resistor ladder network, resistors and capacitors.

Since the designer creates only 2 metal layers, only a short design and processing time are required.

The designer creates the custom part of the layout of the chip using the OCEAN/Nelsis design environment. This involves placement and routing of components from the digital and analog library, only on the SoG core.

A first version of the chip will be processed at DIMES in 1.6 µm CMOS technology Q4 2004.

References

[1] P. Groeneveld, E. Hendriks, A. Bakker, R. Nouta and C. Verhoeven, "The TU Delft undergraduate design course: Students design a complex sea-of-gates chip from scratch up to a ‘working product’", Proceedings Fourth Eurochip Workshop on VLSI Design Training, pp. 2-17, Toledo, Spain, 1993.

[2] P. Groeneveld and P. Stravers, Ocean: The Sea-of-Gates Design System, Delft University of Technology, The Netherlands, Feb. 1993.