ON EFFECTIVE COMPUTATION WITH NANODEVICES: A SINGLE ELECTRON TUNNELLING TECHNOLOGY CASE STUDY

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Abstract
It is generally accepted that fundamental physical limitations will eventually inhibit further (C)MOS feature size reduction. Several emerging nano-electronic technologies with greater scaling potential, such as Single Electron Tunneling (SET), are currently under investigation. Each of these exhibit their own switching behavior, resulting in new paradigms for logic design and computation. This paper presents a case study on SET based logic. We analyze and compare three different SET designs styles as follows. First, SET transistor based designs that mimic conventional CMOS. Second, single electron threshold logic based on the voltage threshold of SET tunnel junctions. Third, electron counting logic based on direct encoding of integers as charge combined with computation via charge transport.

1. INTRODUCTION

Feature size reduction in microelectronic circuits has been an important contributing factor to the dramatic increase in the processing power of logic and arithmetic circuits. However, it is generally accepted that sooner or later MOS based circuits cannot be reduced further in (feature) size due to fundamental physical restrictions [1]. Therefore, several emerging technologies are currently being investigated [2].

When examining the progress made with these new technologies one can certainly observe that the main research effort occurs at the device level. As a result of this, limited innovation has been occurred at the circuit and system level. Mainly, there have been attempts to mold the emerging devices to the CMOS design style by making them mimic the behavior of the MOS transistor. Given that most nano devices exhibit a different behavior than the MOS transistor, such attempts make limited use of the potential of the technology itself. We believe that an emerging (nano)technology can be effectively used only if its specific behavior is explicitly utilized at all design levels, i.e., device, circuit and system. In other words, one should examine and utilize a technology's unique features. In an attempt to demonstrate this we carry on a case study on the Single Electron Tunnelling (SET) technology.

Single Electron Tunnelling (SET) [3], [4] is a novel technology candidate that offers greater scaling potential than MOS as well as the potential for ultra-low power consumption. Additionally, recent advances in silicon based fabrication technology (see for example [5]) show potential for room temperature operation. However, similar to other future technology candidates, SET devices display a switching behavior that differs from traditional MOS devices. This provides new possibilities and challenges for implementing digital circuits.

The SET technology introduces the quantum tunnel junction as a new circuit element for (logic) circuits. The tunnel junction can be thought of as a "leaky" capacitor, such that the "leaking" can be controlled by the voltage across the tunnel junction. Although this behavior at first glance appears similar to that of a diode, the difference stands in the scale at which switching occurs. Charge transport though a tunnel junction can only occur in quantities of a single electron at a time. Additionally, given the feature sizes anticipated for such circuits, the transport of a single electron can have a significant effect on the voltage across a tunnel junction, such that transporting a few electrons through a tunnel junction will inhibit further charge transport, making it possible to control the transport of charge in discrete and accurate quantities.

In this paper we analyze and compare three different SET design styles. First, a CMOS-like design style based on SET transistors. Second, single electron encoded logic in which Boolean variables are encoded as a net charge of $0e$ and $1e$ present on the gate's output node. Third, electron counting logic in which integers variables are encoded directly in charge. Each design style is introduced in detail and its main advantages and disadvantages are analyzed. We then compare these design styles in terms of area, delay and power consumption.

The remainder of this paper is organized as follows. Section 2 briefly presents some SET background theory, explaining the basic switching behavior appearing in SET circuits and a method for calculating delay

and power. Section 3 presents the SET equivalent of the CMOS design style. Section 4 presents the implementation of single electron encoded threshold logic gates in SET technology. Section 5 presents electron counting logic and schemes for the calculation of addition and multiplication via a the controlled transport of single electrons. Section 6 discusses the main problems of the SET technology in general and compares the three design styles. Finally, Section 7 concludes the paper with some final remarks.

2. BACKGROUND

A tunnel junction can be thought of as a leaky capacitor. The transport of charge through a tunnel junction is referred to as *tunneling*, where the transport of a single electron through a tunnel junction is referred to as a *tunnel event*. Electrons are considered to tunnel through a tunnel junction strictly one after another. We assume that all conditions are met such that charge quantization is observable ($E_C >> E_Q$) and that tunnel events due to thermal energy can be ignored ($E_C >> K_bT$). Under these conditions, the critical voltage V_c across a tunnel junction is the voltage threshold that is needed across the tunnel junction in order to make a tunnel event through this tunnel junction possible.

For calculating the critical voltage of a junction, we assume a tunnel junction with a capacitance of C_j. The remainder of the circuit, as viewed from the tunnel junction's perspective, has an equivalent capacitance of C_e. Given the approach presented in [6], we calculate the critical voltage V_c for the junction as:

$$V_c = \frac{e}{2(C_e + C_j)}. \tag{1}$$

In the equation above, as well as in the remainder of this discussion, we refer to the charge of the electron as $q_e = 1.602 * 10^{-19}\ C$. Strictly speaking this is incorrect, as the charge of the electron is of course negative. However, it is more intuitive to consider e as a positive constant for the formulas which determine whether or not a tunnel event will occur. We of course correct for this when we discuss the direction in which the tunnel event takes place.

Generally speaking, if we define the voltage across a junction as V_j, and assuming the conditions stated above, a tunnel event will occur through this tunnel junction if and only if:

$$|V_j| \geq V_c. \tag{2}$$

If tunnel events cannot occur in any of the circuit's tunnel junctions, i.e., $|V_j| < V_c$ for all junctions in the circuit, the circuit is in a *stable state*. For our investigation we only consider circuits where a limited number of tunnel events may occur, resulting in a stable state. Each stable state determines a new output value resulting from the distribution of charge throughout the circuit.

The transport of an electron through a tunnel junction is a stochastic process. This means that we cannot analyze delay in the traditional sense. Instead, assuming a non-zero probability for charge transport ($|V_j| > V_c$), the switching delay t_d of a single electron transport can be calculated based on an error probability P_{error} that the desired transport did not occur as

$$t_d = \frac{-ln(P_{error})q_eR_t}{|V_j| - V_c}, \tag{3}$$

where $R_t = 10^5\Omega$ is the tunnel resistance (though depending on the physical implementation this value is typically assumed). The error probability P_{error} determines the reliability of the circuit. Given that the switching behavior is stochastic in nature, the error probability cannot be reduces to 0. It is therefore assumed that when P_{error} is not acceptable a certain error correction mechanism has to be embedded in the form of hardware or data redundancy in order to achieve the desired accuracy.

When charge transport occurs through a tunnel junction, the difference in the total amount of energy present in the circuit before and after the tunnel event can be calculated by

$$\Delta E = E_{final} - E_{initial} = -q_e(|V_j| - V_c). \tag{4}$$

Therefore, the energy consumed by a single tunnel event occurring in a single tunnel junction can be calculated by taking the absolute value of ΔE. In order to calculate the power consumption of a gate, the energy consumption of each tunnel event is multiplied by the frequency of switching. The switching frequency in turn depends on the frequency at which the gate's inputs change and it is input data dependent, as a new combination of inputs may or may not results in charge transport.

In addition to the switching error probability as described in Equation (3) there are two fundamental phenomena that may cause errors: thermally induced tunnelling and co-tunnelling. Given a maximum acceptable switching error probability, we must ensure that both the thermal error probability as well as the co-tunnelling error probability are of the same order of magnitude or less. For any temperature $T > 0$ there exists a non-zero probability that a tunnel event will occur through a junction even if $|V_j| < V_c$. The error probability P_{therm} due to thermal tunnelling can be described by a simple formula as

$$P_{therm} = e^{-\Delta E/K_bT}. \tag{5}$$

For a multi-junction system in which a combination of tunnel events leads to a reduction of the energy present in the entire system there exists a non-zero

probability that those tunnel events occur simultaneously even if $|V_j| < V_c$ for all individual tunnel junction involved. This phenomenon is commonly referred to as co-tunnelling [7], [8].

Although a detailed analysis of co-tunnelling is outside the scope of the present work, we remark that several means are available to reduce the co-tunnelling error probability. First, the ratio of co-tunnelling rate to the desired tunnelling rate can be reduced linearly by increasing the tunnel resistance R_t of the tunnel junctions involved in co-tunnelling. The main problem of this approach is that it also linearly increases the switching delay as stated in Equation (3). Second, each of the individual junctions involved in the co-tunnelling process can be replaced by N junctions ($N > 1$) separated by islands. Although such an approach results in an exponential decrease of the co-tunnelling probability, it also approximately results in a linear increase of the delay time as an electron must now tunnel through N times as many junctions as before. Third, resistors can be added between the SET circuit and the supply voltage lines as demonstrated in [9], [10], [11]. This method can reduce the co-tunnelling rate without significantly increasing the delay. This is due to the fact that the delay added by a resistor is on the RC scale. Thus, assuming for example $R = O(10^6)\ \Omega$ and $C = O(10^{-17})\ F$, we find that the delay added by the resistor is $t_{RC} = O(10^{-11})\ s$. Given that for the structures we discuss in this paper the switching delay t_d is in the order of $O(10^{-9})\ s$, the additional delay due to the co-tunnelling suppressing resistors can be neglected. Although the circuits discussed in the remainder of this paper do not contain such resistors, co-tunnelling suppressing resistors of appropriate value can be appended to the designs in order to reduce the co-tunnelling error to the acceptable error probability.

3. CMOS-LIKE TRANSISTOR LOGIC

One of the first SET circuits examined in literature is the capacitively coupled SET transistor (see [12] for an early review paper). The SET transistor consists of two tunnel junctions in series, with a capacitor attached to the inter-laying circuit node, as depicted in Figure 1. The resulting 3-terminal structure can be seen as being similar to a MOS transistor, such that the gate voltage V_g can control the transport of charge through the tunnel junctions (current I_d).

However, unlike the MOS transistor, the current I_d through the SET transistor has a periodic response to the input voltage V_g. By extending the SET transistor design with a capacitively coupled biasing input, one can translate the transfer function of the SET transistor over the V_g axis.

When combining two complementary biased SET transistors in a single circuit, we arrive at the SET

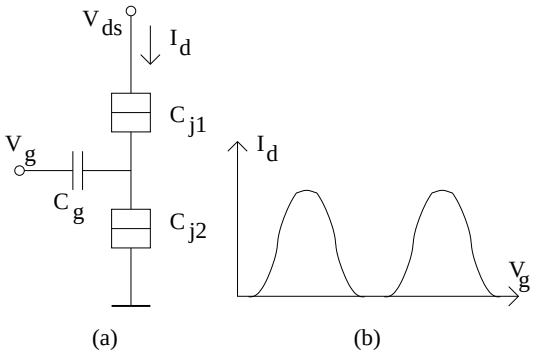

Fig. 1. The SET transistor (a) circuit and (b) transfer function.

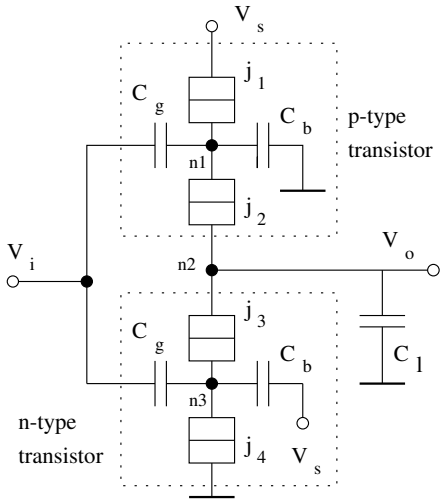

Fig. 2. CMOS-like SET inverter.

inverter structure depicted in Figure 2. The SET inverter, as first proposed in [13], operates as follows. The upper SET transistor behaves similar to a p-type transistor, while the lower transistor operates similar to an n-type transistor. Output switching (from 0 to 1) is accomplished by transporting electrons (typically over 100) from the output node $n2$ to the top supply voltage terminal V_s, or (from 1 to 0) by transporting electrons from the bottom ground terminal to the output node $n2$.

Given that SET transistors can be biased such that they behave similar to p or n transistors, we can convert existing CMOS cell libraries to their SET equivalents. Various complementary SET transistor logic families have been proposed [14], [13], [15], [16], [17], [18], [19], [20]. Figure 3 for example depicts an implementation of a CMOS-like NOR gate based on [18].

The main advantage of the approach described above is the re-utilization of existing knowledge and tools. Once a family of Boolean logic gates has been developed in a novel technology such as SET, existing gate level designs of (larger) components, such as

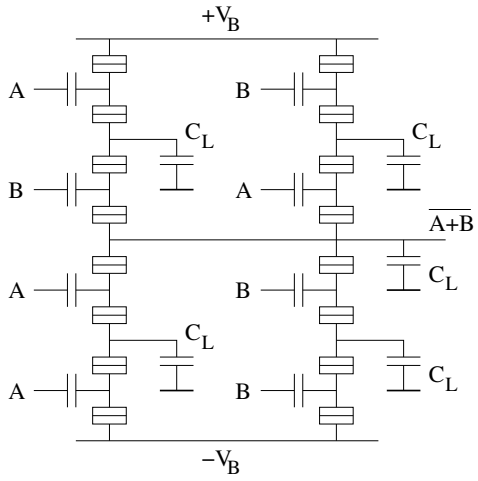

Fig. 3. CMOS-like NOR gate.

adders, multipliers, etc., can be realized in a straightforward manner. Equally important, existing design tools can be ported at very little cost and effort.

The main disadvantage of this approach is induced by the fact that usually a technology is most likely not utilized to its full potential when it is mold to mimic an existing technology. Focusing on SET, the CMOS-like design style has the following disadvantages. First, the designs only operate correctly when the current though an "open" transistor consists of a large number of electrons. Given that electron tunnelling is a sequential process, this is obviously a far slower process then the transport of only one electron through the same junction. Second, the "closed" transistor is not completely closed, resulting in a static current and a dramatic increase in power consumption.

Thus the logical next step would be to limit the charge transport through open transistors to just 1 electron, and to design the circuits such that closed transistors are completely closed. This results in the principle of Single Electron Encoded Logic (SEEL), in which the Boolean logic values 0 and 1 are encoded as a net charge of $0e$ and $1e$ on the circuit's output node. However, when the SEEL approach is applied to converted CMOS cells with multiple p-type or n-type transistors in series, the circuits will no longer operate correctly, as clarified by the following example. Assume a series of 2 p-type transistors, of which the one bordering the load capacitor is open while the other one is closed. This situation will result in the removal of 1 electron from the load capacitor, resulting in an incorrect "high" output. Thus when the circuit parameters are properly adjusted the inverter circuit itself will to operate correctly under a SEEL regime but no other CMOS alike SET Boolean gate will. This implies that CMOS type SET logic must encode the Boolean logic values 0 and 1 as "few" and "many" electron charges. We can therefore conclude that CMOS-type SET logic cannot efficiently utilize the SET features. In the next section we discuss a different design style based on SET based threshold logic gates that can operate according to the SEEL paradigm.

4. SINGLE ELECTRON ENCODED LOGIC

Threshold Logic Gates (TLG) are devices which are able to compute any linearly separable Boolean function given by:

$$F(X) = sgn\{\mathcal{F}(X)\} = \begin{cases} 0 & \text{if } \mathcal{F}(X) < 0 \\ 1 & \text{if } \mathcal{F}(X) \geq 0 \end{cases} \quad (6)$$

$$\mathcal{F}(X) = \sum_{i=1}^{n} \omega_i x_i - \psi, \quad (7)$$

where x_i are the n Boolean inputs and w_i are the corresponding n integer weights. The TLG performs a comparison between the weighted sum of the inputs $\Sigma_{i=1}^{n} \omega_i x_i$ and the threshold value ψ. If the weighted sum of inputs is *greater then or equal to* the threshold, the gate produces a logic 1. Otherwise the output is a logic 0.

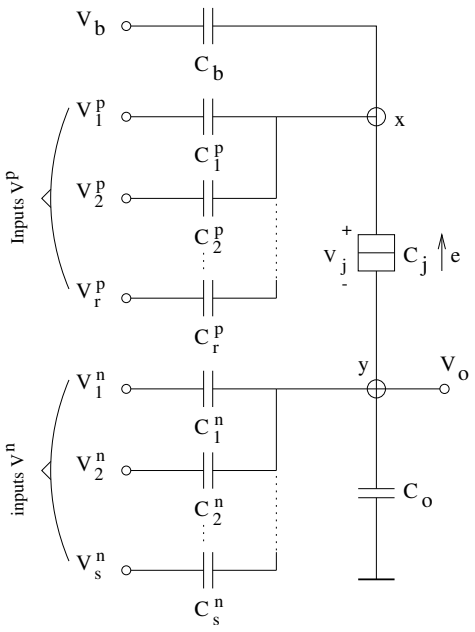

Fig. 4. The n-input linear threshold gate.

As stated in Section 2, a SET tunnel junction requires a minimum voltage $|V_j| \geq V_c$ in order for a tunnel event to occur. This critical voltage V_c acts as a naturally occurring threshold ψ with which the junction voltage V_j is compared. If we add capacitively coupled inputs to the circuit nodes on either side of the tunnel junction, the inputs will make a positively or negatively weighted contribution to the voltage across this junction (depending on the sign definition of V_j).

Similarly, we can add a capacitively coupled biasing voltage in order to adjust the threshold to the desired value. This approach resulted in the generic SEEL TLG implementation [21] as displayed in Figure 4.

In this figure, the input signals $V^p = \{V_1^p, V_2^p, \ldots, V_r^p\}$ are weighted by their corresponding capacitors $C^p = \{C_1^p, C_2^p, \ldots, C_r^p\}$ and added to the voltage across the tunnel junction. The input signals $V^n = \{V_1^n, V_2^n, \ldots, V_r^n\}$ are weighted by their corresponding capacitors $C^n = \{C_1^n, C_2^n, \ldots, C_r^n\}$ and subtracted from the voltage across the tunnel junction. The biasing voltage V_b, weighted by the capacitor C_b, is used to adjust the gate threshold to the desired value ψ. If $sgn\{V_j - V_c\} = 1$, a single electron is transported from node y to node x, which results in a high output. The resulting threshold function calculated by the circuit is:

$$\mathcal{F}(X) = C_\Sigma^n \Sigma_{k=1}^r C_k^p V_k^p - C_\Sigma^p \Sigma_{l=1}^s C_l^n V_l^n - \psi \quad (8)$$

$$\psi = \frac{1}{2}(C_\Sigma^p + C_\Sigma^n)e - C_\Sigma^n C_b V_b, \quad (9)$$

where $C_\Sigma^p = C_b + \Sigma_{k=1}^r C_k^p$ and $C_\Sigma^n = C_o + \Sigma_{l=1}^s C_l^n$. The SET TLG allows for both positive and negative weights and thus can potentially be used to calculate any threshold function in a single gate. We note here that this is a very important TLG feature as schemes that allows for positive weights only may results in less efficient implementations of algorithms [22].

The discussed TLG is a passive SET circuit, as it solely consists of passive elements (a tunnel junction and capacitors). When networks of passive SET circuits are constructed, strong crosstalk effects occur, which can result in incorrect behavior. These crosstalk effects are for a large part due to the charge transport inside gates which switch output values. The second source of crosstalk is due to supply voltage crosstalk. Given that the supply voltage is a constant signal, these crosstalk effects can be compensated for by adjusting the circuit parameters. This does unfortunately not hold true for the voltage fluctuations due to switching activity. As demonstrated in [23] sufficient buffering between different TLGs can alleviate all crosstalk effects and buffered TLGs can be utilized as building blocks for larger networks. Buffering can be achieved by the CMOS-like inverter depicted in Figure 2 which was modified to operate according to the SEEL paradigm [24].

Given that the basic Boolean logic functions AND, OR, NAND and NOR can be specified in the form of Equations (6,7), we can implement n-input AND, OR, NAND and NOR gates as instances of the threshold gate circuit. Limiting the discussion to 2-input gates only, the threshold gate computations corresponding to the previously mentioned Boolean functions are:

$$AND(a,b) = sgn\{a+b-2\} \quad (10)$$

$$OR(a,b) = sgn\{a+b-1\} \quad (11)$$

$$NAND(a,b) = sgn\{-a-b+1\} \quad (12)$$

$$NOR(a,b) = sgn\{-a-b\} \quad (13)$$

Each of the above threshold equations can be implemented by a single buffered TLG. Figure 5 for example depicts an implementation of the NOR gate. We can thus design a family of Boolean logic based on the buffered TLG. Moreover, threshold logic gates are more powerful than Boolean gates and this generally results in a reduction of the number of required gates and logic levels [22].

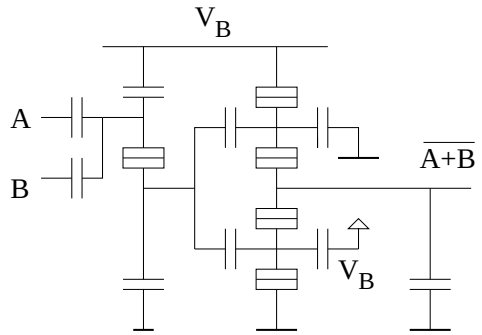

Fig. 5. Buffered TLG-based NOR gate.

The main advantage of the buffered TLG is the increased utilization of the specific property of the SET technology, e.g., the ability to control the transport of individual electrons. This potentially results in reduced delay and power consumption. An additional benefit is a significant reduction of the number of circuit elements that are required to implement the standard Boolean logic functions. For example the CMOS-like NOR gate example in Figure 3 requires 25 circuit elements whereas the same NOR gate but now designed in SEEL as depicted in Figure 5 requires only 14 circuit elements which indicates an area reduction of about 40 %. Also, by utilizing the SET TLG approach, all the Boolean and/or Threshold logic schemes for the computation of arithmetic functions can be potentially implemented with no major changes in the paradigm.

The main disadvantage is the increased sensitivity to errors. Given that output signals are encoded as just 1 electron, a single erroneous tunnel event (for example due to thermally induced tunnelling or co-tunnelling) will result in an incorrect output signal. This places additional constraints on the design process, as one must ensure that the error probability remains within acceptable bounds.

Although the SEEL TLG based approach better utilizes the SET technology due to an efficient information encoding it does not yet use the full potential of

SET. While SEEL is still based on Boolean variables the majority of computational and storage logic is intended for multi-bit variables (e.g., n-bit adders, registers, etc.). Thus a paradigm that can operate directly on such operands will potentially lead to more effective computation. Given that in SET technology it is possible to control the number of transported electrons, we can further attempt to improve efficiency by encoding n-bit operands directly as the number of electrons stored at a specific circuit location. Once integer values have been encoded as a number of electrons, we can perform arithmetic operations directly in electron charges. This reveals a broad range of novel computational schemes, which we generally refer to as electron counting. This approach is discussed in detail in the next section.

5. ELECTRON COUNTING LOGIC

In the this section we assume binary encoded n-bit operands, $A = (a_0, a_1, \ldots, a_{n-1})$ and $B = (b_0, b_1, \ldots, b_{n-1})$ and discuss electron counting schemes to compute the result of their addition and multiplication. The basic idea behind the method [25] is first to convert the operands from digital to charge representation, add/subtract them in charge format, and convert the result back to binary digital representation. Before describing the concept in more details we briefly discuss the two types of electron counting building blocks which are required for these schemes.

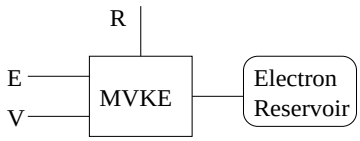

Fig. 6. The MVke block.

The $MVke$ block displayed in Figure 6 is an electron counting building block with which a variable number of electrons can be added to or removed from a charge reservoir. Thus it can be utilized to move electrons within a SET circuit. Typically, a charge reservoir is a circuit node that is capacitively coupled to ground. A charge reservoir with a capacitance C_r containing a charge of $V \times e$ is therefore equivalent to a voltage source $U = \frac{V \times e}{C_r}$. The $MVke$ block behavior is controlled via two Boolean input signals R (reset) and E (enable) and it operates as follows: if $R = 0$, a charge of $V \times k \times e$, where k is a positive integer constant and V is an integer (variable) value, is moved to the electron reservoir when the block is triggered by $E = 1$. Note that V could either be another charge reservoir containing $V \times e$ electrons or an equivalent voltage source. For positive V values the $MVke$ block is in "add" mode (adding charge to the reservoir) while for negative V values the $MVke$ block is in "remove" mode (removing charge from the reservoir). The $MVke$ block has a dynamic logic behavior thus before a new charge transport can be initiated it has to be reset and this can be achieved by $R = 1$.

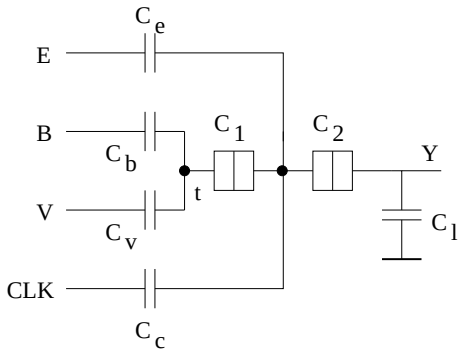

Fig. 7. $MVke$ block implementation.

A possible implementation of the $MVke$ block is displayed in Figure 7. The circuit operates as follows. If a clock pulse CLK arrives, the SET transistor (C_1 and C_2) is opened if and only if $E = 1$. When the transistor opens, $V \times k \times q_e$ charge is added to the load capacitor C_l. As a result of this charge transport, an opposite charge $-V \times k \times e$ is stored on node 't'. The voltage resulting from this opposite charge cancels the effect of voltage source V, inhibiting further charge transport. The circuit is biased via the the DC input B. Given that the capacitor C_v acts as a weight factor for V, the desired multiplication constant value k can be adjusted by changing the value of C_k.

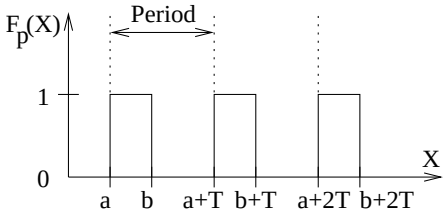

Fig. 8. Period symmetric function $F_p(X)$.

A Boolean symmetric function $F_s(x_0, x_1, \ldots, x_{n-1})$ is a Boolean function for which the output depends on the sum of the inputs $X = \sum_{i=0}^{n-1} x_i$. A Periodic Symmetric Function (PSF) $F_p(X)$ is a symmetric function for which $F_p(X) = F_p(X + T)$, where T is the period. Any PSF can be completely characterized by T, the value of its period, and a,b, the values of X corresponding with the first positive transition and the first negative transition, as displayed in Figure8. Efficient implementation of periodic symmetric functions is quite important as many functions involved in computer arithmetic

computations, e.g., parity, belong to this class of functions. The PSF block is an electron counting building block that can evaluate a PSF, where it is assumed that the sum of the inputs X is charge encoded and stored in a charge reservoir.

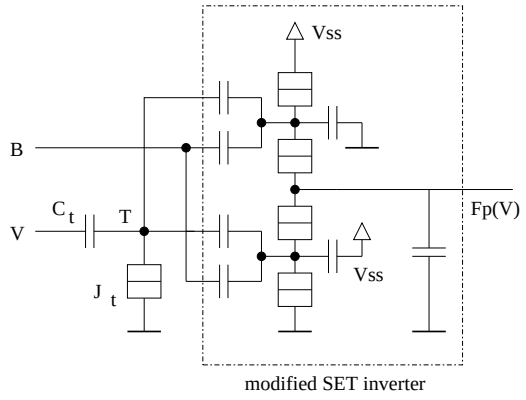

Fig. 9. PSF block implementation.

A possible implementation of the PSF block is displayed in Figure 9. The circuit operates as follows. The capacitor C_t and junction J_t form an electron trap structure. The charge encoded input value V serves as the input to the electron trap. Given than the output of an electron trap circuit has a periodic behavior, the electron trap's output node T has a periodic response to input V. The voltage on node T is capacitively added to a biasing voltage B and then serves as input for a SET inverter. The SET inverter behaves as a literal gate and transforms its input signal (within a limited range) to either logic 0 of logic 1.

Given these two types of building blocks we can now discuss electron counting schemes for addition and multiplication. Assuming binary operands, the first step in any electron counting process is to convert a binary integer value X to its discrete analog equivalent Xe using a Digital to Analog Converter (DAC) which follows the general organization of the one introduced in [26]. As described earlier, the $MVke$ block in Figure 7 can be utilized to add/remove a number of electrons to/from a charge reservoir. When multiple such $MVke$ blocks operate in parallel on the same charge reservoir, electrons can be added to the reservoir in parallel. More specific, to convert an operand $X = (x_0, x_1, \ldots, x_{n-1})$, each bit x_i, $i = 0, 1, \ldots, n-1$ is connected to the E input of an $MVke$ block that has the V input hardwired to a bias potential that induces a $V \times k$ value equal with 2^i. Therefore, the operand X can be encoded as $\sum_{i=0}^{n-1} x_i 2^i e$ at the cost of n $MVke$ blocks in "add" mode. Thus this DAC scheme has an $O(n)$ asymptotic complexity in terms of the number of required building blocks.

Given the $MVke$-DAC encoding scheme described above, the addition operation can be implemented in a straightforward manner. The addition of two n-bit operands A and B can be embedded in the conversion process if the operands are converted into charge format, via a total of $2n$ $MVke$ blocks in "add" mode that share the same charge reservoir. Once the result corresponding to the addition is available in the charge reservoir as a charge Ye, where $Y = A + B$, we need to convert this result back to a digital format in order to finalize the computation process. To achieve this an Analog to Digital Conversion (ADC) process is required. In the following we describe an ADC circuit based on the PSF block.

If N is the maximum number of extra electrons that can be present in the result charge reservoir, $m = 1 + [\log N]$ bits are required to represent this value in binary format. Then, following the base 2 counting rules, any ADC output bit s_i, $i = 0, 1, \ldots, [\log N]$ is equal to 1 inside an interval that includes 2^i consecutive integers, every 2^{i+1} integers, and 0 otherwise. Thus each bit s_i can be described by a periodic symmetric function with period 2^{i+1}. As consequence of this property each output bit s_i can be computed by a PSF block that had been adjusted in order to have a transfer function that copies the periodic symmetric function required for the bit position i. Thus we can implement an m-bit ADC using m PSF blocks (the PSF applied at bit position i is tuned to exhibits the periodic transfer function corresponding to that s_i bit) that operate in parallel on a charge reservoir. Given that we are addressing the particular case of n-bit operand addition, such that $m = n+1$, the cost of the required ADC circuit is in the order of $O(n)$.

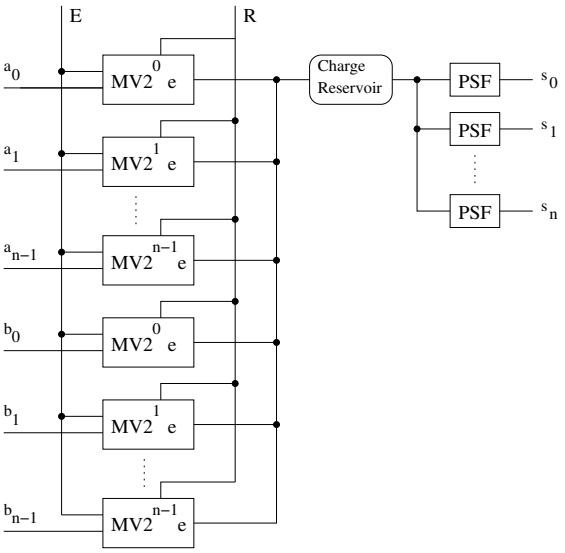

Fig. 10. Organization of n-bit addition circuit.

Summarizing, the electron counting based addition of two n-bit operands can be implemented with a

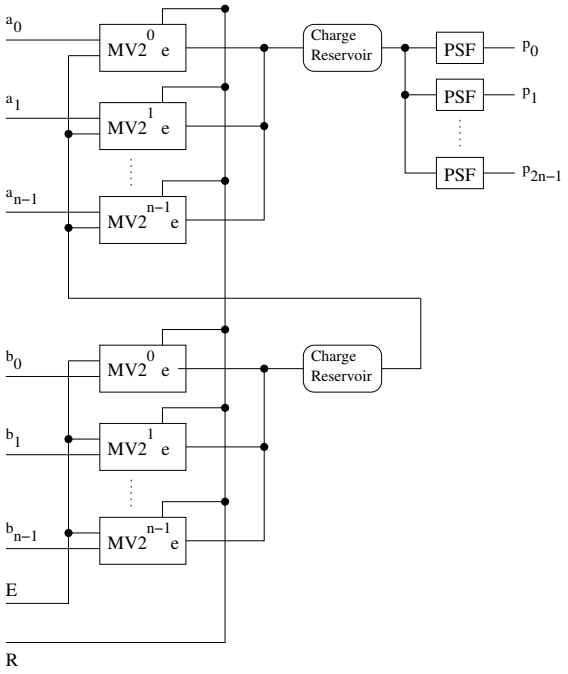

Fig. 11. Organization of n-bit multiplication circuit.

depth-2 SET network composed out of $3n+1$ electron counting building blocks, then with an $O(n)$ asymptotic complexity measured in terms of building blocks. The overall organization of the circuit is depicted in Figure 10. We note here that in the Figure, the value k of the $MVke$ blocks has been drawn inside the block to suggest that it was implemented by properly adjusting the corresponding circuit parameter(s), while all inputs V have been fixed to the equivalent of a charge reservoir with $1e$ charge. Even though the proposed addition scheme is primarily meant for addition/subtraction, it has a broader scope. Some of the alternative utilizations include n-bit subtraction, n-bit parity functions, multi-operand addition and $n|\log n$ counters.

We next discuss an electron counting multiplication scheme that follows to some extent the paradigm we introduced for addition. Assume we have the input operands A and B and we want to compute $P = A \times B$. As indicated in [25] a straightforward application of the electron counting principle to the multiplication produces a depth-3 network with an overall asymptotic complexity measured in terms of circuit elements in the order of $O(n^2)$. A more effective implementation is also possible if one make use of the ability to transport a variable number of electrons to/from a charge reservoir exhibited by the $MVke$ structure depicted in Figure 6. Such a block can transport $V \times k$ electrons when k is a built in constant (can be changed via circuit parameter(s)) and V is a variable specified by the content of a charge reservoir.

The basic idea behind the scheme is again to add a charge Pe to a charge reservoir and to utilize an ADC structure to obtain the binary representation of the product P. The general organization of the proposed multiplication circuit is depicted in Figure 11. Again, the value k of the $MVke$ blocks has been drawn inside the blocks themselves to suggest that that k value was implemented inside the block by properly adjusting the corresponding circuit parameter(s). The scheme is utilizing a clock for synchronization purposes[1] and the computation process can be described as follows: First, on the positive clock value, a number of electrons corresponding to the value of the B operand, i.e., $\sum_{i=0}^{n-1} b_i 2^i$, are added to the corresponding charge reservoir. This is achieved with n $MVke$ blocks each of them assuming as inputs the b_i bit and having the V input hardwired to the equivalent of a charge reservoir with $1e$ charge, such that $V \times k = 2^i$. Second, on the negative clock value, a charge of $A \times Be$ is added to the other charge reservoir. This is achieved with n $MVke$ blocks assuming as inputs the a_i bits and the analog value present on the charge reservoir processed in the previous computation step. As each $MVke$ block in this stage contributes $a_i \times 2^i \times B$ electrons, a final charge of $\sum_{i=0}^{n-1} a_i 2^i \times Be$, i.e, $A \times Be$ is present in the output charge reservoir when second step is completed. Last, the value on the output charge reservoir is converted to digital with $2n-1$ PSF blocks.

This scheme still implies a depth-3 network but requires $2n$ $MVke$ blocks and $2n-1$ PSF blocks, thus the overall asymptotic complexity is reduced to $O(n)$.

The main advantage of electron counting logic is the potential to encode an n-bit binary number as a single variable. First, this can result in a large reduction of area for memory cell arrays as well as for arithmetic circuits. Second, it can potentially result in reduced delay for arithmetic operations as its utilization eliminates the carry chain that usually determines the critical path of such operations. Although the addition and multiplication schemes described above assume n-bit calculation, we can assume that for practical situations a limited number of bits can be encoded as a single variable. If this is the case we can combine electron counting with traditional approaches in high radix computation schemes. If for example we assume radix 16 calculation (4 bits per digit), the digit operations can be done in the electron counting paradigm while the carry between digit positions can be handled with traditional schemes. Roughly speaking this reduces the carry chain of arithmetic operations by a factor 4.

The main disadvantage of electron counting logic is the need for additional signal amplification. Given that the charge present in a charge reservoir can potentially

[1]We assume here a level triggered behavior but the scheme can work with edge triggered policy as well.

vary over a large range, the capacitance of the charge reservoir should be relatively large in order to reduce feedback to the attached electron counting building blocks. This also implies that the feed forward signal is relatively small and that it requires amplification. As this signal is non-Boolean, a simple buffer such as an inverter cannot be utilized. Instead, it will require the presence of OpAmp-like buffers. It may however be possible to delay signal amplification until a charge encoded result is converted into a binary number, such that an inverter chain is sufficient for signal level restoration.

Concluding, the electron counting logic approach further increase the efficiency at which the SET technology is utilized. However, this comes at the price of loss in signal strength. A potential interesting application for this encoding scheme is the implementation of memory cell arrays, as a large number of memory cells can utilize a single DAC and ADC.

6. DISCUSSION

Single Electron Tunnelling (SET) is a future technology candidate that can be seen as one of the potential successors of (C)MOS. It's main advantages are as follows. First, the tunnel junction by itself is technology independent as its fabrication only requires a gap in a conducting material. This material can be a conventional metal strip, but also an advanced material such as a carbon nanotube. SET behavior is determined by a fundamental physical phenomenon, e.g., the discrete nature of charge transport which occurs through tunnel junctions and the Coulomb blockade effect, the energy barrier that must be overcome in order to make this transport possible. Second, unlike MOS, SET has the potential to be be scaled down to molecular dimensions due to the simplicity of the tunnel junction. Third, given the ability to control charge transport at a scale of individual electrons, and the potential to design circuits operating with such small scale charge transport, the SET technology offers the potential for ultra low power consumption. Given that such SET circuits will likely be constructed with feature sizes in the order of 1 nm, the number of devices per cm^2 might be in the order of 10^{11} or more. This implies that ultra low power is critical for the success of any nanometer-scale technology.

The main problems associated with the SET technology are as follows. First, the energy scale at which charge transport is controlled is the Coulomb energy. In order to accurately control charge transport, one must ensure that other forms of energy present in the circuit, including the thermal energy, are much smaller then the Coulomb energy. The Coulomb energy is inverse proportional to the size of the capacitors in the circuit. In order to operate at room temperature these capacitors must be in the order of 10^{-18} F or less. At the present state-of-the-art of lithographic technology, this is not possible in a commercial setting and can only be achieved in special laboratories. Second, given that SET circuits operate at a charge transport scale of 1 electron, the circuits are extremely sensitive to charge pollution in the substrate. If a single charge particle is present near a tunnel junction, it can severely alter the junctions critical voltage V_c, thereby resulting in switching errors. All SET schemes presented in here are susceptible to this random background charge effect and will fail to operate reliably if such charge is present. However, with improved manufacturing capabilities this problem might be reduce such that error correction schemes can become viable.

In an attempt to demonstrate that emerging devices like SET can be effectively used only if their specific behavior is explicitly utilized at the circuit and system level we discussed three different SET logic design styles. Some of their advantages and disadvantages are summarized in the following.

The CMOS-like design styles required the largest area in terms of circuit elements. Also, its power consumption is the largest as it not only transports a larger amount of charge but also consumes static current. The delay of Boolean gates designed in the CMOS-like style is typically in the order 10 ns or more. For example the NOR gate example in Figure 3, with $C_L = O(10^{-15})$ and $R_t = O(10^5)$ as suggested in [18] one can evaluate a gate delay of about 10 ns. The same NOR gate but now designed in SEEL as depicted in Figure 5 and with the circuit parameters considered in [24] has a delay of about 1 ns.

The SEEL design style requires less area, consume less power (in the order of 1 meV per output switching) and have less delay (in the order of 1 ns). Additionally, the SEEL based approach has the added benefit of being able to directly implement threshold logic based circuits. For example, a TL based full adder implementation only requires 2 TLGs, while its Boolean counterpart requires about 10 gates.

The electron counting based approach is novel and more research is required in order to be able to characterize the proposed schemes in terms of area, delay or power. Our recent research has demonstrated the potential benefits this novel paradigm might have in terms of required area and delay for addition related operations. However we do not yet have sufficient simulation data to evaluate some practical cases. We anticipate that the delay of the electron counting basic building blocks might be larger than the one of the SEEL gate but we expect that the very shallow networks produced by the electron counting paradigm can compensate for this. For example when considering the n-bit addition any fast structure based on carry lookahead or another similar technique [27] requires a delay in the order of $O(\log n)$ whereas the electron

counting produces a depth-2 network. Wether or not this is enough to compensate for the larger delay of the block and/or for other practical issues that might limit the number of bits that can be accommodated into a charge reservoir it is still an open issue and subject of future research. However, we expect that the required area for addition related operations implemented in the electron counting paradigm will be lesser than the one required by SEEL implementation based on Boolean and/or threshold gates. When assuming that signal amplification can be achieved with an inverter chain, the power consumption might be comparable to the SEEL approach but this issue also requires more future investigations.

7. CONCLUSIONS

It is generally accepted that fundamental physical limitations will eventually inhibit further (C)MOS feature size reduction. Several emerging nano-electronic technologies with greater scaling potential, such as Single Electron Tunneling (SET), are currently under investigation. Each of these exhibit their own switching behavior, resulting in new paradigms for logic design and computation. This paper presented a case study on SET based logic. We analyzed and compared three different SET designs styles. First, SET transistor based designs that mimic conventional CMOS. Second, single electron threshold logic based on the voltage threshold of SET tunnel junctions. Third, electron counting logic based on the direct encoding of integers as charge and performing computation by charge transport.

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