Digital to analogue converter based on single-electron tunnelling transistor

C.H. Hu, S.D. Cotofana and J.F. Jiang

Abstract: A digital to analogue converter (DAC) based on a single-electron tunnelling transistor (SETT) is proposed. The proposed scheme fully utilises the Coulomb blockade effect and only a SETT and n + 1 capacitors are necessary for an *n*-bit DAC implementation. Using this scheme, a 4-bit DAC is demonstrated by means of simulation.

1 Introduction

Current progress in microelectronics is pushing metal-oxide-semiconductor field-effect-transistor (MOSFET) dimensions towards the 10 nm gate-length limits, which is expected to be the basic physical limit of conventional MOSFETs. To ensure further feature-size reduction, one possible solution is to develop single-electron tunnelling (SET) devices. In fact, SET devices and circuits have been developed rapidly in both theory and experiment because the essential nanofabrication techniques have become available during the past two decades [1–4]. The fundamental principle of SET devices and circuits is the Coulomb blockade, which was first observed and studied by Gorter [5]. SET circuits are promising for future large-scale integrated circuits (LSIs) because of their ultra low power and ultra high density. Several SET circuits have been proposed in the literature: SET memories [6], inverters [1, 7], pumps [8], majority gates [9], threshold gates [10], analogue to digital conversion [11, 12], latching switch [13], etc. Furthermore, some hybrid SET transistor (SETT)/FET circuits have also been proposed; for example, hybrid SETT/FET memories [13] and multiple-valued logic [11]. However, only a few circuits have fully explored the inherent SET characteristics, such as Coulomb blockade and Coulomb oscillation, up to now. In this paper we propose a SETT based digital to analogue converter (DAC) structure that exploits the inherent SET characteristics. First we analyse the behaviour of a SETT-based multiple-value *k* electron (MVke) block, with which a variable number of electrons *ke* can be added to the output node one by one. Based on the MVke block, we propose a SETT-based DAC structure that fully utilises the Coulomb blockade effect and requires only one SETT and *n+1* capacitors for an *n*-bit DAC implementation.

IEE Proceedings online no. 20040992

doi:10.1049/ip-cds:20040992

Paper first received 16th October 2003 and in revised form 11th June 2004. Originally published online: 17th September 2004

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2 Background

A tunnel junction can be considered to approximate a leaky capacitor. According to orthodox theory [2], we can calculate the critical voltage V_c, which is the minimum voltage across the tunnel junction to make an electron tunnel possible, as

$$V_c = \frac{e}{2(C_e + C_j)} \tag{1}$$

where $e = 1.602 \times 10^{-19}\,C$, C_j is the tunnel junction capacitance and C_e is the equivalent capacitance of the remainder of the circuit as viewed from the tunnel junction's perspective.

For zero temperature or ultralow temperature approximation, the tunnel junction acts as a capacitor if $|V_j| < V_c$, and an electron will tunnel across the junction if and only if $|V_j| \geq V_c$. This phenomenon is also called Coulomb blockade.

SETT is similar to a conventional MOSFET, but with a small conducting island embedded between two tunnel junctions [2] instead of the usual inversion channel. Distinguished by the type of circuit element that is connected to the island, SETTs can be classified as follows: C-SETT if the circuit element is a capacitor (as depicted in Fig. 1), R-SETT if the circuit element is a resistor, and RC-SETT if the circuit element is a resistor and a capacitor in series. In this paper we consider only C-SETT structures,

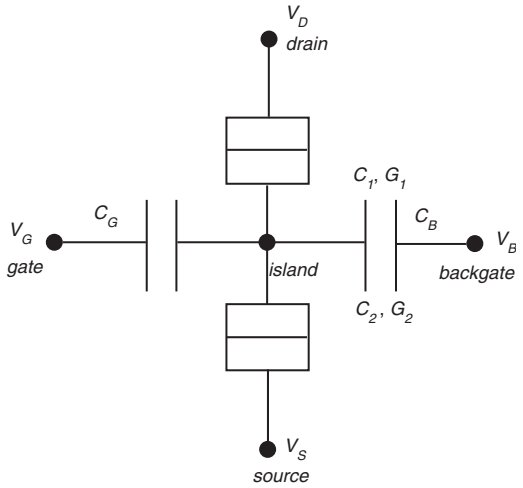

Fig. 1 *Schematic of C-SETT*

thus, for simplicity, we refer to C-SETT as SETT. For the tunnel junctions in Fig. 1, the tunnel conductance is G_1 and G_2, the junction capacitance is C_1 and C_2, respectively, and the gate and backgate capacitance is C_G and C_B, respectively. The drain, source, gate and backgate voltage is V_D, V_S, V_G and V_B, respectively. For proper operation of the SETT, both G_1 and G_2 should be much smaller than $1/R_Q$, where $R_Q = h/e^2 \approx 25.8$ kΩ is the quantum unit of resistance. Furthermore, we assume that the charge energy is dominant over the thermal fluctuation, that is $e^2/2C$ is much greater than k BT, where C is the total capacitance between the island and environment, and is equal to the sum of C_1, C_2, C_G and C_B in the case of SETT.

In the next Section, we utilise the Coulomb blockade effect and analyse the SETT-based MVke block.

3 Analysis of a SETT-based MVke block

The MVke block introduced in [14], depicted in Fig. 2, is a basic block with which a variable number of electrons ke can be added to the output node where k is determined by input voltage V_{in}. It is composed of a SETT with its drain capacitively coupled to V_{in}, its source capacitively coupled to ground, and its source regarded as the output node. Moreover, both V_G and V_B are utilised as control signals. This Section presents a detailed analysis of the behaviour of this SETT-based MVke block.

First, we introduce the following notation: for junction 1,

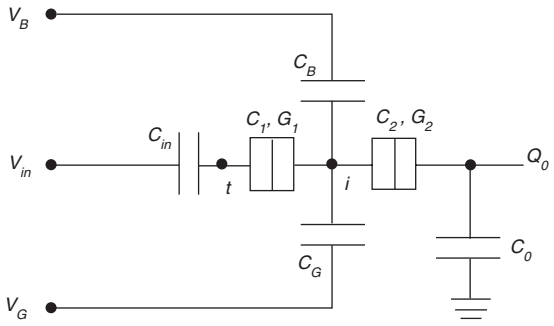

Fig. 2 *Schematic of SETT-based MVke block*

V_{c1} is junction 1's critical voltage, $V_{j1}(V_G)$, $V_{j1}(V_B)$, $V_{j1}(Q_t(ke))$, $V_{j1}(Q_i(ke))$ and $V_{j1}(Q_o(ke))$ is the voltage effects on junction 1 by V_G, V_B, $Q_t(ke)$, $Q_i(ke)$ and $Q_o(ke)$, respectively. $Q_t(ke)$, $Q_i(ke)$ and $Q_o(ke)$ are the number of electrons present at node 't', the island node 'i' and the output node, respectively, where k is a variable. Moreover, we introduce an operator to describe the capacitance of two capacitors in series for convenience:

$$C_a||C_b = \frac{C_a \cdot C_b}{C_a + C_b} \tag{2}$$

Then, for junction 1, the following holds true:

$$V_{c1} = \frac{e}{2(C_1 + C_{in}||(C_B + C_G + C_2||C_o))} \tag{3}$$

$$V_{j1}(V_{in}) = \frac{C_{in}V_{in}}{C_{in} + C_1||(C_B + C_G + C_2||C_o)} \cdot \frac{C_B + C_G + C_2||C_o}{C_1 + C_B + C_G + C_2||C_o} \tag{4}$$

$$V_{j1}(V_G) = \frac{-C_G V_G}{C_1||C_{in} + C_B + C_G + C_2||C_o} \cdot \frac{C_{in}}{C_1 + C_{in}} \tag{5}$$

$$V_{j1}(V_B) = \frac{-C_B V_B}{C_1||C_{in} + C_B + C_G + C_2||C_o} \cdot \frac{C_{in}}{C_1 + C_{in}} \tag{6}$$

$$V_{j1}(Q_t(ke)) = \frac{ke}{C_{in} + C_1||(C_B + C_G + C_2||C_o)} \cdot \frac{C_B + C_G + C_2||C_o}{C_1 + C_B + C_G + C_2||C_o} \tag{7}$$

$$V_{j1}(Q_i(ke)) = \frac{-ke}{C_1||C_{in} + C_B + C_G + C_2||C_o} \cdot \frac{C_{in}}{C_1 + C_{in}} \tag{8}$$

$$V_{j1}(Q_o(ke)) = \frac{-ke}{C_o + C_2||(C_1||C_{in} + C_B + C_G)} \cdot \frac{C_2}{C_2 + C_1||C_{in} + C_B + C_G} \cdot \frac{C_{in}}{C_1 + C_{in}} \tag{9}$$

Applying similar reasoning to junction 2, we derive

$$V_{c2} = \frac{e}{2(C_2 + C_o||(C_B + C_G + C_1||C_{in}))} \tag{10}$$

$$V_{j2}(V_{in}) = \frac{C_{in}V_{in}}{C_{in} + C_1||(C_B + C_G + C_2||C_o)} \cdot \frac{C_1}{C_1 + C_B + C_G + C_2||C_o} \cdot \frac{C_o}{C_2 + C_o} \tag{11}$$

$$V_{j2}(V_G) = \frac{C_G V_G}{C_1||C_{in} + C_B + C_G + C_2||C_o} \cdot \frac{C_o}{C_2 + C_o} \tag{12}$$

$$V_{j2}(V_B) = \frac{C_B V_B}{C_1||C_{in} + C_B + C_G + C_2||C_o} \cdot \frac{C_o}{C_2 + C_o} \tag{13}$$

$$V_{j2}(Q_t(ke)) = \frac{ke}{C_{in} + C_1||(C_B + C_G + C_2||C_o)} \cdot \frac{C_1}{C_1 + C_B + C_G + C_2||C_o} \cdot \frac{C_o}{C_2 + C_o} \tag{14}$$

$$V_{j2}(Q_i(ke)) = \frac{ke}{C_1||C_{in} + C_B + C_G + C_2||C_o} \cdot \frac{C_o}{C_2 + C_o} \tag{15}$$

$$V_{j2}(Q_o(ke)) = \frac{-ke}{C_o + C_2||(C_1||C_{in} + C_B + C_G)} \cdot \frac{C_1||C_{in} + C_B + C_G}{C_2 + C_1||C_{in} + C_B + C_G} \tag{16}$$

A possible implementation of the MVke block can be derived as follows. When V_{in} is zero and both V_G and V_B are high (we choose $V_G = V_B = e/4C_G$ as the high level, where usually $C_B = C_G$, and $V_G = V_B = 0$ as the low level), junction 1 is closed due to the reverse threshold $-V_{c1}$ and junction 2 is closed due to the forward threshold V_{c2}. When V_{in} increases from zero, junction 1 is closed due to the Coulomb blockade effect and junction 2 opens first when V_{in} reaches the value V_{TH} and one electron is transferred to the output node. Then junction 1 opens and one electron is transferred to the island under the effect of $V_{j1}(Q_i(-e))$

and $V_{j1}(Q_o(e))$. Then, under the effect of $V_{j1}(Q_t(-e))$, $V_{j1}(Q_o(e))$ and $V_{j2}((Q_t(-e)$, $V_{j2}(Q_o(e))$, both junction 1 and junction 2 are closed until V_{in} reaches the value $V_{TH}+V_T$ when junction 2 opens again and a second electron is transferred to the output node. As indicated in Fig. 3, V_T is the amount by which the input voltage may increase without any change in the number of output charges present at the output node when both V_G and V_B are high. The rest of the process follows the same operation paradigm. In the situation when one of V_B, V_G or both are low, both junction 1 and 2 are closed due to Coulomb blockade, regardless of V_{in}.

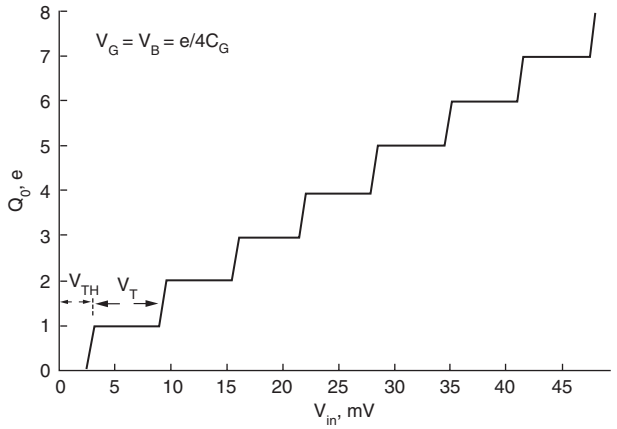

Fig. 3 *Input–output characteristic of SETT-based MVke block*

In order to arrive at a final state with k ($k>0$) electrons in the output node, the circuit parameters have to fulfil the following constraints:

$$V_{j1}(V_B)+V_{j1}(V_G)+V_{j1}(V_{in})+V_{j1}(Q_t(-(k-1)e)) + V_{j1}(Q_o((k-1)e))<V_{c1} \tag{17}$$

$$V_{j2}(V_B)+V_{j2}(V_G)+V_{j2}(V_{in})+V_{j2}(Q_t(-(k-1)e)) + V_{j2}(Q_o((k-1)e))\geq V_{c2} \tag{18}$$

$$V_{j1}(V_B)+V_{j1}(V_G)+V_{j1}(V_{in}) + V_{j1}(Q_t(-(k-1)e)) + V_{j1}(Q_i(-e))+V_{j1}(Q_o(ke))\geq V_{c1} \tag{19}$$

$$V_{j2}(V_B)+V_{j2}(V_G)+V_{j2}(V_{in}) + V_{j2}(Q_t(-ke))+V_{j2}(Q_o(ke))<V_{c2} \tag{20}$$

$$V_{j1}(V_B)+V_{j1}(V_G)+V_{j1}(V_{in}) + V_{j1}(Q_t(-ke))+V_{j1}(Q_o(ke))<V_{c1} \tag{21}$$

From (11) and (18), we can deduce the input voltage threshold V_{TH}:

$$V_{TH}=\left[V_{c2}-\left(V_{j2}(V_B)+V_{j2}(V_G)\right)\right]\cdot\frac{C_2+C_o}{C_o}\cdot \frac{C_1+C_G+C_B+C_2||C_o}{C_1}\cdot\frac{C_{in}+C_1||(C_G+C_B+C_2||C_o)}{C_{in}} \tag{22}$$

and from (11), (14) and (16), the period V_T can also be deduced:

$$V_T=-\left[V_{j2}(Q_t(-e))+V_{j2}(Q_o(e))\right]\cdot\frac{C_2+C_o}{C_o}\cdot\frac{C_1+C_G+C_B+C_2||C_o}{C_1}\cdot\frac{C_{in}+C_1||(C_G+C_B+C_2||C_o)}{C_{in}} \tag{23}$$

When only one of V_B, V_G is high or both are low, the following constraints have to be satisfied:

$$V_{j1}(V_B)+V_{j1}(V_{in})<V_{c1} \tag{24}$$

$$V_{j2}(V_B)+V_{j2}(V_{in})<V_{c2} \tag{25}$$

$$V_{j1}(V_G)+V_{j1}(V_{in})<V_{c1} \tag{26}$$

$$V_{j2}(V_G)+V_{j2}(V_{in})<V_{c2} \tag{27}$$

$$V_{j1}(V_{in})<V_{c1} \tag{28}$$

$$V_{j2}(V_{in})<V_{c2} \tag{29}$$

And the maximum of k (k_{max}) is determined by the minimum k satisfying the following constraints.

$$V_{j1}(V_B)+V_{j1}(V_{in})\geq V_{c1} \tag{30}$$

$$V_{j2}(V_B)+V_{j2}(V_{in})\geq V_{c2} \tag{31}$$

$$V_{j1}(V_G)+V_{j1}(V_{in})\geq V_{c1} \tag{32}$$

$$V_{j2}(V_G)+V_{j2}(V_{in})\geq V_{c2} \tag{33}$$

$$V_{j1}(V_{in})\geq V_{c1} \tag{34}$$

$$V_{j2}(V_{in})\geq V_{c2} \tag{35}$$

$$V_{j1}(V_G)+V_{j1}(V_B)+V_{j1}(V_{in})+V_{j1}(Q_t(-(k-1)e)) + V_{j1}(Q_o((k-1)e))\geq V_{c1} \tag{36}$$

where

$$V_{TH}+(k-1)\cdot V_T<V_{in}<V_{TH}+k\cdot V_T$$

$$\text{that is } k=\left[\frac{V_{in}-V_{TH}}{V_T}\right]+1 \tag{37}$$

where we use the function $[x]$ to represent the maximum integer less than x.

As an example, we start with the following values for the capacitances in the circuit: $C_1 = C_2 = 0.1\ aF$, $C_B = C_G = 0.2\ aF$, $C_{in} = C_o = 150\ aF$, and we deduce that $V_{TH} =$ 2.671 mV, $V_T = 6.411$mV using (22) and (23), respectively; and $k_{max} = 25$, which is determined by (34) in this case. The input–output characteristic of this MVke block instance, obtained via simulation is depicted in Fig. 3, where the simulation tool used was SIMON [2]. The results calculated by the analysis method are identical with the simulation results.

4 SETT-based digital to analogue converter

The presented SETT-based MVke block can be used as a core building block to implement a DAC circuit. An n-bit DAC implementation based on the SETT-based MVke block is depicted in Fig. 4, where V_G is utilised as an enable signal, V_B as a clock signal, and C_{in} in the MVke block in Fig. 2 is replaced with n capacitors ($C_{in(i)}$) in order to

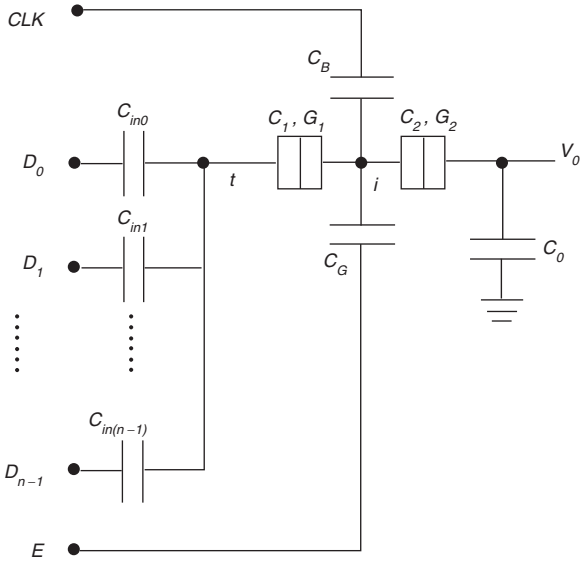

Fig. 4 *Implementation for n-bit SETT-based DAC*

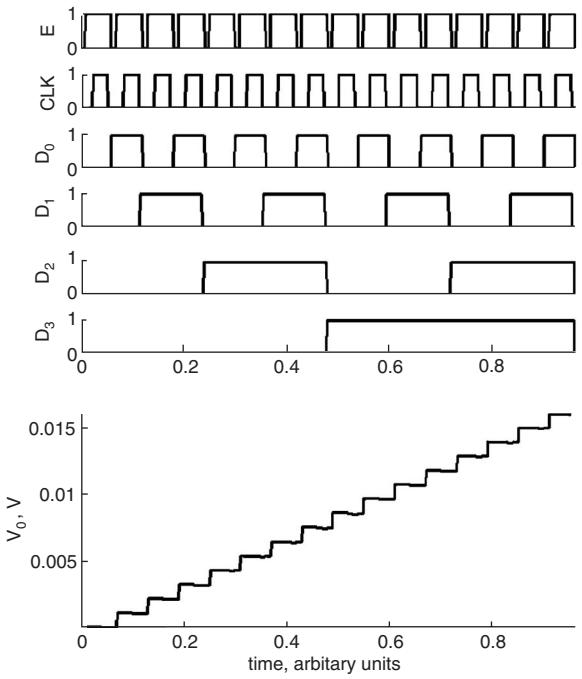

Fig. 5 *Simulation results for 4-bit SETT-based DA*

associate proper weight values to the DAC inputs. We have chosen

$$C_{in(i)} = \frac{2^i C_{in}}{2^n - 1} \quad i = 0, 1, 2 \ldots n-1$$

and in this way, if these input voltages work separately, we can deduce:

$$V_{TH(i)} = \frac{2^n - 1}{2^i} V_{TH} \tag{38}$$

$$V_{T(i)} = \frac{2^n - 1}{2^i} V_T \tag{39}$$

In order to choose the input voltage value to represent the logic '1' value, we can express the input voltage contribution of all the inputs in terms of the contribution of the input at the D_0 node. For proper DAC operation, the input voltage has to satisfy the following constraints.

$$V_{TH0} < V_{in} < V_{TH0} + V_{T0} \tag{40(1)}$$

$$V_{TH0} + V_{T0} < 2 \cdot V_{in} < V_{TH0} + 2 \cdot V_{T0}$$

(40(2–1))

$$V_{TH0} + (2^n - 2) \cdot V_{T0} < (2^n - 1) \cdot V_{in} < V_{TH0} + (2^n - 1) \cdot V_{T0} \tag{40(2^{n-1})}$$

And when $V_{T0} > V_{TH0}$, the group of inequalities above can be reduced to

$$\frac{1}{2^n - 1} V_{TH0} + \frac{2^n - 2}{2^n - 1} \cdot V_{T0} < V_{in} < \frac{1}{2^n - 1} V_{TH0} + V_{T0} \tag{41}$$

Using this scheme, we present a 4-bit DAC based on the SETT-based MVke block described in Section 3 and where the logic value '1' is chosen to be 95 mV (according to (41), V_{in} has to satisfy 92.43 mV < V_{in} < 98.84 mV). The simulation results are presented in Fig. 5, where the output voltage is approximately ke/C_o ($k = \sum_i 2^i \cdot D_i$). It is noticeable that the output voltage remains unchanged even when the enable signal and the clock signal become low until the next enable signal and clock signal become high. The simulation results demonstrate DAC performance only with monotonously increasing input voltage. In fact, the output has slightly different results when the input voltage decreases gradually. The reason is that, in this case, k electrons will be kept in the output node first, and then one by one transferred to node 't' as the input voltage decreases. That is junction 1 rather than junction 2 in the above-mentioned situation dominates the SETT turn-on (reverse tunnelling) in this case. This problem can easily be alleviated if a conversion with all the inputs set to zero is performed in order to reset the circuit before doing the targeted digital to analogue conversion.

5 Comparison

Generally speaking, when compared with previous SET-based DAC [15, 16] proposals, our scheme is compact and requires the least number of circuit components. For an n-bit DAC implementation, the one in [15] needs $3 \cdot (2^n – 1)$ tunnel junctions and $3 \cdot (2^n – 1) + 6$ capacitors; the one in [16] needs 7 tunnel junctions and $n+3$ capacitors, whereas our proposal needs only 2 tunnel junctions and $n+3$ capacitors.

Related to conversion speed, our proposal is potentially faster than the one in [16] as our scheme results in a shallower network. When compared with the approach in [15] our DAC is slower but this is quite natural as we transport the k electrons in a serial fashion whereas the DAC in [15] operates in parallel with a much more expensive network. Even though in theory it is possible to realise an n-bit DAC using all the above solutions, various restrictions may apply in practice due to fabrication technology related aspects, background charge fluctuations, and ultralow operating temperature. The limitations of the solution in [15] are mainly related to the large number of components and output feedback, whereas the solution in [16] suffers from the increase in the effective capacitance of the SET box to further reduce the operating temperature. Due to the small number of circuit components in our proposal, it is potentially less sensitive to fabrication technology related aspects and background charge fluctuations.

Furthermore, we could replace the SETT with a scaled-down MOSFET and realise the same DAC function. The MOSFET-based scheme has smaller temperature dependence and fabrication restrictions, but the SETT-based scheme has lower power dissipation and smaller size.

6 Conclusion

In summary, a SETT-based DAC is proposed. The proposed scheme fully utilises the Coulomb blockade effect and only a SETT and *n+1* capacitors is necessary for an *n*-bit DAC. Using this scheme, a 4-bit DAC is demonstrated by means of simulation.

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