Testing for Parasitic Memory Effect in SRAMs

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***Abstract*—Parasitic memory effect can occur due to the impact of parasitic node capacitances and faulty node voltages on the electrical behavior of SRAMs. This memory effect can cause detectable faults to become undetectable using existing industrial tests. This paper analyzes, evaluates and identifies the unique detection conditions for faults in SRAMs. It demonstrates the limitation of existing industrial tests that do not take the impact of parasitic memory effect into consideration. Finally, the paper presents March SME, a memory test that detects SRAM static faults in the presence of parasitic memory effect.**

***Index Terms*—Memory tests, parasitic memory effect, static faults, SRAMs.**

I. Introduction

Certain defects in today's integrated circuits exhibit complex behaviors that may not be accurately modeled by existing fault analysis approaches. This is due to the presence of factors such as parasitic memory effects, for example, which entails the presence of parasitic capacitance and varied node voltages on the memory's defective nodes.

In the presence of this effect, the fault coverage of existing memory tests is reduced, while test escapes and DPM rates increase. Test generation for such defects must depend on fault analysis that adequately models and represents this faulty behavior, and must allow for easy generation of test operations and algorithms.

Some work has been done on investigating resistive defects [1], [3], [6], [11], [12], [14], and the electrical characterization and modeling of resistive opens [2], [4], [5], [6], [7], [8], [12], [13], [14], [15]. but without considering the presence of parasitic components (capacitance and faulty node voltages) of the defective nodes. The presence of parasitic memory effect has been established in CMOS logic [13], [14] and in SRAMs [9], [10].

However, no memory tests exist nor detection mechanism been developed that account for this faulty behavior in SRAMs.

Therefore, the main contributions of this paper are as follows:

- Spice simulations, analysis and evaluation that identify and describe the detection conditions for faults in the presence of parasitic memory effect.
- An optimal test, March SME that detects these faults in the presence of parasitic memory effect.

The paper is organized in the following way. Section II presents the background for parasitic memory effect in SRAMs, while Section III discusses the impact of parasitic memory effect on static faults. Section IV presents the testing approach for parasitic memory effect, and Section V presents March SME that detects static faults in SRAMs. The paper is concluded in Section VI.

II. Parasitic memory effect in SRAMs

The presence of parasitic node capacitance (C_n) in the defective node has been shown to exacerbate the faulty behavior in SRAMs [10]. It can also induce the dependence of a faulty node's voltage on the voltage of previous operations; an effect that is known as parasitic memory effect.

In general, both the values of the defect resistance (R_{def}) as well as the parasitic capacitance (C_n) influence the timing behavior of the circuit, and therefore decide the eventual output of the memory. These two parameters create a space of possible (C_n, R_{def}) values that can be divided into two regions: pass and fail. For example, Figure 1 shows the plot of (C_n, R_{def}) for the write 1, read 1 sequence (seq = $\{$w1 r1$\}$) when defect R2c shown in Figure 2 has been injected, where the R_{cr} curve in the figure divides the (C_n, R_{def}) plane into the pass and fail regions. R_{cr} is the resistive value (critical resistance) for a specific operation in the R_{def} range, below which a cell functions properly despite the presence of a defect (the pass region), and above which the cell fails (the fail region).

Figure 1 shows that as C_n increases, the fail region expands, while the pass region decreases. This underscores the importance of C_n, and the need to account for it as an important component of the defective node.

Therefore, it is important to evaluate the impact of the parasitic memory effect on the faulty behavior of SRAMs. An understanding of this impact will facilitate the generation of high quality tests.

To describe the failure mechanism, we consider that the defective node (N) in the SRAM device is characterized by three important components, namely,

- The resistive defect (R_{def}) of the defective node
- The parasitic capacitance (C_n) of the defective node
- The voltage (V_n) on the defective node

Figure 2 shows all 18 open defect positions injected into the SRAM cell, and an example of parasitic capacitance on the defective node, assuming an open defect position R2. Open defects are usually caused by broken lines or particle

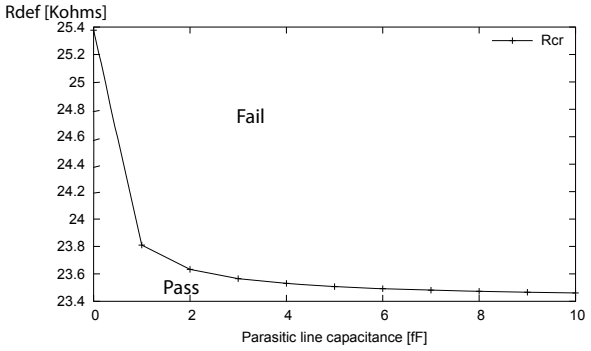

Fig. 1. Plot of R_{cr} (R_{def} against C_n values)

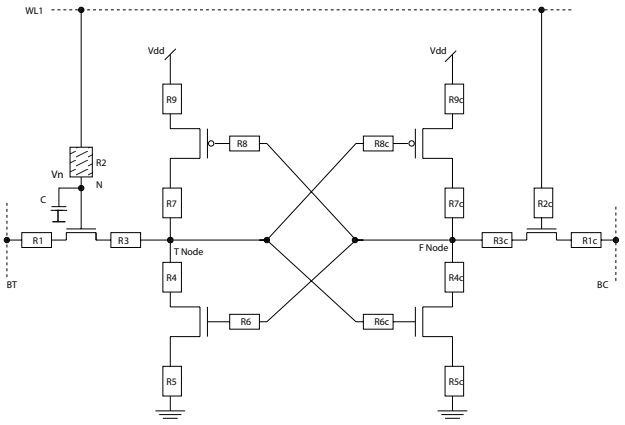

Fig. 2. SRAM cell showing R_{def} and C_{def}

contamination that result in increasing line resistivity at the open position.

Resistive opens combined with parasitic capacitance on a defective node, can modify the timing behavior of the circuit, which can cause faults. Such modified behavior can result in faults being manifested depending on the operating faulty voltage on the defective node. Such faults can only be detected using tests that expose the incorrect timing behavior due to these parasitic effects. This paper focuses on the generation of such tests.

III. Impact on static faults

This section briefly discusses functional fault models in Section III-A. It further presents the analysis of the impact of parasitic node components on the detection of single-cell static faults [9] in Section III-B.

A. Functional fault models

Functional fault models (FFMs) can be defined as a non-empty set of fault primitives (FPs). These FFMs and their corresponding FPs have been presented in [16].

FPs are denoted as $< S/F/R >$. S refers to a value or the operation sequence that sensitizes the fault, F describes the logic value in the faulty cell ($F \in \{0, 1\}$), and R describes the logic output value of a read operation ($R \in \{0, 1, -\}$). R has a value of 0 or 1 when the fault is sensitized by a read operation, while '$-$' is used when a write operation sensitizes the fault. For example, in the FP $< 1w0/1/- >$, which is the down-transition fault, $S = 1w0$ means that a $w0$ operation is applied to a cell initialized to 1. The fault effect $F = 1$ indicates that after performing $w0$, the cell remains in state 1. The output of the read operation (R = $-$) indicates that there is no expected output for the memory.

Static faults are faults that are sensitized by at most one operation. Two important FFM classes are the *single-cell* and *two-cell static* FFMs. This paper focuses on tests for single-cell static faults as listed in Table I.

TABLE I
SINGLE-CELL STATIC FFMS

Fault	Fault primitives	Fault	Fault primitives
SF_0	$< 0/1/- >$	RDF_0	$< 0r0/1/1 >$
SF_1	$< 1/0/- >$	RDF_1	$< 1r1/0/0 >$
TF_1	$< 0w1/0/- >$	$DRDF_0$	$< 0r0/1/0 >$
TF_0	$< 1w0/1/- >$	$DRDF_1$	$< 1r1/0/1 >$
WDF_0	$< 0w0/1/- >$	IRF_0	$< 0r0/0/1 >$
WDF_1	$< 1w1/0/- >$	IRF_1	$< 1r1/1/0 >$

B. Faulty behavior and static faults

In this section we summarize the analysis of the impact of parasitic node components on detection of single-cell static faults in SRAMs. We present the analysis for defect R2c, and thereafter show the summary for the remaining defects as tabulated in Table II. For these simulations an electrical Spice model of the SRAM cell has been used. In this model, the transistor parameters are based on the 65nm BSIM4 model card as described by the Predictive Technology Model [17].

1) Analysis of defect R2c: As shown in Figure 2, consider the defect R2c located between WL and the gate of the pass transistor on the F-node side, with the floating node between the pass transistor and the defect. An open between WL and the gate of the pass transistor on F-node side will limit connectivity to the gate such that the pass transistor will not function properly.

The essence of this simulation is to determine the impact of parasitic components of the faulty node (capacitance and varying floating node voltages) on the detection of the corresponding single-cell faults in SRAMs. An insight into this behavior will facilitate the proper detection of such faults.

The defect resistance R_{def} values of $0 < R_{def} < 10\text{G}\Omega$, varying floating node voltages of $0.0V < V_n < 1.2\text{V}$ and parasitic node capacitance, C_n, of 4.5fF are used. Note that other close values of C_n would yield the same behavior shown in this paper.

The operations $\{1r1,\ 0r0,\ 1w1,\ 1w0,\ 0w1$ and $0w0\}$ are applied. Note that at most one operation is applied at a

TABLE II
STATIC FAULTS FOR DEFECTS ON F-NODE SIDE

Defect	Defective node voltage (V_n) in Volts												
	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
R1c	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1
R2c	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	– TF_1	– TF_1	– TF_1	– TF_1	– –	– –	– –	– –	– –	– –
R3c	– TF_1	– TF_1	– TF_1	– TF_1	– TF_1	– TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1	IRF_1 TF_1
R4c	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1
R5c	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1	RDF_1
R6c	– RDF_1 – TF_0	– RDF_1 – TF_0	– RDF_1 – TF_0	– RDF_1 – TF_0	– – – TF_0	RDF_0 – WDF_0 TF_0	RDF_0 – WDF_0 TF_0	RDF_0 – WDF_0 TF_0	RDF_0 – WDF_0 TF_0	RDF_0 – WDF_0 TF_0	RDF_0 – WDF_0 TF_0	RDF_0 – WDF_0 TF_0	RDF_0 – WDF_0 TF_0
R7c	–	–	–	–	–	–	–	–	–	–	–	–	–
R8c	–	–	–	–	–	–	–	–	–	–	–	–	–
R9c	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	$DRDF_0$	–	–	–	–	–	–	–

time; therefore the analysis is static. Only static faults can be sensitized with such an analysis.

For the operation $1r1$, it was observed that at V_n values $0.0V < V_n < 0.2$V, the correct logic value is yielded by the sense amplifier at the output when R_{def} is in the range $1K\Omega < R_{def} < 100K\Omega$. However, for R_{def} = 1MΩ and above using the same V_n values, incorrect logic values are recorded at the output, but the content of the true node shows correct logic values for all simulated R_{def} values from 1KΩ to 10GΩ. Thus, at $0.0V < V_n < 0.2$V and for $1M\Omega < R_{def} < 10G\Omega$ at C_n = 4.5fF the cell exhibits an Incorrect Read Fault IRF_1 ($< 1r1/1/0 >$). Consequently, an inspection of the BLs indicates a distortion such that the difference in potential between the true BL and the complementary BL is greatly reduced for the values where the fails occurred, thereby making it hard for the sense amplifier to read the correct value from the cell.

However, with an increased faulty node voltage of $0.3V < V_n < 1.2$V no fail is observed. This underscores the importance of taking into consideration the parasitic effects of the faulty node during fault detection.

In the same way, using seq = $\{0w1\}$, we evaluate the impact on the faulty behavior of the cell by observing the content of the true node. The results show that for V_n values in the range $0.0V < V_n < 0.6$V when $1K\Omega < R_{def} < 100K\Omega$ the true node shows that the cell contains the expected correct logic 1 value indicating a successful write transition. But, when $1M\Omega < R_{def} < 10G\Omega$, incorrect logic 0 value is observed at the true node. Thus, at $0.0V < V_n < 0.6$V, when $1M\Omega < R_{def} < 10G\Omega$ the cell exhibits the Transition Fault TF_1 ($< 0w1/0/- >$).

However, at $0.7V < V_n < 1.2$V for all simulated values of R_{def} $1K\Omega < R_{def} < 10G\Omega$ the true node shows that the cell contains correct logic 1 and did not fail. Using the operation $\{1w1\}$, the performed operation successfully passed and the true node shows that the cell contains the expected correct logic 1 value. Likewise, using the operation $\{0w0\}$ and seq = $\{1w0\}$, both operations passed irrespective of the value of the parasitic components used.

2) Analysis for other defect positions: This section summarizes some results of the analysis for the faulty behavior of open defects in the SRAM cell.

Table II and Table III list results for defects shown in Figure 2. In each table, the first column indicates the defects considered, while the first row lists the defective node voltages simulated. For all operation sequences performed, the detected faults are listed against the corresponding defective node voltage value at which the fault is detected. The entry '-' indicates the absence of a fault for the corresponding defect and/or defective node voltage listed.

IV. TESTING FOR PARASITIC MEMORY EFFECT

A. Challenges of static faults detection

Since the detection of faults can depend on the floating node voltages, most available industrial tests may not be able to properly detect static faults in the presence of the parasitic memory effect. Therefore, it is important to consider this factor while developing memory tests.

As shown in Tables II and III, it is clear that certain single-cell static faults are only observed at specific V_n values and not throughout the whole range of the faulty node's voltage. The fact that the faulty behavior depends on the different parameters of the parasitic node underscores the importance of taking into consideration the presence of parasitic memory effects on the faulty node during fault detection. Whereas the value of the defective resistance cannot be readily predetermined or influenced by external operations, it is possible to influence and determine the value of the parasitic node voltage using memory operations, such that the appropriate V_n values are initialized in the faulty nodes prior to sensitization and detection. In this way, one can ensure proper detection of the occurring faults in the presence of the parasitic memory effect.

Thus, it is important to specifically identify what memory operations that would necessitate the required variations in V_n, and then develop suitable tests using these detection conditions.

TABLE III
STATIC FAULTS FOR DEFECTS ON T-NODE SIDE

Defect	Defective node voltage (V_n) in Volts												
	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
R1	–	–	–	–	–	–	–	–	–	–	–	–	–
R2	–	–	–	–	–	–	–	–	–	–	–	–	–
R3	–	–	–	–	–	–	–	–	–	–	–	–	–
R4	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0
R5	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0	RDF_0
R6	RDF_0 –	RDF_0 –	RDF_0 –	RDF_0 –	RDF_0 –	– $DRDF_1$	– –	– RDF_1	– RDF_1	– RDF_1	– RDF_1	– RDF_1	– RDF_1
R7	–	–	–	–	–	–	–	–	–	–	–	–	–
R8	–	–	–	–	–	–	–	–	–	–	–	–	–
R9	–	–	–	–	–	–	–	–	–	–	–	–	–

B. Detection requirements for single-cell faults

Now, for the simulation an electrical Spice model of the SRAM cell has been used. In this model, the transistor parameters are based on the 65nm BSIM4 model card. The defect resistance R_{def} of $0 < R_{def} < 10\text{G}\Omega$ with logarithmic incremental steps of 1, 10, 100, 1000, etc., and parasitic node capacitance C_n of 4.5fF are used. Note that other close values of C_n will yield the same behavior shown in this paper.

Each injected resistive open within the cell creates a floating node (V_n), whose voltage varies between GND and V_{DD}. A floating node is a memory node that is not properly controlled by a memory operation due to a defect, which leads to an improper voltage on the floating node at the end of the operation. The analysis require performing memory operations, while observing the impact on V_n. For all injected defects, the performed memory operations are write-0 ($w0$), read-0 ($r0$), write-1 ($w1$), and read-1 ($r1$). For each fault, the failing V_n range is simulated and determined.

Our aim is to determine what specific memory operations are needed to ensure that the required V_n range is induced prior to sensitization and detection of each fault.

Now, three important phases are considered during test development and generation, namely, the *initialization*, *sensitization* and *detection* phases. This work focuses on the initialization phase. The reason is that the sensitization and detection requirements for the faults remain the same, whereas the initialization conditions (appropriate V_n range) required for proper sensitization must be induced. For detection of a given type of faulty behavior in the presence of parasitic memory effect, a test must ensure that the required V_n range is initialized prior to sensitization and detection.

Note that on the one hand, different faults require different V_n ranges to be detected. For example, Table II shows that to detect an Incorrect Read Fault (IRF_1) caused as a result of defect R3c, V_n should be in the range $0.6\text{V} < V_n < 1.2\text{V}$, below which the fault could be undetectable. On the other hand, the same fault model induced when a specific defect has been injected could have different V_n requirement when induced by another injected defect. For example, the Incorrect Read Fault (IRF_1) observed when R2c is injected requires a lower V_n range, while the same Incorrect Read Fault (IRF_1) induced in the presence of R3c requires higher V_n range. These unique requirements have been accounted for in our analysis.

Figure 3(a) shows simulation results for multiple $w0$ operation performed when defect R2c is injected for the detection of the Transition Fault (TF_1). Assuming a scenario, where V_n = V_{DD} = 1.2V, the figure shows that when the operation is performed, V_n significantly decreases from 1.2V to between 0.4V and 0.5V. The figure also shows that a single $w0$ will not be sufficient to appropriately initialize V_n to any value lower than 0.6V at which this fault can be detected.

Likewise, assuming a scenario, where V_n = GND = 0.0V, Figure 3(b) shows that the performed multiple $w0$ operations causes V_n to increase from 0.0V to about 0.5V at which the fault can be detected. In addition, a single $w0$ operation could be sufficient to initialize V_n of lower than 0.6V such that this fault can also be detected.

Furthermore, Figure 4 shows the simulation result for multiple $w0$ operations when defect R6 on the T-node's side is injected. The figure shows that for multiple $w0$ operations, V_n increases from 0.0V to about 1.0V at which the Read Destructive Fault (RDF_1) is detected. It also shows that a single $w0$ operation will initiate V_n at a value less than the 0.5V value necessary for detecting Read Destructive Fault (RDF_0).

Table IV presents a summary of the initializing operations that yield proper conditions for the sensitization and detection of the occurring fault models. In the table, the first column lists the defects, while the second column states the fault model. The third column lists the R_{def} range where the corresponding fault occurs, while the fourth column gives the required V_n range to enable sensitizing the fault. The entries in this column are *high* indicating that a V_n is needed between 0.6V to 1.2V, and *low* which implies values between 0.0V to 0.6V. The fifth column lists the initializing operations needed to achieve the required V_n values. An entry $'-'$ indicates that no operation is able to initialize V_n to the required voltage range needed to sensitize the fault. This means that we only need to test for those faults that can be initialized to the required V_n. The sixth column states the sensitizing operations for the fault model.

V. MARCH SME

Several tests exist that are generated to detect all single-cell static faults, but from the analysis in this paper, several such tests will not detect these faults in the presence of parasitic memory effect. For example, March SSS shown

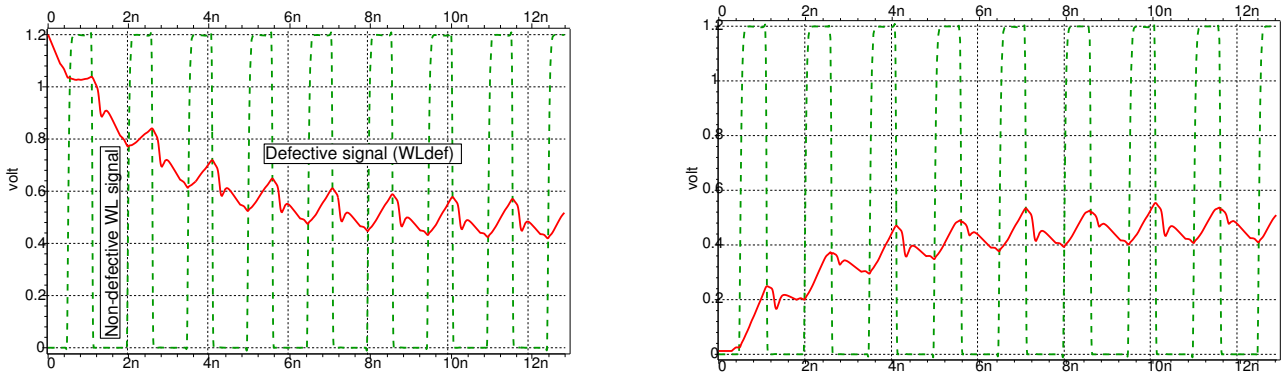

Fig. 3. Impact on V_n when R2c is injected. (a) when V_n = 1.2V and (b) when V_n = 0.0V

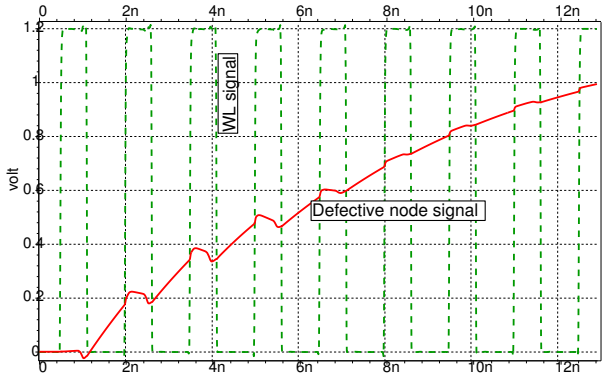

Fig. 4. Impact on V_n when R6 is injected

below is an optimal test for detecting all single-cell static faults. To detect these faults, March element ME0 initializes the memory to 0. ME1 starts by sensitizing TF_1 during the first $w1$ operation, then WDF_1 during the second $w1$ operation. These two faults are detected during the first $r1$ of ME1, which also sensitizes and detects SF_1, RDF_1 and IRF_1. Finally, the second $r1$ operation of ME1 sensitizes and detects $DRDF_1$. The complementary counterparts of these faults are sensitized and detected in the same way by ME2.

However, March SSS will not detect all these faults in the presence of parasitic memory effect. This is true since no march element in March SSS ensures the required initialization to sensitize and detect these faults.

$$\begin{aligned}\text{March SSS} = \{\ & \Updownarrow(w0); && \text{ME0}\\ & \Updownarrow(w1,w1,r1,r1); && \text{ME1}\\ & \Updownarrow(w0,w0,r0,r0)\} && \text{ME2}\end{aligned}$$

Now, we present March SME, a test that detects single-cell static faults shown in Table IV in the presence of parasitic memory effect.

$$\begin{aligned}\text{March SME} = \{\ & \Updownarrow(w0,(r0)^i); && \text{ME0}\\ & \Updownarrow(w1,w1); && \text{ME1}\\ & \Updownarrow(r1)^i; && \text{ME2}\\ & \Updownarrow(w0)^i; && \text{ME3}\\ & \Updownarrow(r0,r0); && \text{ME4}\\ & \Updownarrow(w1,r1)\} && \text{ME5}\end{aligned}$$

In March SME, $(op)^i$ represents the number of times (i) that an initialization operation (op) is performed. The test has a time complexity of $7n$+$3n \cdot i$. This test ensures that the required operations are performed on a given cell that would yield exactly the proper range of initializing voltage. It ensures the detection of single-cell static faults both in the presence and absence of parasitic memory effect in the following way.

1. *Detection in the absence of parasitic memory effect*

In march element ME0 the entire memory is initialized to 0. ME1 starts by sensitizing TF_1 during the first $w1$ operation, then WDF_1 during the second $w1$ operation. These two faults are detected during the first $r1$ of ME2, which also sensitizes and detects SF_1, RDF_1 and IRF_1, as well as $DRDF_1$ in the subsequent read. In ME3, TF_0 is sentistized during the first $w0$ operation, and WDF_0 during the second $w0$. These two faults are detected during the first $r0$ of ME4, which also sensitizes and detects SF_0, RDF_0 and IRF_0, as well as $DRDF_0$ in the second $r0$.

2. *Detection in the presence of parasitic memory effect*

March element ME0 initializes the entire memory to 0, while a subsequent $(r0)^i$ initializes the required low V_n value for the fault TF_1 associated with the defect R2c shown in Table IV. ME1 starts by sensitizing TF_1 during the first $w1$ operation, which is detected during the first $r1$ of ME2. In addition, $(r1)^i$ of ME2 also initializes the required high V_n and ensures the sensitization and detection of IRF_1 associated with R3c. Subsequently in ME3, $(w0)^i$ ensures the initialization of the required V_n value and sensitization of WDF_0 associated with R6c, which is then detected by the first $r0$ in ME4. RDF_0 associated with R6c is also initialized in ME3, then sensitized and detected in ME4. Finally, ME3 also initializes the required V_n for sensitizing RDF_1 associated with R6,

TABLE IV
DETECTION CONDITIONS FOR SINGLE-CELL FFMS

Defect	Fault	R_{def} (KΩ)	Required V_n	Initializing op	Sensitizing op
R2c	TF_1	> 100	Low	$w0, w1, r0, r1$	$0w1$
	IRF_1	> 1000	Low	—	$1r1$
R3c	IRF_1	> 1000	High	$w0, r1, r0$	$1r1$
R6c	WDF_0	> 100	High	$w0, w1, r1$	$1w1$
	RDF_0	> 1000	High	$w0, w1, r1$	$0r0$
	RDF_1	> 1000	Low	—	$1r1$
R9c	RDF_0	> 1000	Low	—	$0r0$
R6	RDF_0	> 1000	Low	—	$0r0$
	RDF_1	> 100	High	$w0$	$1r1$

which is sensitized and detected in ME5.

VI. CONCLUSION

This paper has evaluated the impact of parasitic memory effect on single-cell static faults in SRAMs. The paper has demonstrated that the detection of these faults is significantly influenced by the parasitic components of the defective node, and that proper initialization is key to detecting them. The paper has simulated and presented detection requirements of each fault model. Finally, the paper presented March SME, which detects all single-cell faults simulated in this paper in the presence and absence of the parasitic memory effect.

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